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A 25 Gbps VCSEL Driving ASIC for Applications in High-Energy Physics Experiments

Due to the advantages in density, bandwidth and radiation performance of VCSEL-based array optical transmission system, it has been prevailingly researched and used for the front-end data acquisition in high-energy physics experiments [1]. This paper presents the design and the test results of a 25 Gbps VCSEL driving ASIC fabricated in 55 nm CMOS technology as a continuous development of the previous 14 Gbps/ch driver [2].
The whole ASIC consists of four independent channels, and each channel has the fixed channel height of 250 μm to keep the whole ASIC as the array form fitting with a four channel VCSEL array. The 25 Gbps VCSEL driver is implemented as one of the four channels. The 25 Gbps VCSEL driver is composed of an input equalizer stage, a limiting amplifier stage and an output driver stage with multiple novel peaking and pre-emphasis techniques. The input equalizer stage adopts a 5-step continuous-time linear equalizer (CTLE) structure [3] to compensate the high frequency losses from the system level including PCB traces, bonding wires and pads. The CTLE boosts maximum up to 5.8 dB at 18 GHz while providing a DC gain of 4.7 dB. To obtain sufficient swing and high bandwidth, the limiting amplifier uses the passive shared inductor structure and active feedback circuit [4]. The output driver stage consists of a main driver stage and an emphasis driver stage. A passive inductor peaking technique is integrated with the traditional structure in the main driver stage. Besides, the feedforward capacitor compensation [5] and T-coil technique [6] are both used in main driver to further enhance the bandwidth. The emphasis driver stage uses the programmable delay unit to acquire the desired pre-emphasis components with adjustable timings to be added with the main signal. The 25 Gbps VCSEL driver can be controlled by the SPI module with the Triple Modular Redundancy (TMR) structure.
The whole ASIC features a size of 2 mm x 2 mm with 52 pads. The 25 Gbps VCSEL driver has a size of 2 mm x 0.25 mm. Widely-open 25 Gbps eye has been observed at the typical settings of 2 mA bias current and 5 mA modulation current in the post layout simulation, and the power consumption is 130 mW when working at 25 Gbps. The chip has been taped out and the tests are planned to be conducted in this April. The driver ASIC will use chip on board (COB) measurement setup, and is wire bonded to an 850 nm VCSEL. The optical test, electrical test and total ionizing dose (TID) test will be performed. The test results will be reported in the meeting.

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[3] S. Gondi et al., A 10 Gb/s CMOS Adaptive Equalizer for Backplane Applications, IEEE ISSCC 2005 (2005) 328-329.
[4] T.-C. Huang et al., A 28 Gb/s 1pJ/b shared-inductor optical receiver with 56% chip-area reduction in 28 nm CMOS, IEEE ISSCC 2014 (2014) 144-145.
[5] Daniel Kucharski et al., A 20Gb/s VCSEL Driver with Pre-Emphasis and Regulated Output Impedance in 0.13μm CMOS, IEEE ISSCC 2005 (2005) 222-223.
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