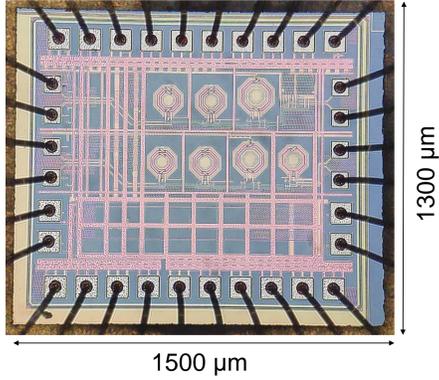


LDLA14: a 14 Gbps optical transceiver ASIC in 55nm for High-Energy Physics Experiments



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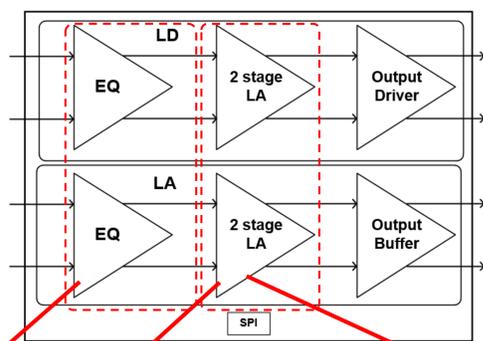
Introduction



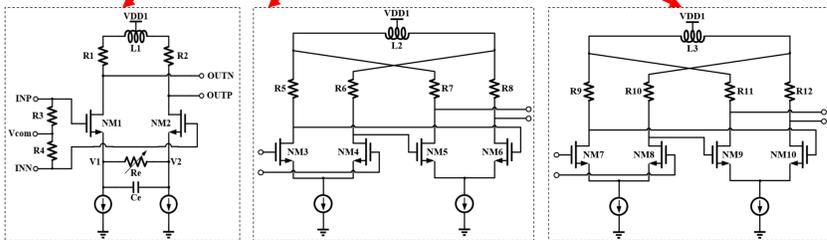
14 Gbps optical transceiver ASIC (LDLA14)

- ◆ LDLA14 is a single channel, 14Gbps optical transceiver ASIC, fabricated with a 55 nm CMOS technology. The chip is designed to be a part of the optical link ASICs in the high-energy physics experiments front-end readout electronics.
- ◆ The LD would drive the external TOSA (Transmitter Optical Subassembly) to generate optical signal for the transmitting side. The LA receives the signal from ROSA (Receiver Optical Subassembly) to provide standard electrical signal for the receiving side.
- ◆ The dimension of the LDLA14 is 1.5 mm × 1.3 mm, including 32 PADs.
- ◆ The output driver of LD adopts a novel structure of capacitive coupling pre-emphasis circuit. The test results show that both the LD and LA output widely-open eye diagrams at data rate of 10 Gbps, and a better eye diagram can be obtained at 14 Gbps rate. The power consumption of LDLA14 is 145mW at 14 Gbps data rate.
- ◆ LDLA14 die was wire bonded to the PCB test board, and the chip completed the optical eye diagram test.

The design of LDLA14



LDLA14 schematic

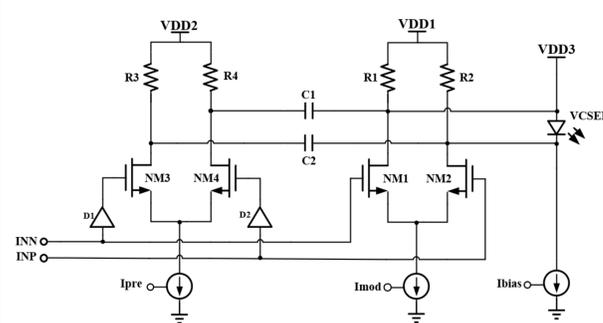


Equalizer

LA_Stage1

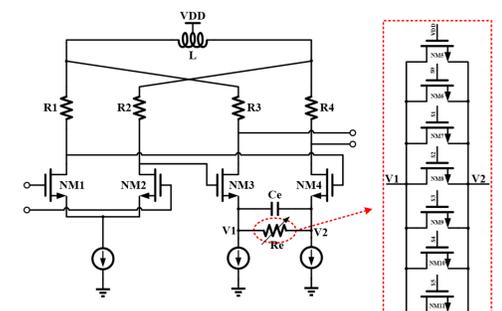
LA_Stage2

- ◆ LD consists of an equalizer (EQ), limiting Amplifier (LA) and an output driver. LA consists of an equalizer (EQ), limiting Amplifier (LA) and an output buffer.
- ◆ LD and LA in LDLA14 adopt the same structure of EQ and LA, the difference is the output stage.



Output driver of LD

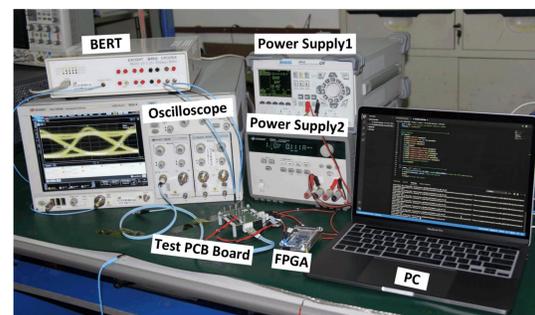
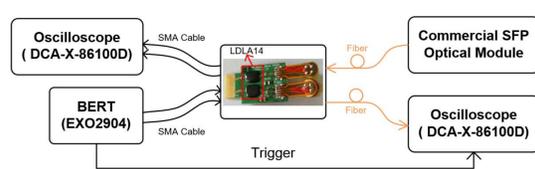
- ◆ For the output stage in LD, a novel structure of capacitive coupling pre-emphasis is proposed to compensate the nonlinear characteristics of VCSEL in TOSA and improve the quality of output eye diagram.
- ◆ The AC coupling capacitor isolates the DC signal of the pre-emphasis circuit and superimposes the high-frequency signal to the output stage to achieve the pre-emphasis effect.
- ◆ Compared with the traditional pre-emphasis structures, the proposed design would not sacrifice the modulation current swing to obtain the same bandwidth boost effect.



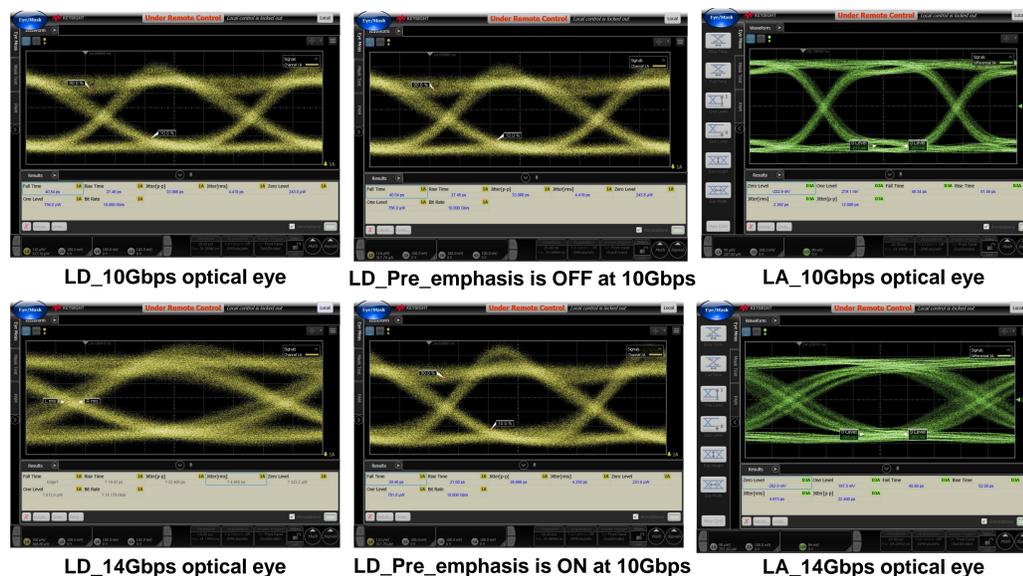
Output buffer of LA

- ◆ The output stage in LA uses two-stage cascaded differential circuits to drive off-chip loads.
- ◆ A R-C degenerated pre-emphasis is combined within the shared inductor structure into the output stage to further optimize the eye diagram.
- ◆ Adopts shared inductors to further expand the output stage bandwidth.
- ◆ The strength of the pre-emphasis can be configured via SPI module.

Optical eye diagram testing set up and test results of LDLA14



LDLA14 optical eye diagram testing set up



LD_10Gbps optical eye

LD_Pre_emphasis is OFF at 10Gbps

LA_10Gbps optical eye

LD_14Gbps optical eye

LD_Pre_emphasis is ON at 10Gbps

LA_14Gbps optical eye

- ◆ **Eye diagram test of LD:** The test result shows that the peak-to-peak jitter and the rms jitter of the 14 Gbps eye diagram is 32.4 ps and 4.4 ps, respectively. The peak-to-peak jitter and the rms jitter of the 10 Gbps eye diagram is 33.0 ps and 4.4 ps, respectively.
- ◆ **Pre-emphasis test of LD:** The test result show that the eye diagram amplitude will not decrease when the pre-emphasis function is turned on compared with turn off.
- ◆ **Eye diagram test of LA:** The test result shows that the peak-to-peak jitter and the rms jitter of the 14 Gbps eye diagram is 22.4 ps and 4.9 ps, respectively. The peak-to-peak jitter and the rms jitter of the 10 Gbps eye diagram is 12.0 ps and 2.3 ps, respectively.

Conclusion

- ◆ Both LD and LA have completed all individual optical tests.
- ◆ LDLA14 completed equalizer and pre-emphasis tests.
- ◆ Use the optical signal output by the LD as the input signal of the LA to complete the loop test of the transmitting channel and the receiving channel.

Acknowledgments

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