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# LDLA14: a 14 Gbps optical transceiver ASIC in 55nm for High-Energy Physics Experiments

High speed and radiation tolerant optical link has been prevailing used between the front-end detector and the back-end data acquisition in the high-energy physics experiments. The optical transceiver (driver/receiver) ASIC is the key component within the optical data transceiver systems. This paper presents the design and test results of an optical transceiver ASIC fabricated in 55 nm CMOS technology. The chip is designed to be a part of the optical link ASICs in the Nuclotron-based Ion Collider fAcility (NICA) [1] front-end readout electronics. NICA is a new accelerator complex designed at the Joint Institute for Nuclear Research (Dubna, Russia) to study properties of dense baryonic matter.

This ASIC (LDLA14) consists of a laser driver module (LD) and a limiting amplifier module (LA) both operating at 14 Gbps. The LD would drive the external TOSA (Transmitter Optical Subassembly) to generate optical signal for the transmitting side. The LA receives the signal from ROSA (Receiver Optical Subassembly) to provide standard electrical signal for the receiving side.

Both the LD and LA are composed of input stage, four-stages limiting amplifiers with feedback circuit and output stage with pre-emphasis. The same designs of input stage and limiting amplifiers are used in LD and LA. The input stage adopts the CTLE (Continuous Time Linear Equalizer) equalizer structure to compensate for the high frequency signal attenuation caused by the transmission lines on PCB, the bonding wires and input pads. The four-stage limiting amplifiers aims at amplifying a wide range of the signals output from equalizer to the saturation level. In order to improve the bandwidth of four-stage limiting amplifiers and minimize the chip area, an inductor is shared between adjacent amplifier stages. To accommodate the Process, Voltage and Temperatures (PVT) variations, an adjustable active feedback circuit is also used within the limiting amplifiers. The strength of the active feedback can be configured via SPI module.

For the output stage in LD, a novel structure of capacitive coupling pre-emphasis is proposed to compensate the nonlinear characteristics of VCSEL [2] in TOSA and improve the quality of output eye diagram. Compared with the traditional pre-emphasis structures [3][4], the proposed design would not sacrifice the modulation current swing to obtain the same bandwidth boost effect. The output stage in LA uses two-stage cascaded differential circuits to drive off-chip loads. Besides, a R-C degenerated pre-emphasis is combined within the shared inductor structure into the output stage to further optimize the eye diagram.

The dimension of the LDLA14 is 1.5 mm x 1.3 mm, including 32 PADs. The post-layout simulation results show that both the LD and LA output widely-open eye diagrams at data rate of 14 Gbps with total power consumption of 190 mW. The ISI (Inter symbol Interference) jitters of LD and LA of eye diagrams are 11 ps and 8 ps, respectively. This chip has been taped out and the tests are planned to be conducted in this April. The plan includes optical eye diagram test of LD, electrical eye diagram test of LA, the bit error ratio (BER) link test of LALD14 and total ionizing dose (TID) irradiation test of the whole chip. The test results will be reported in the meeting.

[1] https://nica.jinr.ru/

[2] Yazaki, Toru et al., 25-Gbps×4 optical transmitter with adjustable asymmetric pre-emphasis in 65-nm CMOS. 2692-2695. 10.1109/ISCAS.2014.6865728.

[3] W. Zhou et al., “LOCld65, a Dual-Channel VCSEL Driver ASIC for Detector FrontEnd Readout,” in IEEE Transactions on Nuclear Science, vol. 66, no.7, pp.1115-1122, July 2019.

[4] Chen, Y., Gong, J., Yao, J. and Tian, L. (2015), 4-channel 35 Gbit/s parallel CMOS LDD. Electron. Lett., 51: 1178-1180. https://doi.org/10.1049/el.2015.0885

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