# 18k Pixel Readout IC for CdTe Detectors Operating in Single Photon Counting Mode with Interpixel Communication

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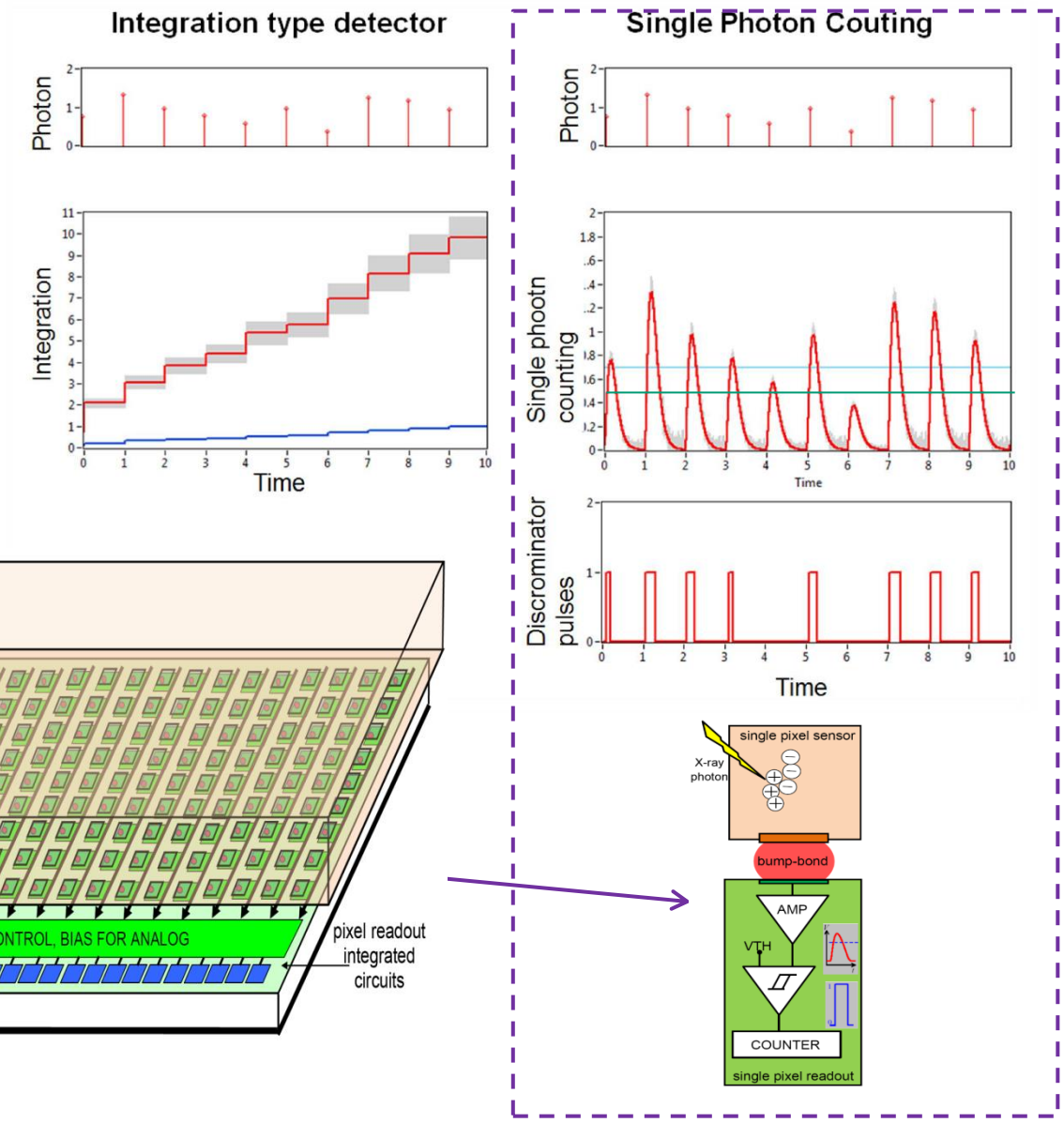
# Outline

1. Introduction
   - Hybrid Pixel Detectors
   - Single Photon Counting vs Integrating
2. Charge sharing effect , existing solutions
3. Multithreshold Pattern Recognition Algorithm for charge sharing compensation
4. MPIX readout IC  with 18k pixels with implemented algorithm
5. Measurements of MPIX 18k integrated circuit
6. Summary

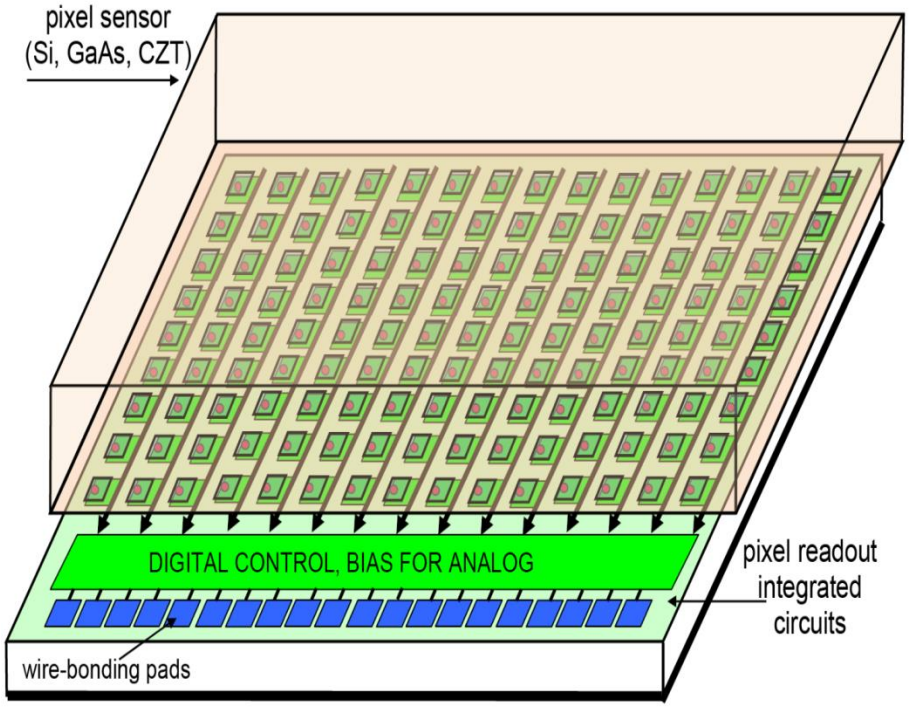
# Readout type:
# Integration vs. Photon Counting Detectors




**SPC detector:**
**- noiseless imaging,**
**- energy bins are possible**
**- leakage current compensation - simple**

**Smaller pixel size:**
**1. Count rate/area ↑**
**2. Position resolution ↑**
**3. Charge sharing effects**

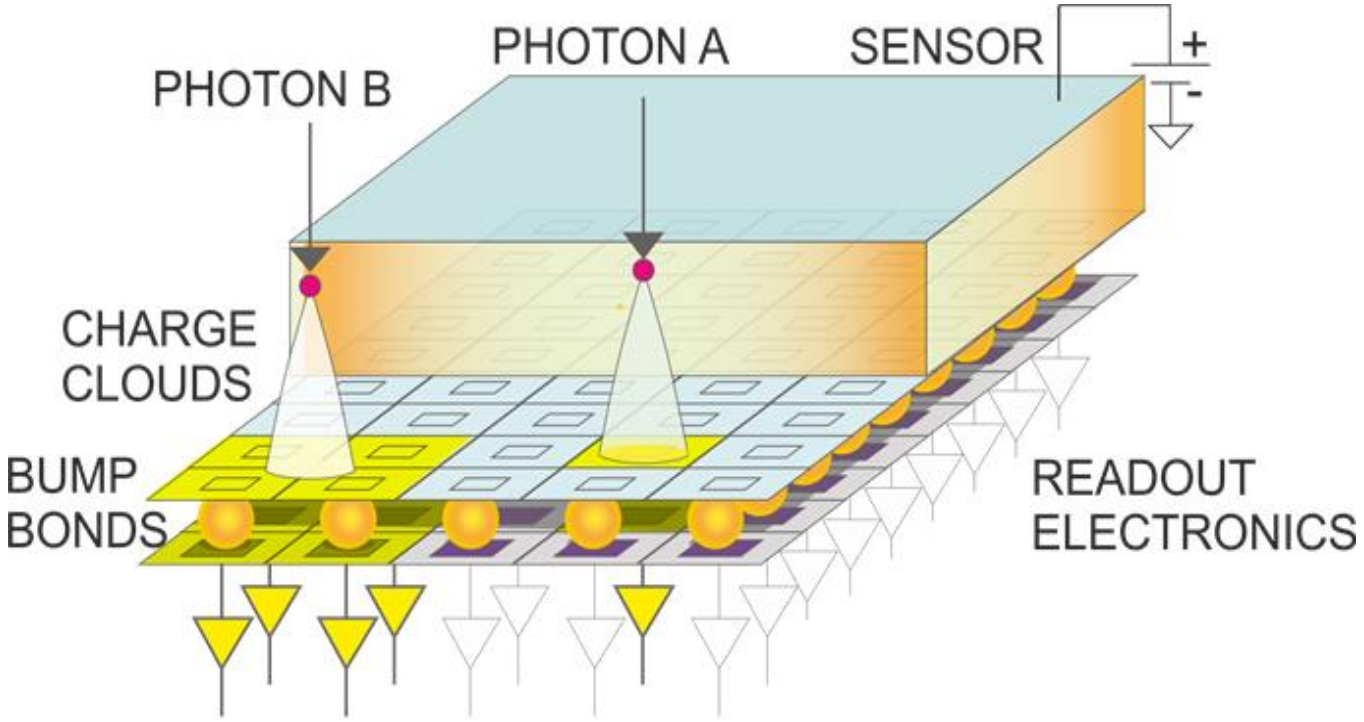
# Detector material suitable for given X-ray energy range




A standard 300 μm thick Si detector converts :
8 keV ~ 100 % of X-ray.
20 keV ~ 27% of X-ray.
60 keV ~ 2% of X-ray.

| Parameter | Si | Ge | GaAs | CdTe | CdZnTe | Diamond# |
|---|---|---|---|---|---|---|
| Average Z | 14 | 32 | 31/33 | 48/52 | 48/30/52 | 6 |
| Energy bandgap [eV] | 1.12 | 0.67 | 1.43 | 1.44 | ~1.6 | 5.48 |
| Density [g/cm$^3$] | 2.3 | 5.3 | 5.4 | 6.1 | 5.8 | 3.5 |
| Energy for electron-hole pair generation [eV] | 3.64 | 2.96 | 4.2 | 4.43 | ~4.6 | 13.1 |
| Mobility at $T$=300K [cm$^2$/Vs] | | | | | | |
| - electrons | 1350 | 1900 | 8000 | 1100 | ~1000 | 1800 |
| - holes | 480 | 3900 | 400 | 100 | ~100 | 1200 |
| Carrier lifetime [μs] | ~250 | 250 | 0.001–0.01 | ~0.1–2 | ~0.1–2 | 0.001 |

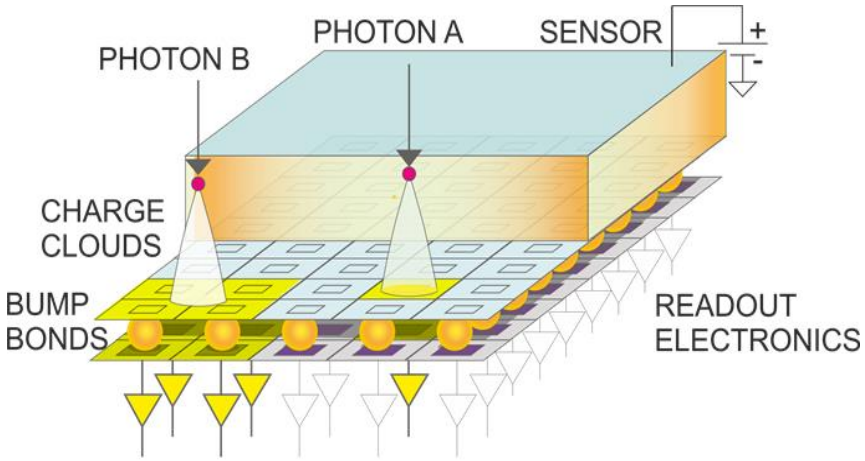
# Important problem – charge sharing

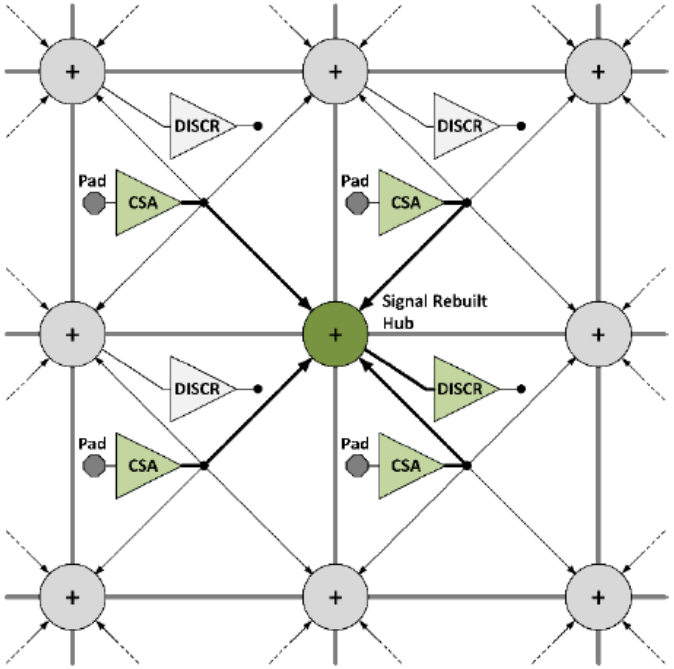



**Charge sharing depends on**: pixel size, detector thicknes, bias voltage, etc

**Example of ASICs with charge sharing compensation:**
Medipix3RX, miniVIPIC, X-Counter, PIXIE-3, Chase Jr, ….

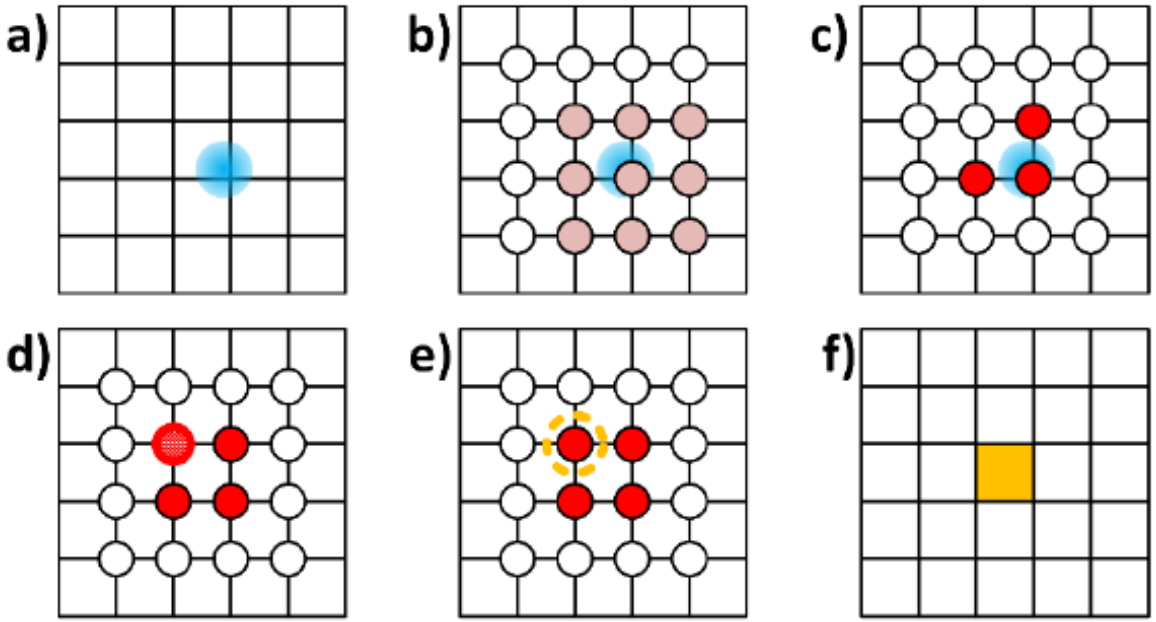
# Charge sharing solution – interpixel communication
(both in analog and digital domain)




**1) Analog domain** – charge reconstruction (4 neighbour pixels)
**2) Digital domain** – charge allocation in digital domain

# Pattern Recognition (PR) algorithm operation
(monoenergetic X-ray radiation)

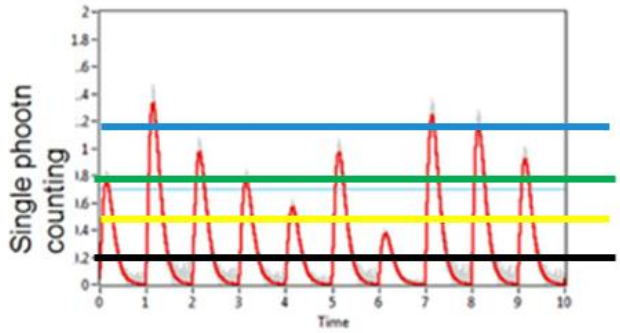


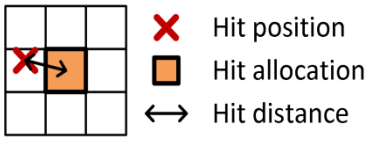

a) charge cloud formation and collection, b) Signal Rebuilt Hubs (SRH) which registered fractional signals, c) SRH which exceeded a threshold set to the half of the photon energy, d) SRHs after 1st step of PR algorithm – closing the neighborhood, e) top-left SRH selected by PR algorithm, f) the winning pixel to allocate the hit.

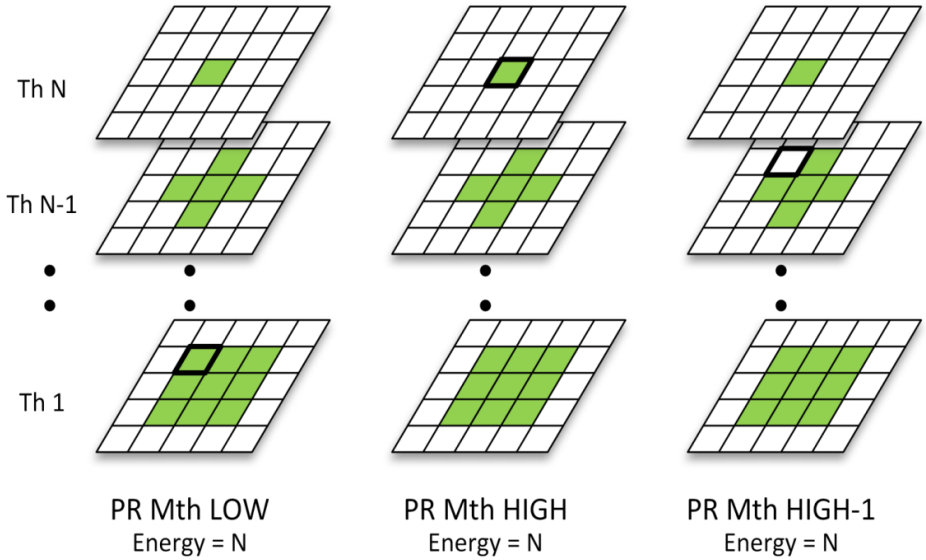
P. Otfinowski,, NIM A, v. 882, 2018, p.91-95
P. Otfinowski, et al., JINST, 2019, C01017

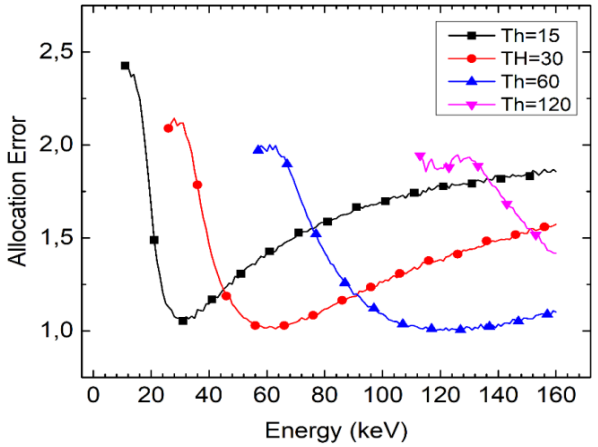
# Multithreshold Pattern Recognition

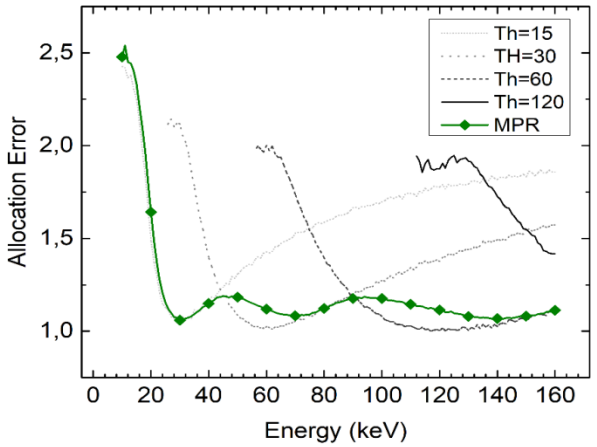
## Allocation threshold selection for MPIX chip



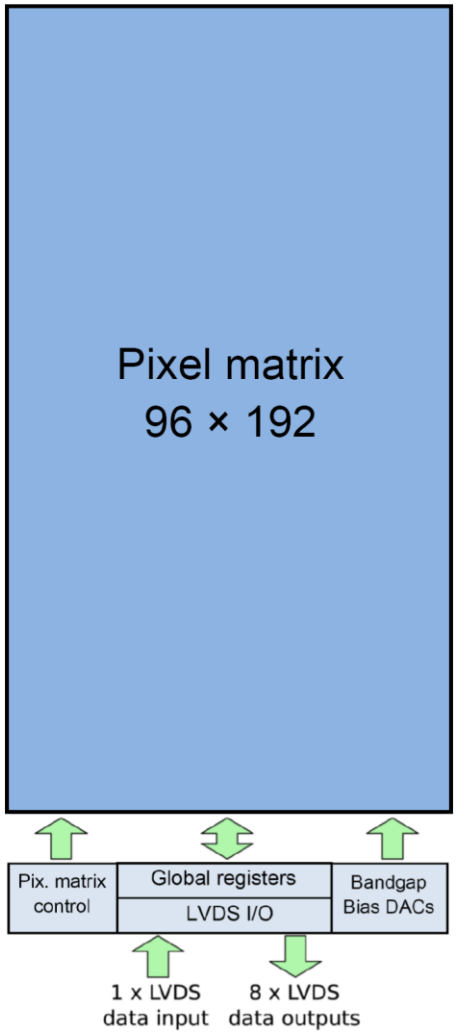

Based on the pattern – the best threshold level for allocation is automatically selected

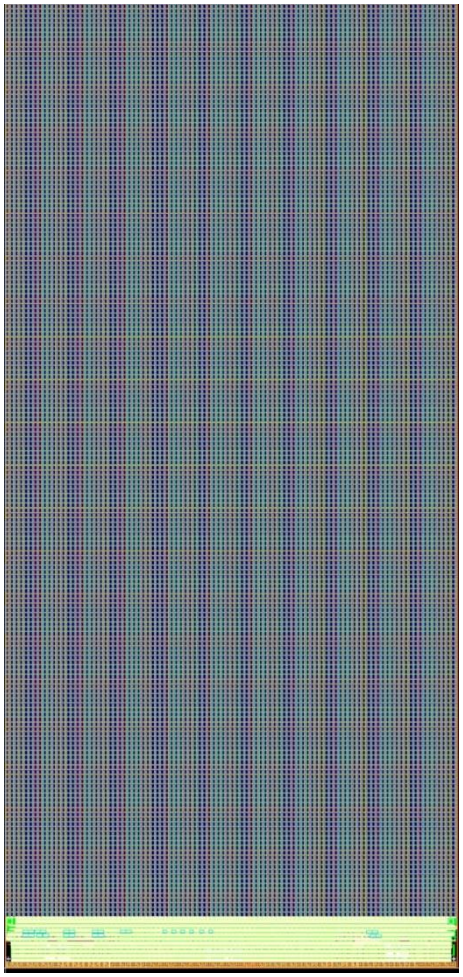
**The normalized allocation error is defined as the standard deviation of the computed distance D normalized to standard deviation of the distance of an ideal, square pixel detector (without charge sharing, parameter spread or noise).**

*Details see: P. Otfinowski, et al., 2019 JINST 14 C01017*

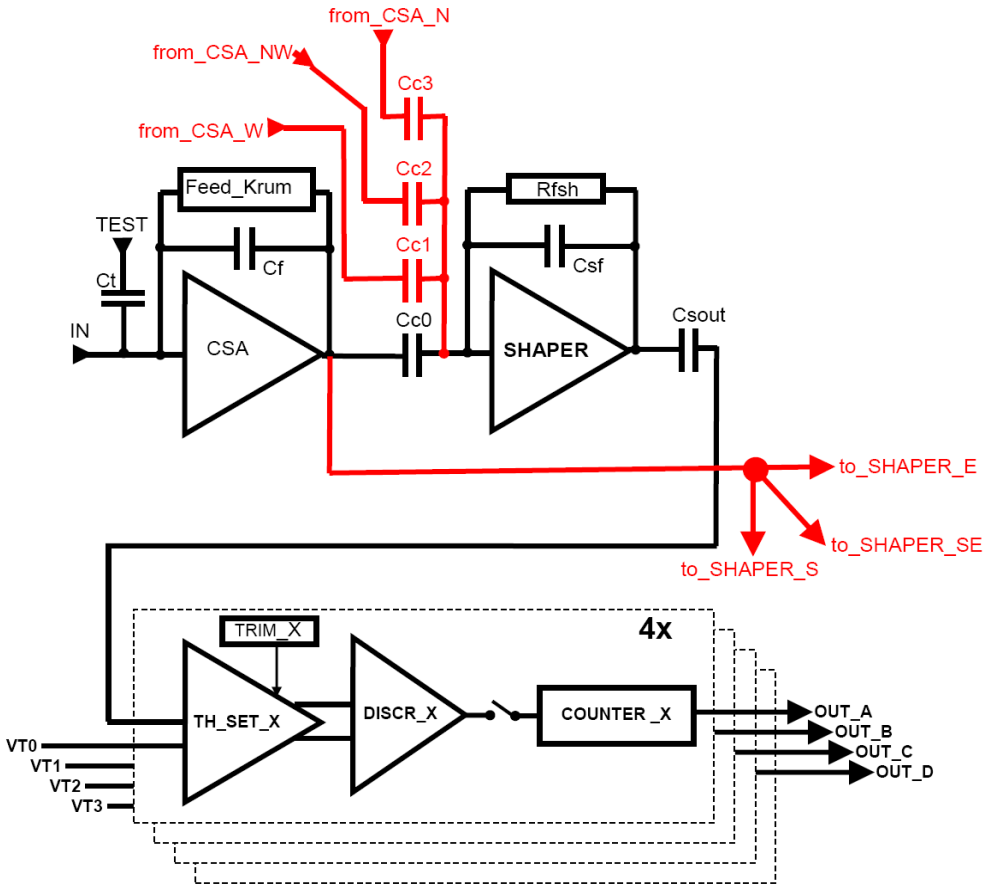
# MPIX (Multithreshold Pixels) IC architecture

MPIX: **96 x 192 =18.432 pixels (size 100 x 100 um$^2$)**
Techn. TSMC CMOS 0.13 μm, 8 metal layers, die size: X=9.631,56 um Y=20.290,89 um

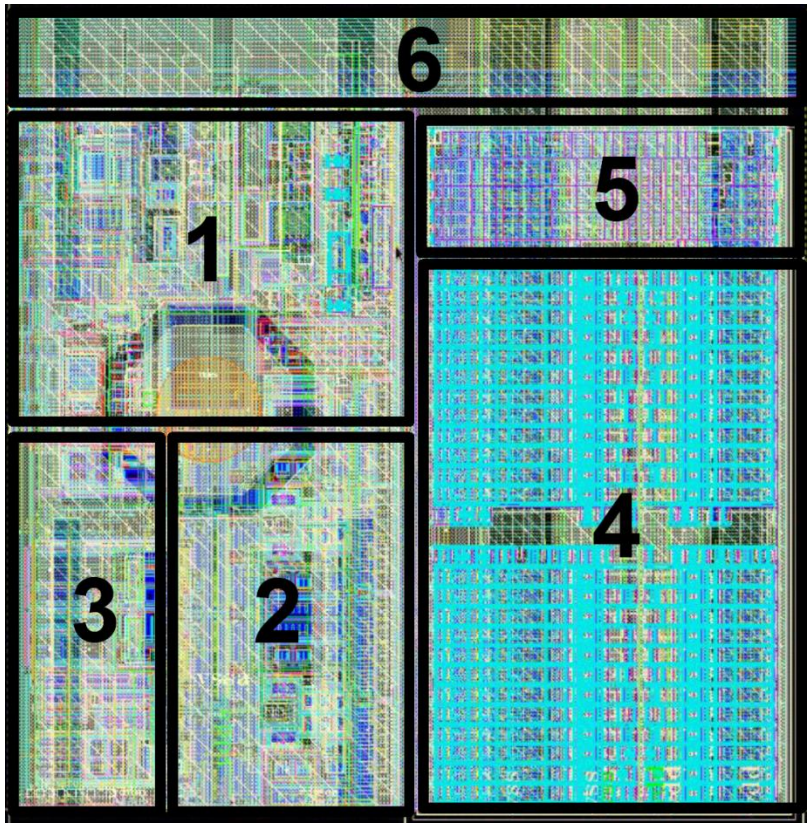


# Single pixel architecture

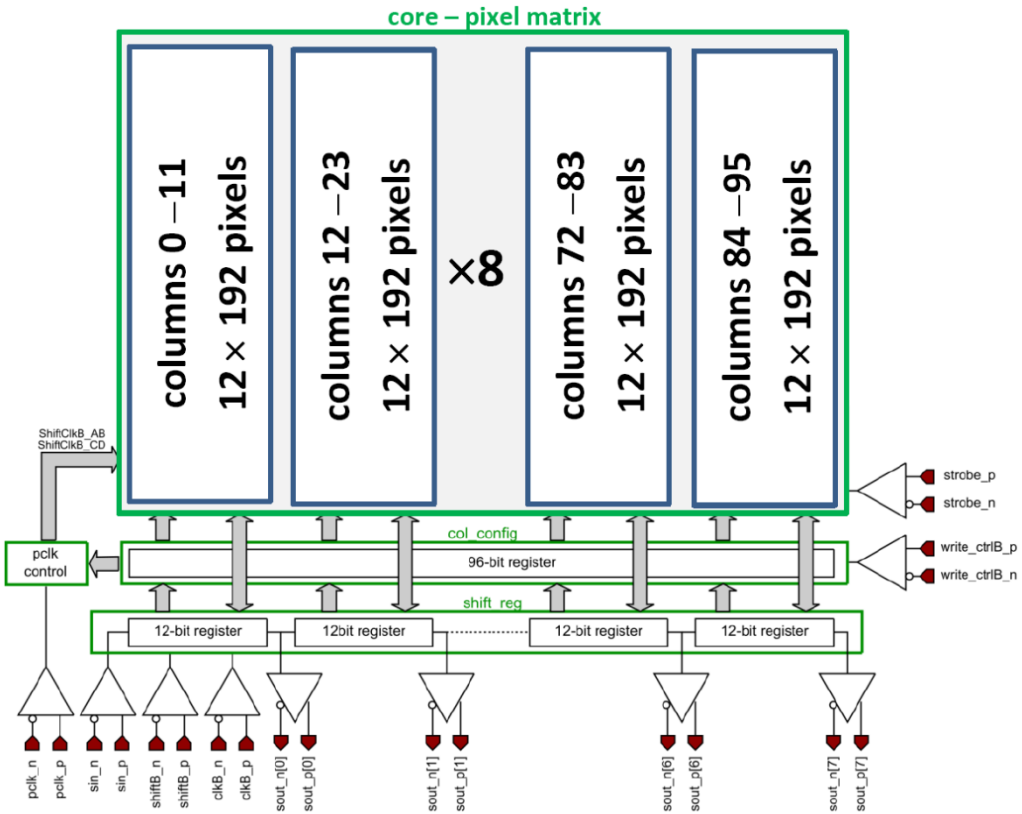



Simplified scheme of a single pixel
(in red the interpixel communication are marked)




Layout of a single pixel of 100 × 100 μm$^2$: 1 – CSA and SHAPER , 2 TH_SET, DISCR and TRIM DAC 3 - references for bias currents, 5 - TH_SET, TRIM_DAC, DISCR, 4 – counters and registers, 5 – logic for charge sharing correction, 6 – interpixel communication channels

# Control of MPIX chip

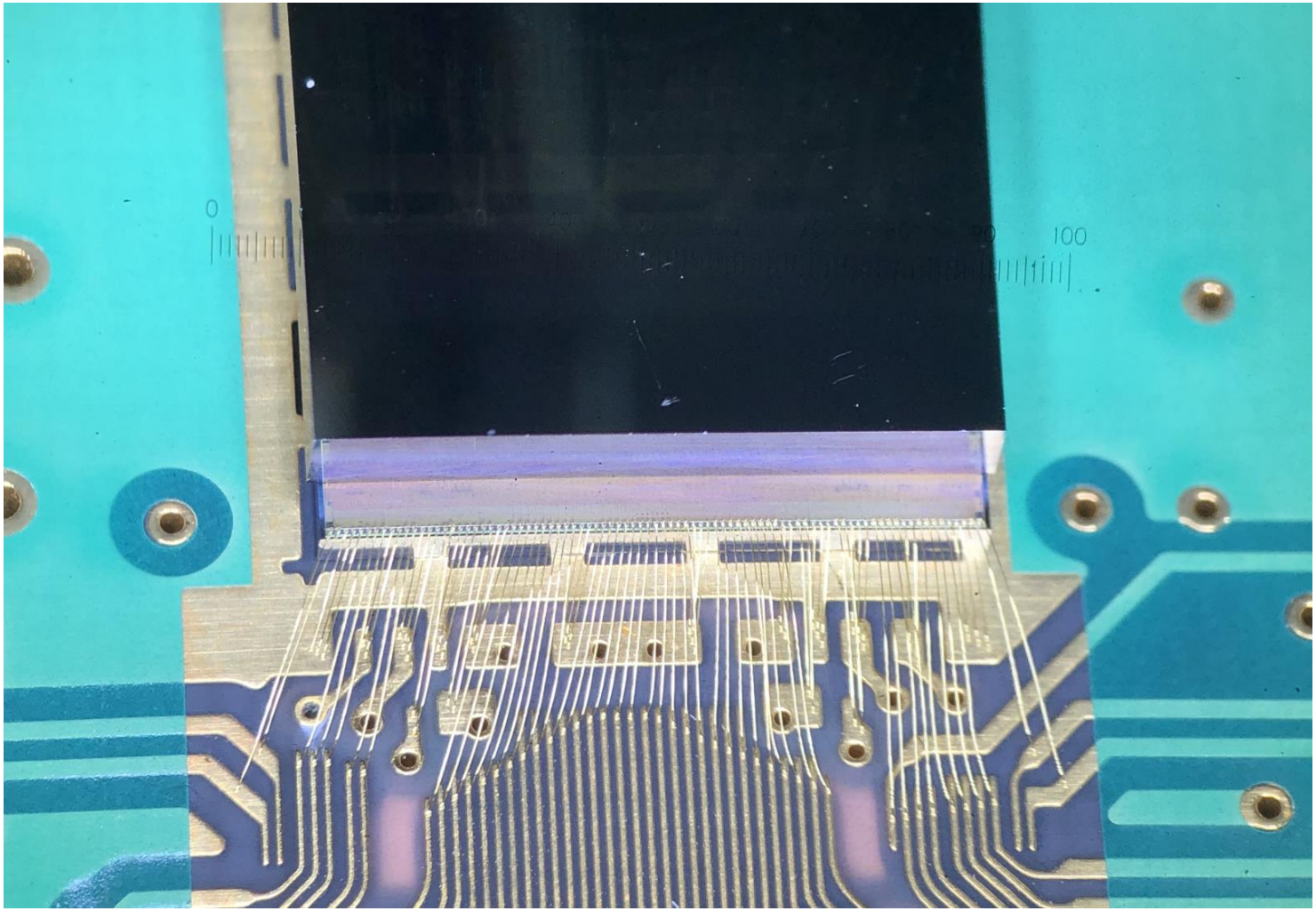



From the top-level readout point of view, **each column is two 1-bit wide shift registers**. The columns are grouped in the blocks of **12 columns** (see Fig). Each block of 12 columns uses 12-bit register to send the data to the LVDS driver, e.g. columns px[11] – px[0] send the data to sout<0> driver, etc. The data from Counter_AB shift register and Counter_CD shift register are multiplexed at the 12-bit register input.

The global control signals of pixel matrix are stored in the 96-bit control register. The control data is first serially loaded into the 96-bit peripheral shift register (shift_reg, MSB first), and then copied into the 96-bit configuration register (col_config).

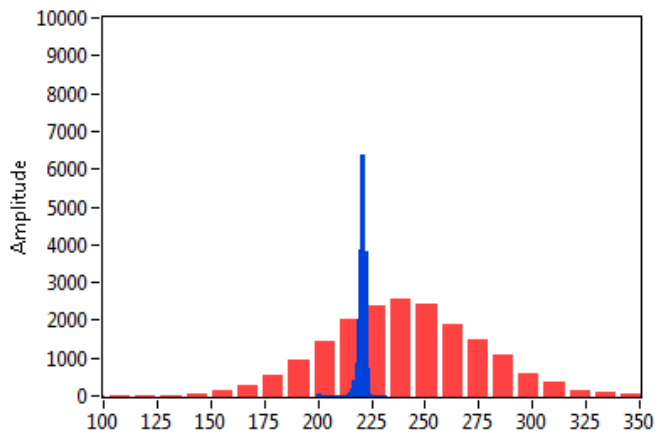
# Bump-bonding of MPIX chip

MPIX chips are bump-bonded to 0.75 mm and 1.5 mm thick CdTe detector

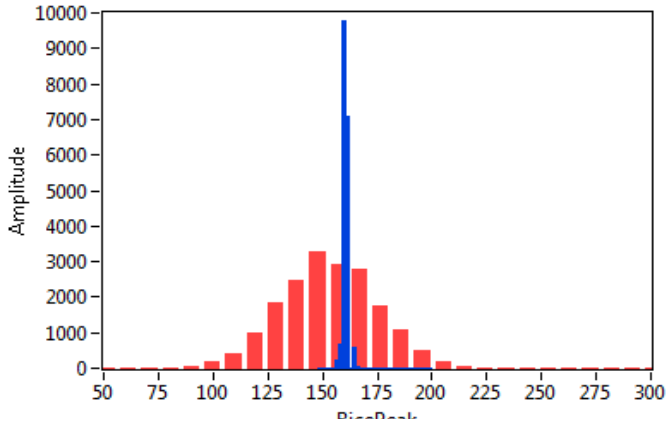


# MPIX – offset before and after correction

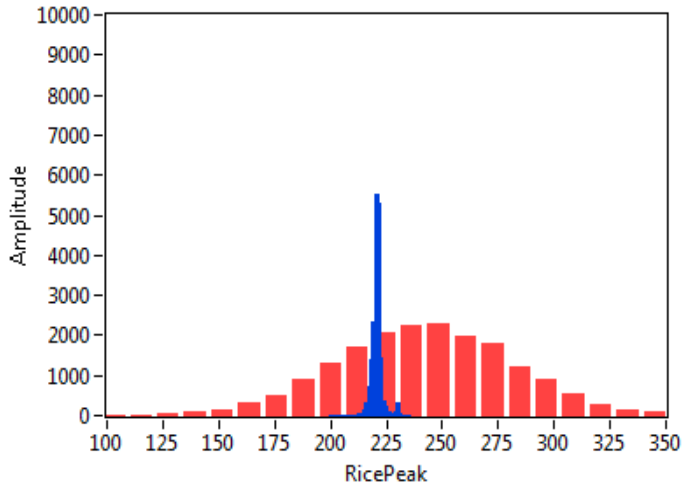
VT0



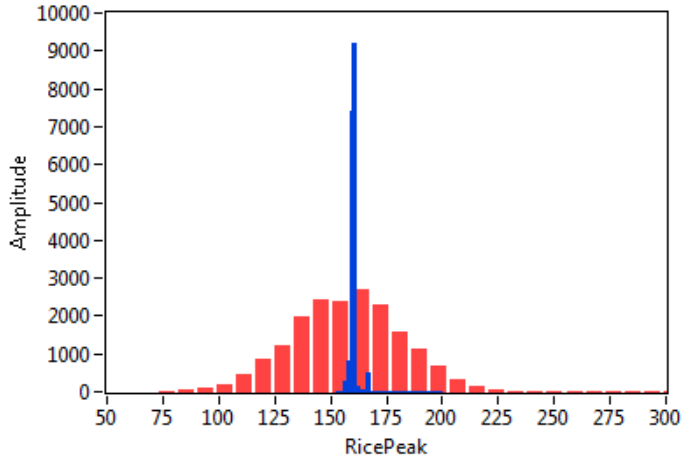

VT2




VT1

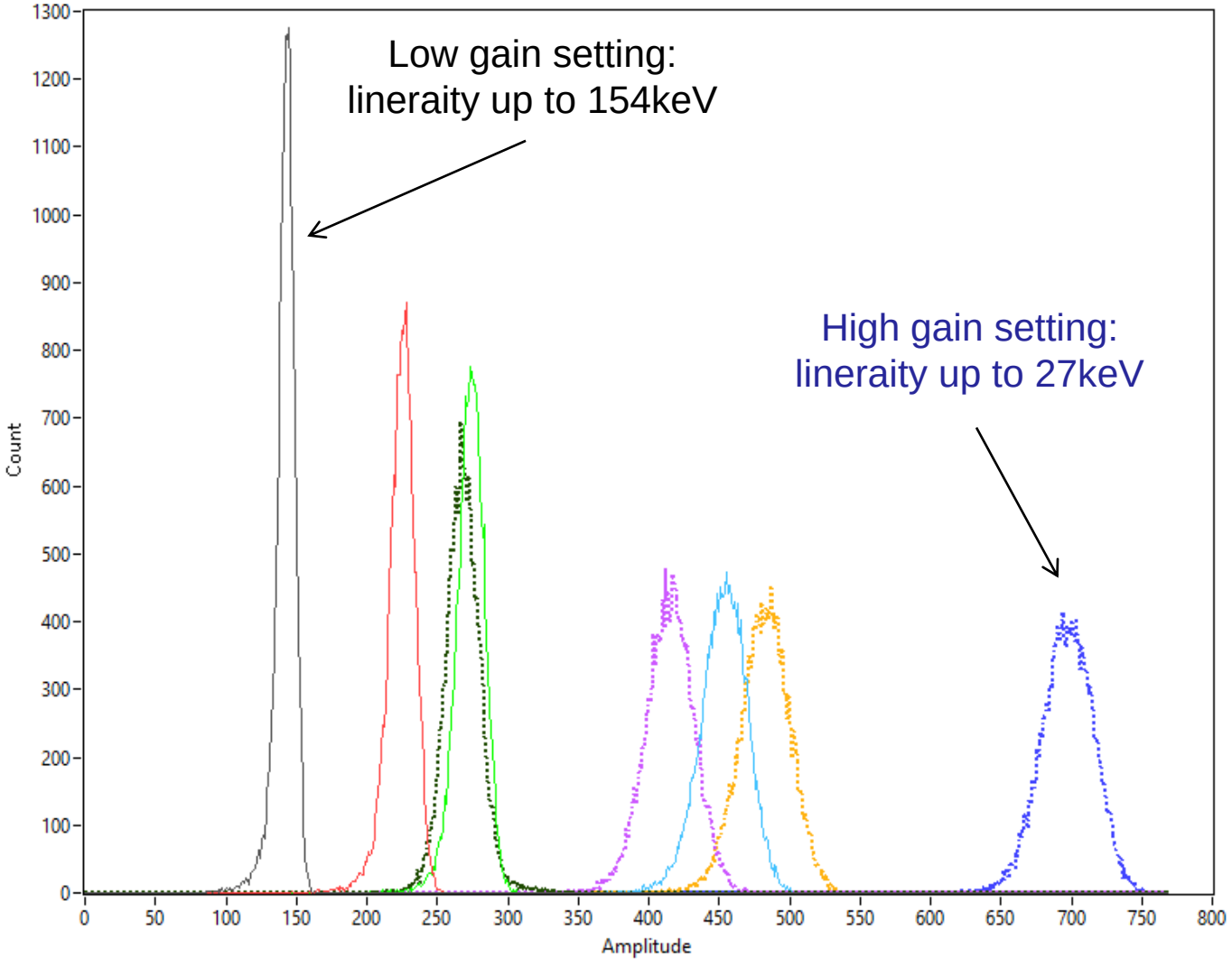



VT3

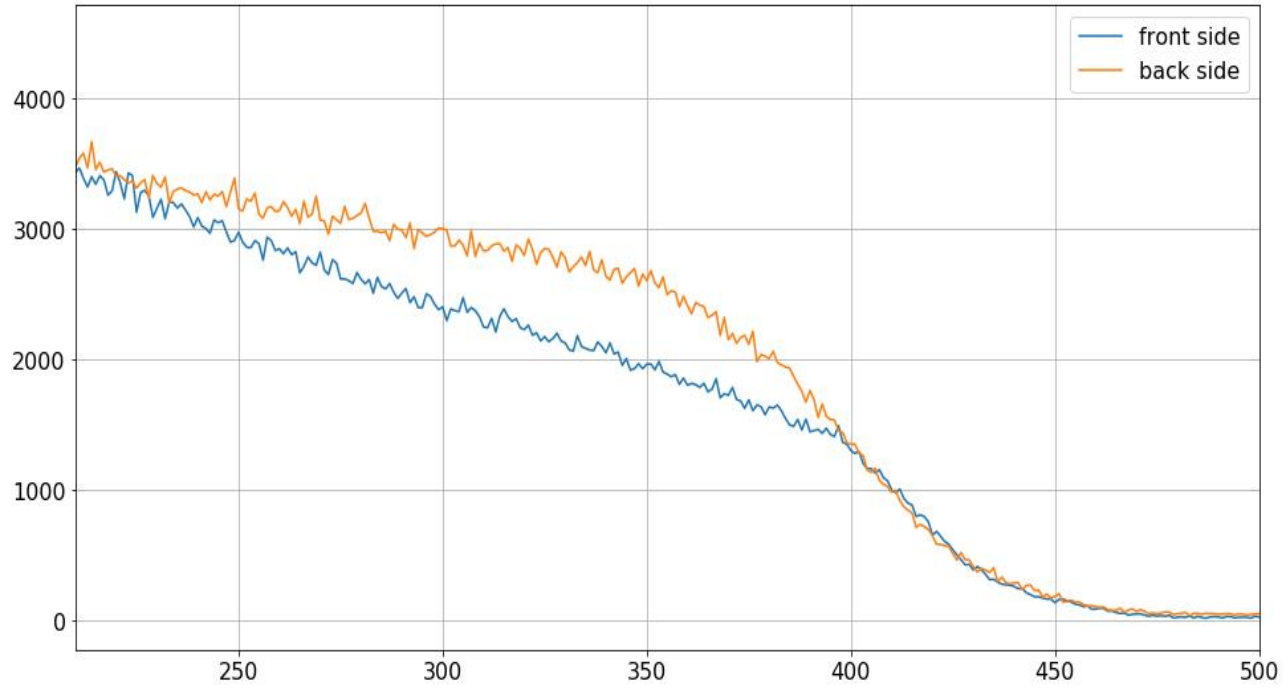



| | | | | | |
|---|---|---|---|---|---|
| VT0 | st dev before correction | 34.82 DAC | → | after correction | 1.83 DAC |
| VT1 | st dev before correction | 39.04 DAC | → | after correction | 2.48 DAC |
| VT2 | st dev before correction | 22.14 DAC | → | after correction | 1.41 DAC |
| VT3 | st dev before correction | 24.25 DAC | → | after correction | 1.51 DAC |

# Gain control and low gain spread from pixel to pixel

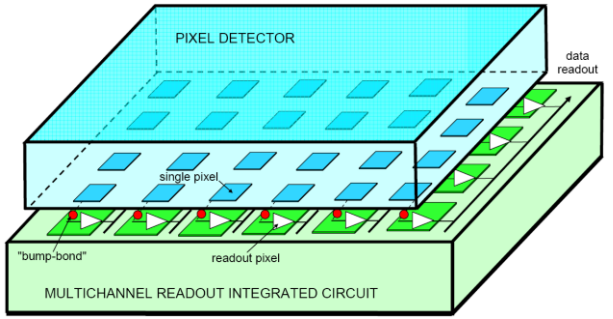


# MPIX – measurements with X-rays: Ag – 22.2 keV
(detector CdTe: thickness 0.75 mm)




Number of count are rescaled
(X-ray absorption in the readout chip)

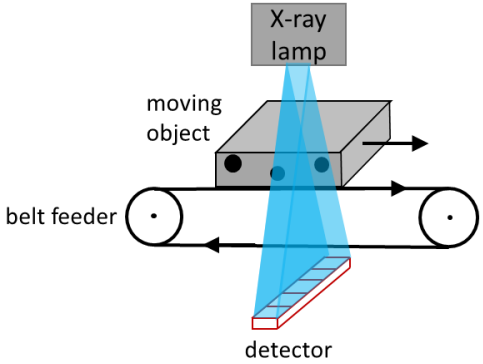
front-side

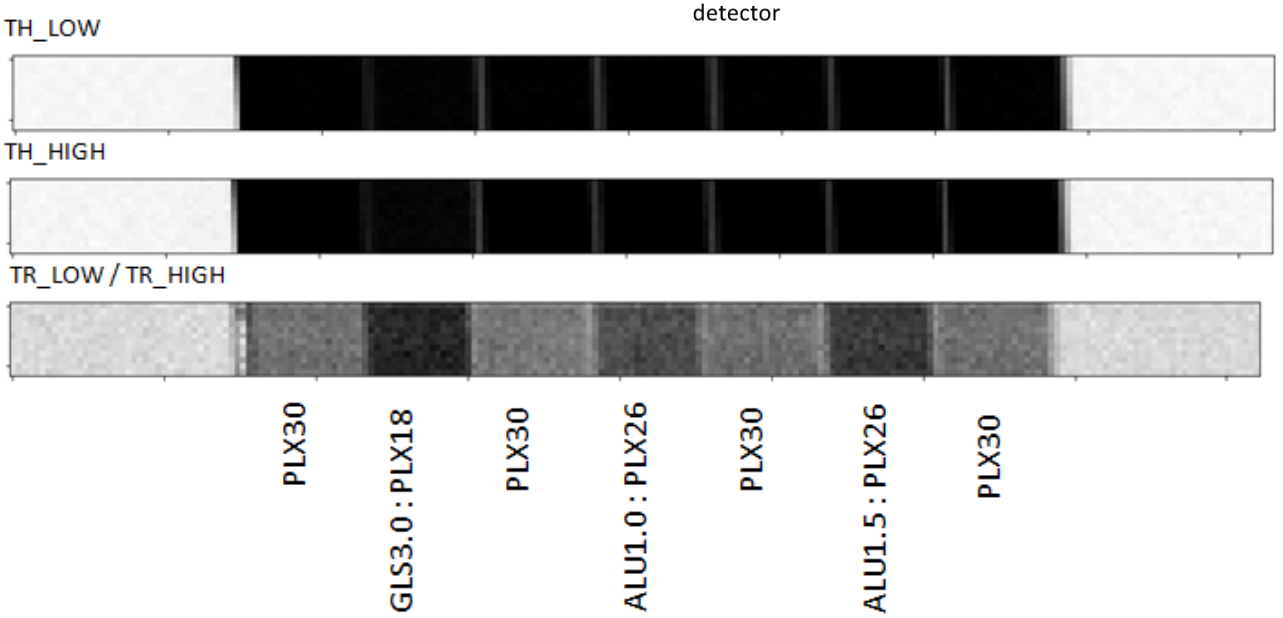



back-side

# MPIX – using two thresholds ($TH_{low}$ =14 keV, $T_{Hhigh}$= 38 keV)
## Time Domain Integration (TDI) on chip

Fantom : moving object – TDI on chip




| |
|---|
| PLX30 |
| PLX18 + GLS3.0 |
| PLX30 |
| PLX26 + ALU1.0 |
| PLX30 |
| PLX26 + GLS1.5 |
| PLX30 |

*More details – see:*
*X-ray imaging of moving objects using on-chip TDI and MDX methods with single photon counting CdTe hybrid pixel detector*
*M. Zoladz, P. Grybos, R. Szczygiel,*
*IWORID 2021, Tue 29/6, time: 4:00 pm*

# MPIX single photon counting mode - summary

**MPIX IC – summary:**

- CMOS 130 nm process
- area of 9.6 mm × 20.3 mm,
- pixel matrix of 96 × 192 with 100 µm pitch,
- pixel : analog front-end & 4 discriminators with 12-bit ripple counters,
- hole and electron collection, leakage current compensation,
- 8 possible different gain settings,
- high gain mode – linear up to 27 keV (CdTe), ENC = 124 el. rms (T=8°C),
- low gain mode – linear up to 154 keV (CdTe), ENC = 192 el. rms (T=8°C)
- uniformity: offset spread of 1 mV rms, gain spread is less than 2 %,
- power consumption per pixel is 80 µW/pixel,
- count-rate –> not measured yet
- interpixel communication – see next slides

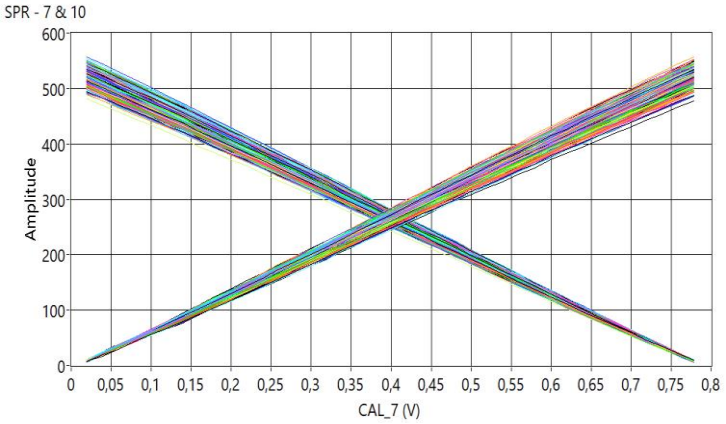
# Testing of algorithm implemented in the chip:
# interpixel communication

# Charge summing between pixels – analog domain
## (with the calibration pulses)

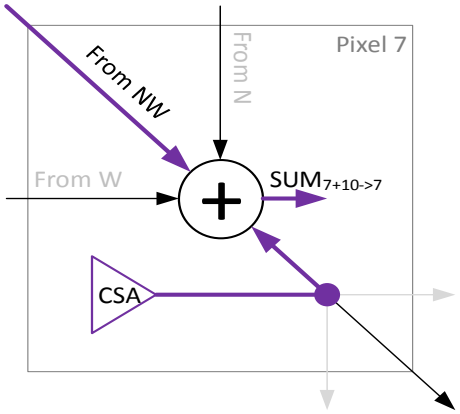
The pixel matrix was divided into group 4x4 pixels

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | 3 | 4 | 1 | 2 | 3 | 4 | |
| | 16 | **13** | **14** | **15** | **16** | 13 | |
| | 12 | **9** | **10** | **11** | **12** | 9 | |
| | 8 | **5** | **6** | **7** | **8** | 5 | |
| | 4 | **1** | **2** | **3** | **4** | 1 | |
| | 13 | 14 | 15 | 16 | 13 | 14 | |
| | | | | | | | |

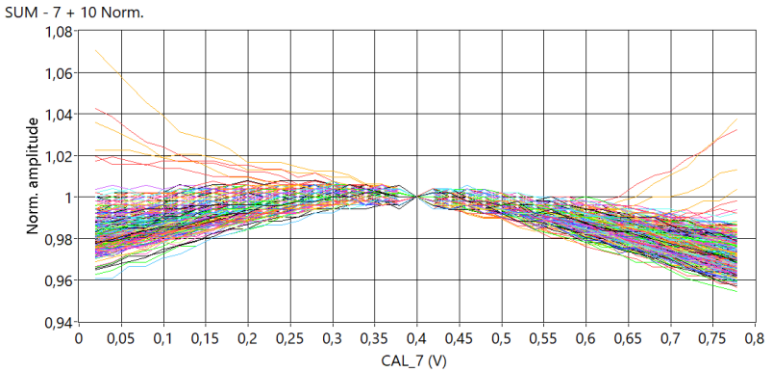
The amplitude of the pulses is change, but the sum is constant



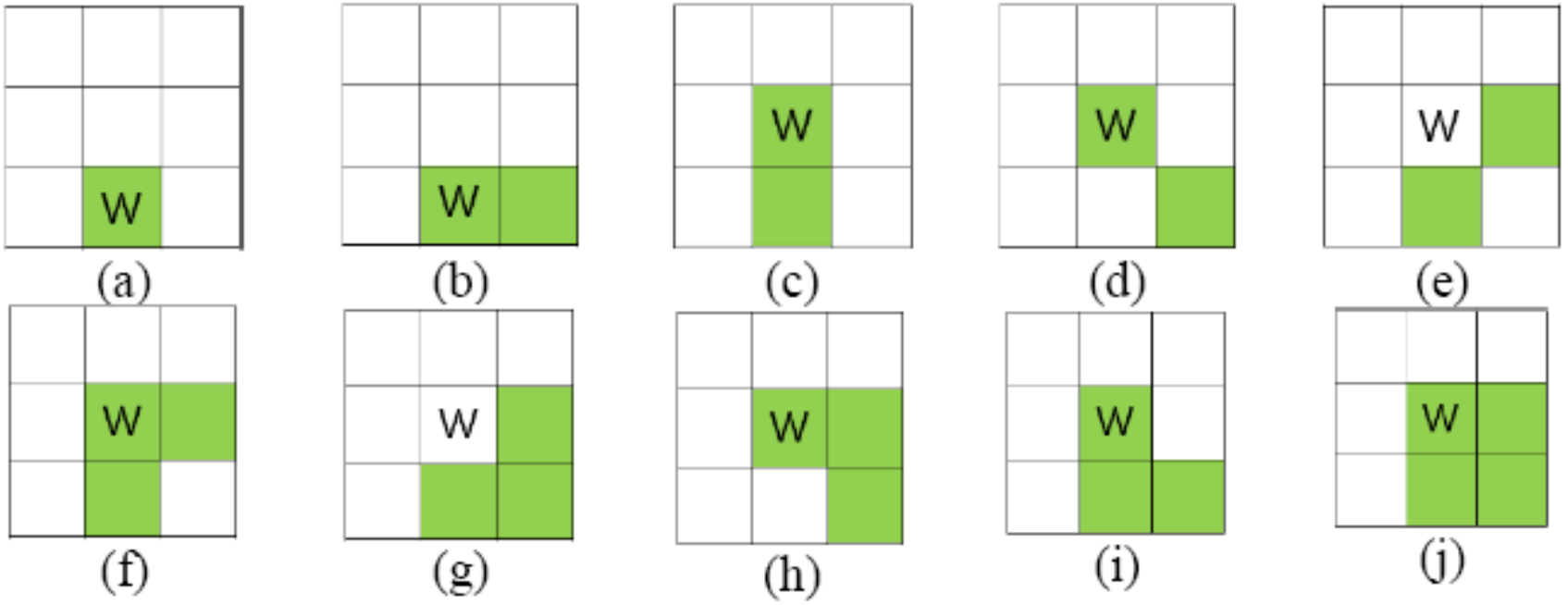

In each group the pulses are injected to 2 nieghbor pixels




The measured sum of two injected pulses

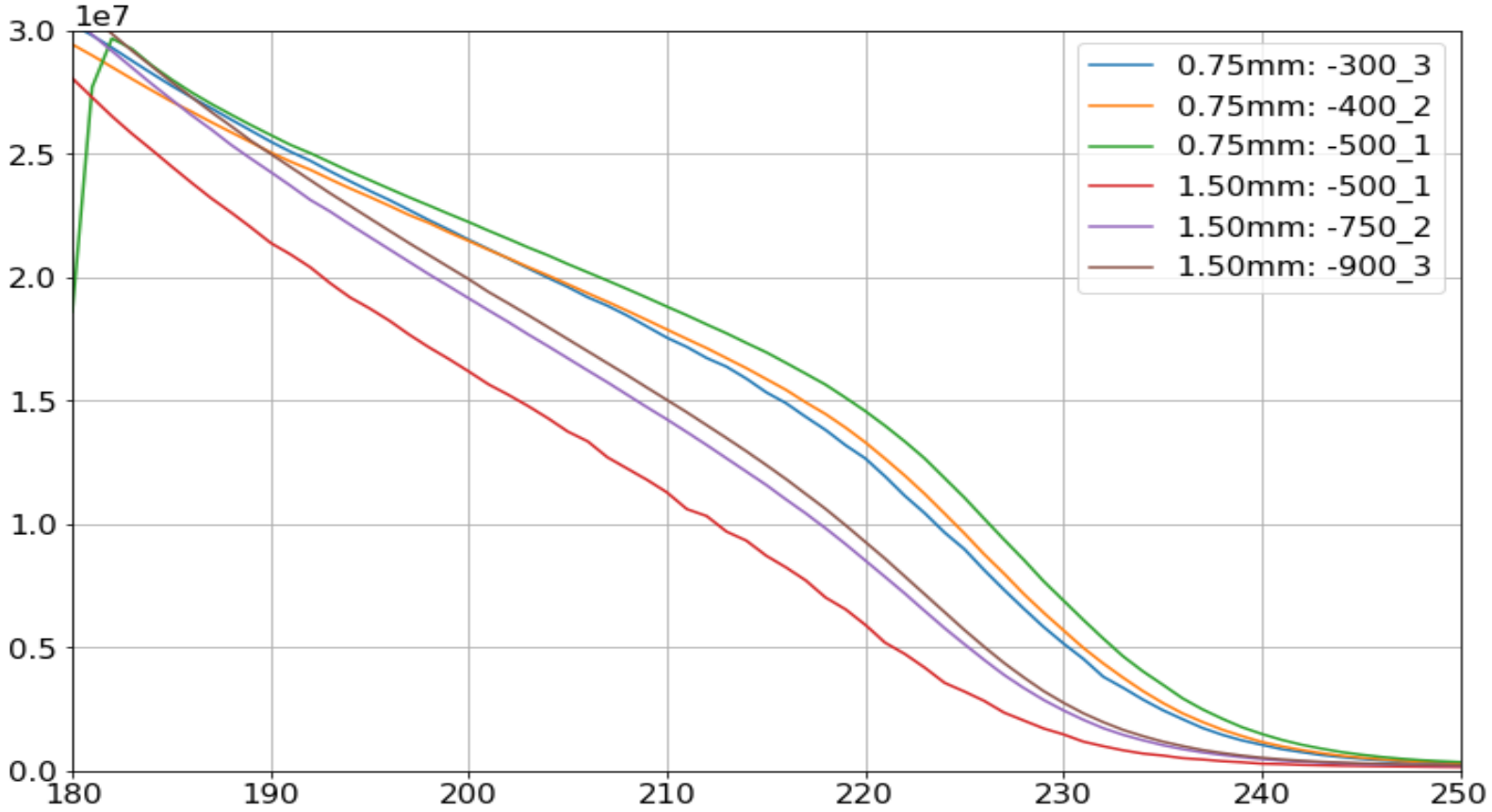


# Allocation (digital pulses) – tested patterns

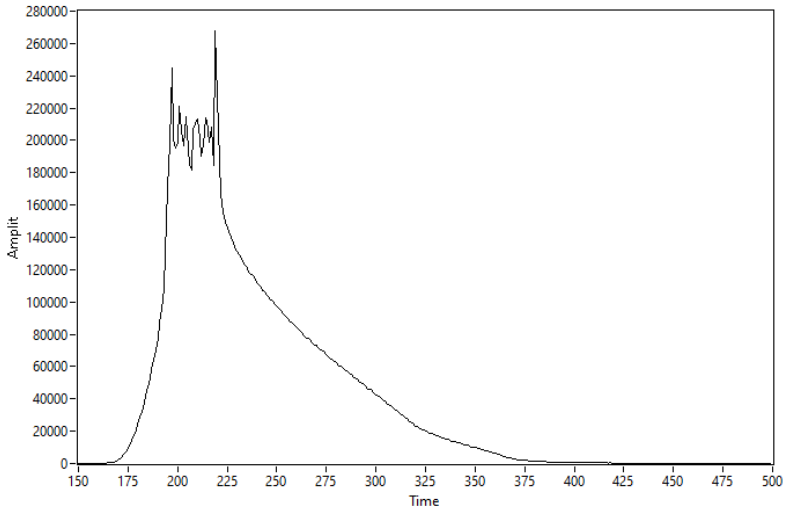


# MPIX – measurements with X-rays – Ag=22.2 keV

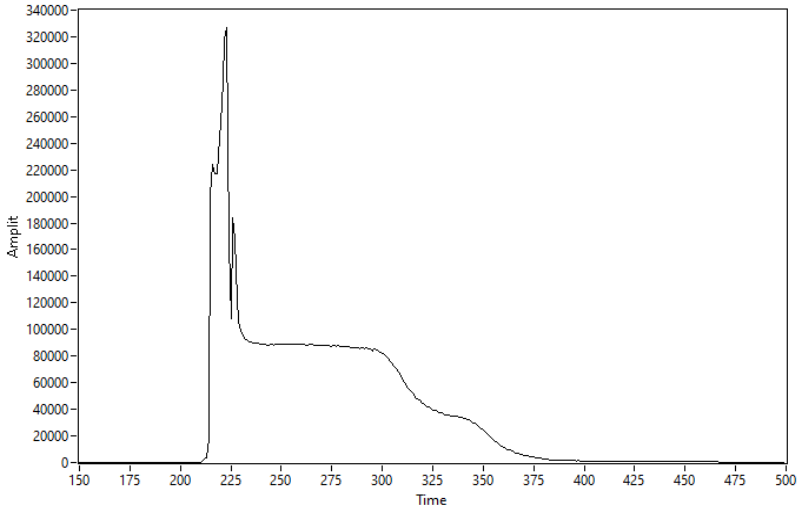
(detector thickness 0.75 mm/1.5 mm)



# MPIX – measurements with X-rays (Ag-22.2 keV, Zr – 15.8keV) (detector thickness 1.5 mm)

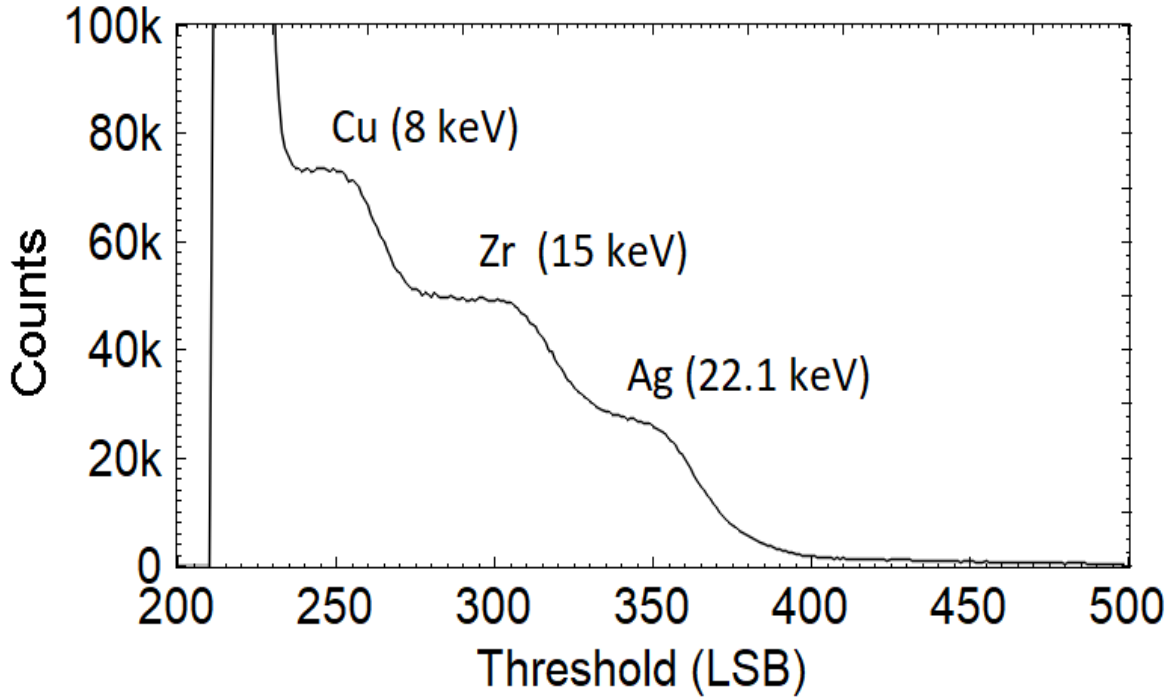



**Standard mode**




**Interpixel communication**

# MPIX – measurements with X-rays – 3 energies (detector thickness 1.5 mm)




Integral spectra of fluorescence samples containg Cu ( 8 keV), Zr (15.7keV) and Ag (22.1keV) measured with MPIX and CdTe 1.5mm-thick sensor biased with -500V.

# Conclusions:

1. MPIX chip is a solution **for high energy X-ray imaging** operating in single photon couting mode: pixel pitch 100 um , CdTe detector, four energy thresholds

2. Algorithm for compensation of charge sharing effect is implemented and preliminary test results of this algorithm are promising.

3. More tests of with bump-bonded detector are still necessary

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