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A 5-Gbps Serializer ASIC in 130 nm for Radiation Readout Environment

The serializer ASIC is used to convert parallel data into a higher bit rate serial data stream, which is widely used in high-speed serial communication systems and becomes one of the key functional modules in the serial data transmission system.This paper presents the design and the test results of a low-power 5Gbps 10:1serializer chip based on standard 130nm CMOS technology.

The chip receives ten channels of 500Mbps parallel data and output one channel of 5Gbps serial data. It is mainly composed of clock Rx, clock divider, parallel data Rx, 5:1module, 2:1module, serial data Tx. The 5:1 module adopts a multiphase structure to convert five channels of 500Mbps parallel data into one channel of 2.5Gbps serial data. The 2:1 module, which follows the two 5:1 modules, receives two channels of 2.5 Gbps data and adopts a tree structure to convert two 2.5Gbps data into one 5Gbps data. The 2:1module has the most restrict requirements on the timing issues of the data and the clock due to its highest data rate within the chip. In order to ensure the timing margin between the data and the clock, a customized multistage LATCH structure is adopted in the 2:1 module. The first stage of the 2:1 module uses a two-path multiple LATCH structure, while the second stage adopts a tree-shaped structure to implement 2:1 serializing. The first path in the front stage is composed of 2 LATCHs, and the second path is composed of 3 LATCHs. Therefore, the phase difference between the two paths (outputs of the first stage)is solely determined by the edge of the clock, instead of any process/temperature dependent buffers. The second stage of the 2:1 module receives two outputs of first stage with fixed phase difference, thus implement the 2:1 serializing safely using tree-shaped structure. An internal parallel PRBS7 source is also added within the chip, and the chip is capable of self-check without external parallel inputs.

The whole serializer ASIC features a size of 1.5mm*1.2mm with 37 pads.The chip has been taped out and a complete logic test has been done. In the self-check mode, a 5 Gbps PRBS 7 serial data has been observed and checked at the output of the ASIC, and the clear widely-open 5 Gbps eye has also been captured on the scope. Both the logic function and analog performance of the ASIC have been verified, and the TID (Total Ionizing Radiation) X-ray radiation test is also planned to be conducted in May. All related test results will be included in the report.

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