Trento Institute for
Fundamental Physics
and Applications

ARCADIA

Advanced **R**eadout **C**MOS **A**rchitectures with **D**epleted **I**ntegrated sensor **A**rrays

Impact of X-ray induced radiation damage on FD-MAPS of the ARCADIA project

T. Corradino, S. Matiazzo, Coralie Neubüser, L. Pancheri
on behalf of the ARCADIA collaboration

01/07/2021

22nd International Workshop on Radiation Imaging Detectors

ARCADIA sensor

design based on SEED project

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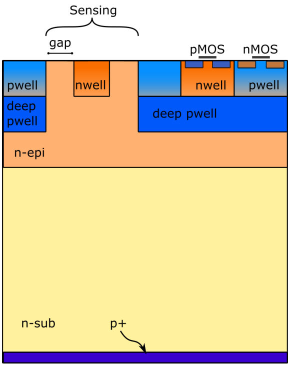


- 110 nm CMOS process with 1.2 V transistors, developed in collaboration between INFN and LFoundry
- fully depleted, charge collection by drift
- backside processing (diode+GR on back)
- low resistivity epi-layer for delayed on-set of punch-through currents

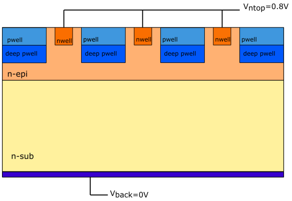
→ first realized in SEED project in 100 - 300 μm ($<$ 100 μm n-substrate in epi, bias from front)
→ first Si of ARCADIA engineering run just arrived

targeted applications:

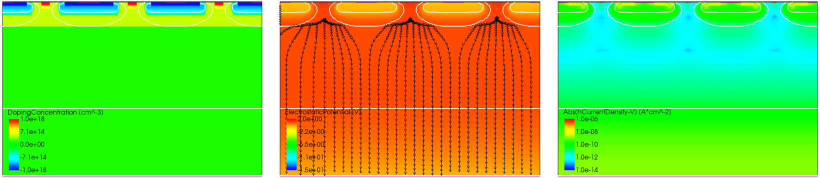
- medical scanners – high rates 10-100 MHz/cm^2
- future lepton colliders – fast charge collection/large area
- space applications – low power consumption 5-20 mW/cm^2

ARCADIA sensor – Operation

2D TCAD simulation of 3 'standard' 25μm pitch pixels, 50μm thickness



- $V_{ntop} = 0.8$V, starts depletion from back side



Values of $V_{dpl}/V_{pt}/V_{pw}$ determined from I-V curves.

ARCADIA sensor – Operation

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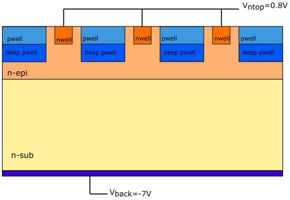
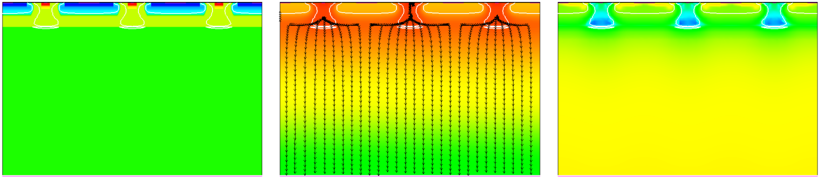


- $V_{ntop} = 0.8$V, starts depletion from back side
- $V_{dpl} = -7$V, epi-layer not fully-depleted but single collection electrodes electrically isolated



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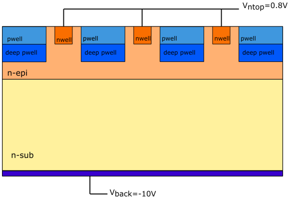

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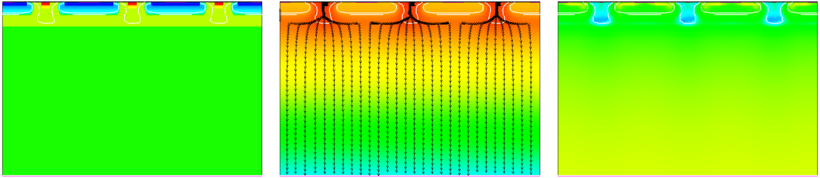

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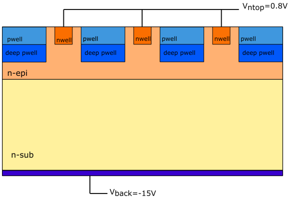

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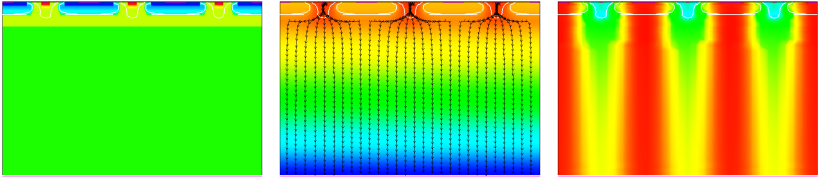
- $V_{pw} = -15.5$V, maximum power consumption 0.1 mW/cm^2



Values of $V_{dpl}/V_{pt}/V_{pw}$ determined from I-V curves.

SEED Pseudo-Matrices (PMs)

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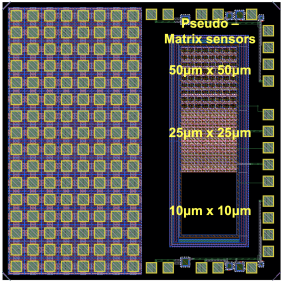
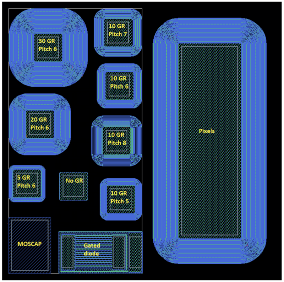
frontside



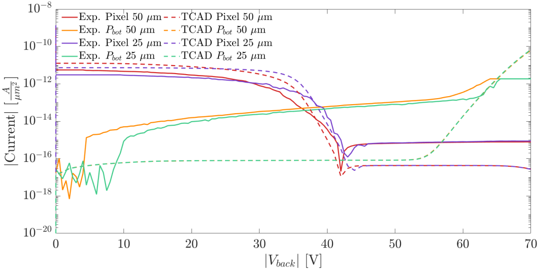
backside

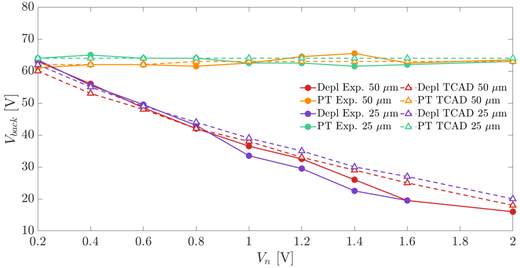


- pixels short-circuited per different pixel pitch matrix:
  - 8×9 pixels of 50μm pitch
  - 16×18 pixels of 25μm pitch
  - 40×45 pixels of 10μm pitch
- tests in micro-beam of 2MeV p^+ in Zagreb
  doi:10.1109/TED.2020.2985639, doi:10.1088/1748-0221/14/06/C06016

SEED Pseudo-Matrices (PMs)

100μm thick substrate





Thomas Corradino, Università Trento
see also: T.Corradino et al. "Design and Characterization of Backside Termination Structures for Thick Fully-Depleted MAPS", Sensors 2021, 21(11), 3809

SEED results on MATISSE chip

Monolithic AcTIve pixel SenSor Electronics

doi:10.1109/NSSMIC.2017.8532806

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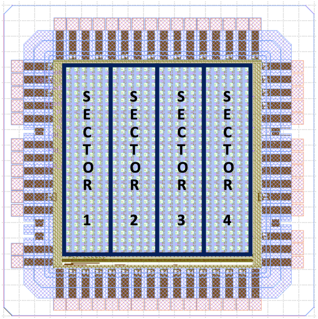
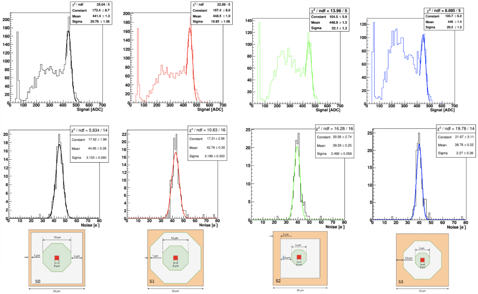


- 24 × 24 active pixel array
- $(50 \times 50)\mu m^2$ pixels
- part. integrated electronics (analog and digital in-pixel)
- 4 sectors read out in parallel
- analog gain 130 mV/fC (2.1 mV/100 e^-)

- scan with ^{55}Fe, 300μm thick at $V_{back} = 200$ V ($V_{dpl} = 100$ V), clustering applied with SNR$\sim$6
- clock frequency 3.125 MHz, 12.8 μs integration time



- different sensing diode designs, possibility to exploit for investigations of surface damage...

Serena Mattiazzo, Padova

X-ray induced radiation damage

gamma rays < 300 keV only penetrate surface

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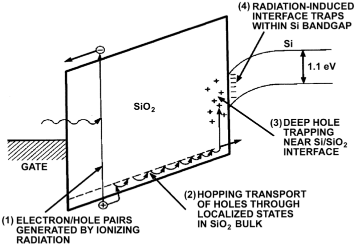
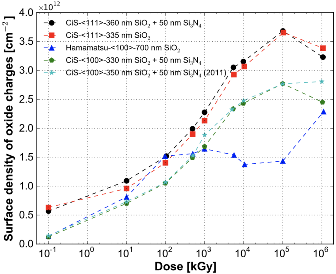
Mechanism of oxide charge and trap creation:

1. ionising radiation creates e/h pairs in the SiO_2 (passivation layer)
2. some charge carriers recombine, others drift according to electric field to electrode or Si-SiO_2 interface
3. holes move slowly towards Si-SiO_2 interface ("polaron hopping") and get trapped by oxygen vacancies to form so-called oxide charges (N_{ox})
4. interface traps (donor/acceptor states in Si)

→ oxide charge concentration of SiO_2 possible to measure with MOS capacitors/gated diodes



T.R. Oldham et al., "Total ionizing dose effects in MOS oxides and devices" (2013), doi:10.1109/TNS.2003.812927

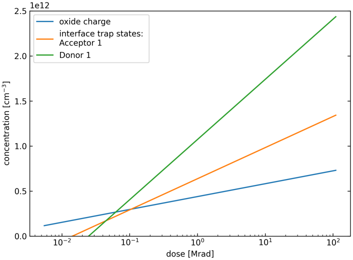


J. Zhang et al., "Investigation of X-ray induced radiation damage at the Si-SiO2 interface of silicon sensors for the European XFEL", 2012 JINST 7 C12012

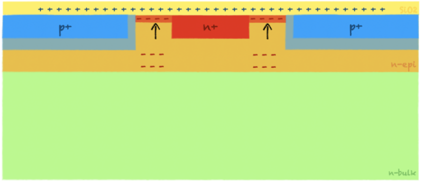
Modelling of surface damage in TCAD

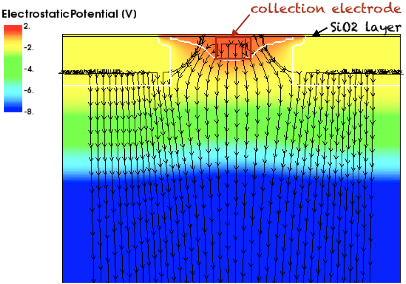
following New Perugia model: *AIDA2020 report*

- included positive oxide charge, and 1 acceptor + 1 donor trap
- parametrized on p-type Si from different producers



- **oxide charge $6.5 \cdot 10^{10}$ cm^{-3} at dose=0**
- accumulation layer of negative charges below the SiO_2





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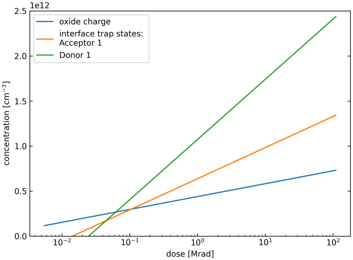
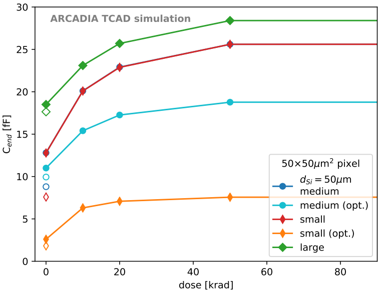


simulation studies suggest:

- smaller electrode alone not effective in capacitance reduction
- reduction of 'free' gap between electrode and pwells preferred to reduce impact of positive charges



C. Neubüser et al., "Sensor design optimization of innovative low-power, large area MAPS for HEP and applied science" submitted to Frontiers in Physics, arXiv:2011.09723

→ validation in data..

Variation of MATISSE pixels

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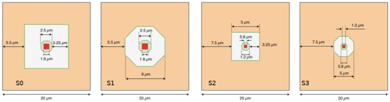
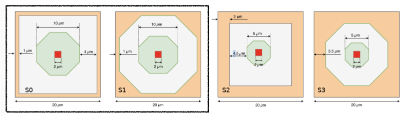
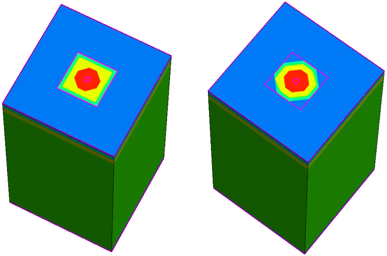
100 μm



300 μm





- in total 8 different pixel geometries
- after different TIDs difference found in noise level of the sectors $\rightarrow$ compare with prediction in simulations using our 2-trap + positive oxide charge model
- 2 types of TCAD domains: octagonal/square pwells

irradiation study performed with:

- X-ray tube with Tungsten anode
- peak photon energy of 10 keV
- 2 Mrad/h at room temperature

Comparison of simulations with data

simplified Equivalent Noise Charge (ENC) estimation

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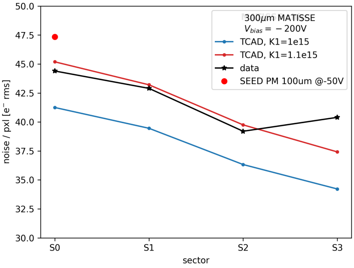
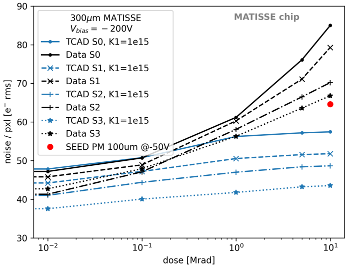
MATISSE signal from switched integrator with Correlated Double Sampling

$$ENC^2 = ((C_{in} + C_d) \cdot K1)^2 + \left(\sqrt{I_{leak} * t_{int}/q_e}\right)^2 \qquad (1)$$





- relation of increased capacitance/noise with 'free' area between electrode and pwell validated, especially for higher doses
- 10% difference in K1 translates directly in 10%
- surface damage model (+ I_{leak} of few pA) does not describe the large noise increase $\leq 1\,$Mrad
- damage of transistors? MOSFETs currently under test in INFN Pavia

Capacitances of SEED PMs and comparison to simulations

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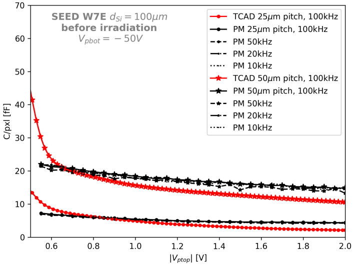
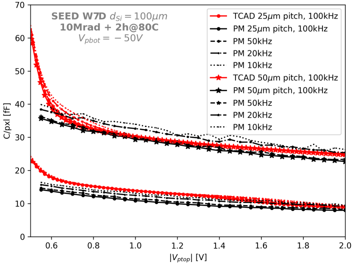
- at fixed backside voltage ($V_{dpl} < V_{pbot} \leq V_{pt}$)
- voltage sweep of pwell bias – increase of epi layer depletion
- parasitic capacitances neglected
- good agreement of data/simulation at operating voltage 0.8 V
- data limited by measurement accuracy
- reproduce the capacitance behavior with frequency





First look at ARCADIA engineering run

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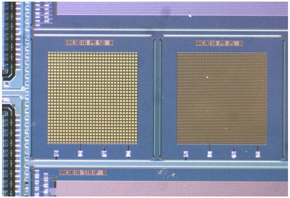
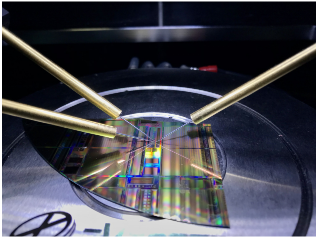
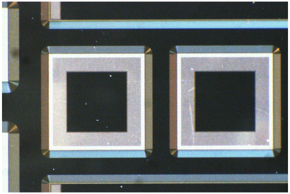
large set of test-structures, here $1.5 \times 1.5\,\mathrm{mm}^2$ Pseudo-Matrices

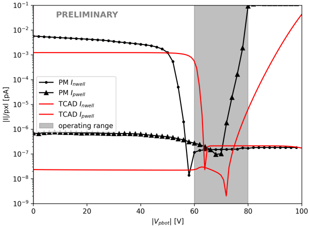
frontside





backside





- operating range limited by high currents, damaged surrounding structures
- predictions of depletion from simulations not yet match data, improvement after dicing expected

First look at ARCADIA engineering run

large set of test-structures, here 1.5 × 1.5 mm² Pseudo-Matrices

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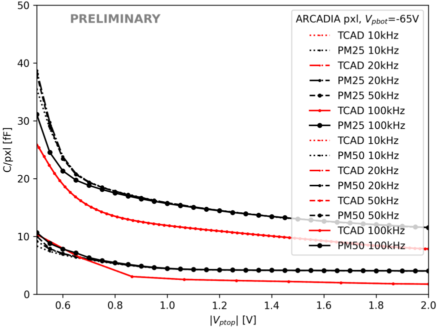

- simulation predicts lower capacitance, but could be effected by contact issues on backside

- multi-dimensional parameter space in simulations to be matched to data
- test-structures include pad diodes, and MOS capacitors → allows for doping profile per wafer, oxide charge measurements

Conclusions

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- ARCADIA sensor technology successfully tested in previous runs
- surface damage non-negligible impact on pixel capacitances
- model prediction in ~10% agreement with measurements passive matrices
- MATISSE chip with integrated electronics shows excess noise after 10Mrad, not explainable by capacitance increase of sensor
- first look at Si of the ARCADIA engineering shows functional matrices, however final results have to be acquired from singulated structures

Outlook

- systematic study of PMs and other test-structures on all thicknesses and pixel flavors planned this summer

Other activities

- DAQ for ARCADIA Main Demonstrator chip $(1.3 \times 1.3)\,\text{cm}^2$ ready
- telescope of 6 ARCADIA MD chips planned for cosmics and possibly testbeam in autumn
- 2nd engineering run on the way.. include a specialized test chip for timing (ALICE3 TOF layer), new sensor designs and electronics

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THANK YOU FOR YOUR ATTENTION!

ARCADIA collaboration

INFN - Bologna, Milano, Padova, Perugia, Pavia, TIFPA, Torino

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Many thanks!

F. Alfonsi, G. Ambrosi, A. Andreazza, E. Bianco, G. Balbi, S. Beolè, M. Caccia, A. Candelori, D. Chiappara, **Thomas Corradino**, T. Croci, M. Da Rocha Rolo, G. F. Dalla Betta, A. De Angelis, G. Dellacasa, N. Demaria, L. De Cilladi, B. Di Ruzza, A. Di Salvo, D. Falchieri, M. Favaro, A. Gabrielli, L. Gaioni, S. Garbolino, G. Gebbia, R. Giampaolo, N. Giangiacomi , P. Giubilato, R. Iuppa, M. Mandurrino, M. Manghisoni, **Serena Mattiazzo**, F. Nozzoli, J. Olave, **Lucio Pancheri**, D. Passeri, A. Paternò, M. Pezzoli, P. Placidi, L. Ratti, E. Ricci, S. B. Ricciarini, A. Rivetti, H. Roghieh, R. Santoro, A. Scorzoni, L. Servoli, F. Tosello, G. Traversi, C. Vacchi, R. Wheadon, J. Wyss, M. Zarghami, P. Zuccon

BACKUP

ARCADIA MD1 – specs

trigger-less, and binary readout

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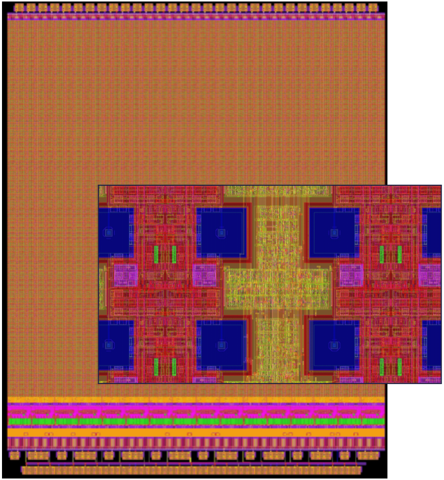
- matrix core 512 × 512 pxls of 25 μm pitch
- pixels are ∼(50/50)% analog/digital
- sensor diode about 20% of total area
- clock-less matrix (to minimize power dissipation)
- pixel regions propagate the output data to the periphery



Manuel Rolo, INFN Torino