Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

Impact of X-ray induced radiation damage on FD-MAPS of the ARCADIA project

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ARCADIA sensor
design based on SEED project

- 110 nm CMOS process with 1.2 V transistors, developed in collaboration between INFN and LFoundry
- fully depleted, charge collection by drift
- backside processing (diode+GR on back)
- low resistivity epi-layer for delayed on-set of punch-through currents
  → first realized in SEED project in 100 - 300 µm (< 100 µm n-substrate in epi, bias from front)
  → first Si of ARCADIA engineering run just arrived

targeted applications:
- medical scanners – high rates 10-100 MHz/cm²
- future lepton colliders – fast charge collection/large area
- space applications – low power consumption 5-20 mW/cm²
2D TCAD simulation of 3 'standard' 25 µm pitch pixels, 50 µm thickness

\[ V_{\text{ntop}} = 0.8 \text{V}, \text{ starts depletion from back side} \]

Values of \( V_{dpl}/V_{pt}/V_{pw} \) determined from I-V curves.
**ARCADIA sensor – Operation**

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- $V_{dpl} = -7$V, epi-layer not fully-depleted but single collection electrodes electrically isolated

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- $V_{pt} = -11V$, on-set of punch-through between pwell and $p^+$ back
- $V_{pw} = -15.5V$, maximum power consumption 0.1 mW/cm$^2$

Values of $V_{dpl}/V_{pt}/V_{pw}$ determined from I-V curves.
pixels short-circuited per different pixel pitch matrix:

- 8 × 9 pixels of 50\(\mu\)m pitch
- 16 × 18 pixels of 25\(\mu\)m pitch
- 40 × 45 pixels of 10\(\mu\)m pitch

tests in micro-beam of 2MeV \(p^+\) in Zagreb

doi:10.1109/TED.2020.2985639,
doi:10.1088/1748-0221/14/06/C06016
SEED Pseudo-Matrices (PMs)

100µm thick substrate

Thomas Corradino, Università Trento
see also: T. Corradino et al. "Design and Characterization of Backside Termination Structures for Thick Fully-Depleted MAPS", Sensors 2021, 21(11), 3809
SEED results on MATISSE chip

Monolithic AcTIve pixel SenSor Electronics
doi:10.1109/NSSMIC.2017.8532806

- 24 × 24 active pixel array
- (50 × 50)µm² pixels
- part. integrated electronics (analog and digital in-pixel)
- 4 sectors read out in parallel
- analog gain 130 mV/fC (2.1 mV/100 e⁻)

- scan with $^{55}$Fe, 300µm thick at $V_{\text{back}} = 200$ V ($V_{dpl} = 100$ V), clustering applied with SNR~6
- clock frequency 3.125 MHz, 12.8 µs integration time

- different sensing diode designs, possibility to exploit for investigations of surface damage...
X-ray induced radiation damage
gamma rays < 300 keV only penetrate surface

Mechanism of oxide charge and trap creation:

1. ionising radiation creates e/h pairs in the SiO₂ (passivation layer)

2. some charge carriers recombine, others drift according to electric field to electrode or Si-SiO₂ interface

3. holes move slowly towards Si-SiO₂ interface ("polaron hopping") and get trapped by oxygen vacancies to form so-called oxide charges ($N_{ox}$)

4. interface traps (donor/acceptor states in Si)

→ oxide charge concentration of SiO₂ possible to measure with MOS capacitors/gated diodes
Modelling of surface damage in TCAD
following New Perugia model: *AIDA2020 report*

- included positive oxide charge, and 1 acceptor + 1 donor trap
- parametrized on p-type Si from different producers

- oxide charge $6.5 \cdot 10^{10}$ cm$^{-3}$ at dose=0
- accumulation layer of negative charges below the SiO$_2$
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Simulation studies suggest:
- smaller electrode alone not effective in capacitance reduction
- reduction of 'free' gap between electrode and pwells preferred to reduce impact of positive charges

→ validation in data.
Variation of MATISSE pixels

100 µm

- in total 8 different pixel geometries
- after different TIDs difference found in noise level of the sectors → compare with prediction in simulations using our 2-trap + positive oxide charge model

300 µm

- 2 types of TCAD domains: octagonal/square pwells

irradiation study performed with:
- X-ray tube with Tungsten anode
- peak photon energy of 10 keV
- 2 Mrad/h at room temperature
Comparison of simulations with data
simplified Equivalent Noise Charge (ENC) estimation

MATISSE signal from switched integrator with Correlated Double Sampling

\[
ENC^2 = ((C_{in} + C_d) \cdot K1)^2 + \left( \sqrt{I_{\text{leak}} \cdot t_{\text{int}}/q_e} \right)^2
\]

- relation of increased capacitance/noise with 'free' area between electrode and pwell validated, especially for higher doses
- 10% difference in \( K1 \) translates directly in 10%
- surface damage model (+ \( I_{\text{leak}} \) of few pA) does not describe the large noise increase \( \leq 1 \text{ Mrad} \)
- damage of transistors? MOSFETs currently under test in INFN Pavia
Capacitances of SEED PMs and comparison to simulations

- at fixed backside voltage \((V_{dpl} < V_{pbot} \leq V_{pt})\)
- voltage sweep of pwell bias – increase of epi layer depletion
- parasitic capacitances neglected
- good agreement of data/simulation at operating voltage 0.8 V
- data limited by measurement accuracy
- reproduce the capacitance behavior with frequency
First look at ARCADIA engineering run

large set of test-structures, here $1.5 \times 1.5 \text{mm}^2$ Pseudo-Matrices

frontside

Backside

- operating range limited by high currents, damaged surrounding structures
- predictions of depletion from simulations not yet match data, improvement after dicing expected
First look at ARCADIA engineering run

large set of test-structures, here $1.5 \times 1.5 \text{mm}^2$ Pseudo-Matrices

- simulation predicts lower capacitance, but could be effected by contact issues on backside

- multi-dimensional parameter space in simulations to be matched to data

- test-structures include pad diodes, and MOS capacitors $\rightarrow$ allows for doping profile per wafer, oxide charge measurements
Conclusions

- ARCADIA sensor technology successfully tested in previous runs
- surface damage non-negligible impact on pixel capacitances
- model prediction in $\sim 10\%$ agreement with measurements passive matrices
- MATISSE chip with integrated electronics shows excess noise after 10Mrad, not explainable by capacitance increase of sensor
- first look at Si of the ARCADIA engineering shows functional matrices, however final results have to be acquired from singulated structures

Outlook

- systematic study of PMs and other test-structures on all thicknesses and pixel flavors planned this summer

Other activities

- DAQ for ARCADIA Main Demonstrator chip $(1.3 \times 1.3) \text{ cm}^2$ ready
- telescope of 6 ARCADIA MD chips planned for cosmics and possibly testbeam in autumn
- 2nd engineering run on the way.. include a specialized test chip for timing (ALICE3 TOF layer), new sensor designs and electronics
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THANK YOU FOR YOUR ATTENTION!
Many thanks!

BACKUP
ARCADIA MD1 – specs
trigger-less, and binary readout

▶ matrix core $512 \times 512$ pxis of $25 \mu m$ pitch
▶ pixels are $\sim (50/50)$% analog/digital
▶ sensor diode about 20% of total area
▶ clock-less matrix (to minimize power dissipation)
▶ pixel regions propagate the output data to the periphery

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