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GBTX emulator for development and special versions of GBT-based readout chains

The GBTX ASIC is a standard solution for providing fast control and data readout for radiation detectors used in HEP experiments [1,2]. However, it is subject to export control restrictions due to the usage of radiation-hard technology. To enable the development of GBT-based readout chains in countries, where the original GBTX can't be imported, an FPGA-based GBTX emulator (GBTxEMU) has been developed. Thanks to utilization of slightly modified GBT-FGPA core [3] it maintains basic compatibility with standard GBT-based systems.
The emulator may be implemented in a relatively cheap Artix 7 FPGA chip. It provides the basic functionality of the original GBTX - time-deterministic transport of downlink messages, allowing synchronization and fast control of front-end, and high-speed transmission of hit data in the uplink direction. The GBTxEMU supports limited modes of E-Link operation with a clock frequency of 40 or 80 MHz. The downlink operates with SDR (40 or 80 Mbps) and the uplink with DDR (80 or 160 Mbps). The number of supported E-Links depends on the E-Link clock frequency and is equal to 28 for 80 MHz and 56 for 40 MHz.
The emulator may also be used in special versions of the GBT-based readout chain, where radiation hardness is not essential, but the overall price of the system may be important. Currently, its usage in DAQ systems for BM@N and MPD experiments is planned [4]. The original hardware implementation is based on a commercial Artix-7 module and a dedicated baseboard providing jitter cleaner and communication interfaces. The development version was created at GSI, and the final BM@N version in Eurocard format was designed at JINR. In the applications where the maximum throughput of the GBTxEMU is not needed, the board may be placed at some distance from the on-detector electronics, outside of high magnetic field and radiation enviroment. The 10-meter length copper cable connection between the front-end electronics and GBTxEMU was proven to be stable in the BM@N STS project.
Thanks to the FPGA-based architecture, the GBTxEMU is highly flexible. The end-user may connect his own IP blocks to the internal bus, creating additional control interfaces. A special address space management system [5] facilitates their easy integration with the control software. The internal registers are accessible either via the GBT link or via IPbus (using 100Mbps or 1Gbps Ethernet). The embedded Forth-based CPU may perform complex initialization procedures during power-up, and be used for interactive diagnostics.
The GBTxEMU may be an interesting solution for the development of GBT-based readout chains and for less demanding experiments.

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Primary authors: Dr ZABOŁOTNY, Wojciech (Institute of Electronic Systems, Warsaw University of Technol-

ogy); Mr BYSZUK, Adrian (Institute of Electronic Systems, Warsaw University of Technology); Mr DEMENTEV, Dmitrii (Veksler and Baldin Laboratory of High Energy Physics, Joint Institute for Nuclear Research); Dr EMSCHERMANN, David (GSI-Helmholtzzentrum für Schwerionenforschung GmbH); Mr GUMIŃSKI, Marek (Institute of Electronic Systems, Warsaw University of Technology); Mr KRUSZEWSKI, Michał (Institute of Electronic Systems, Warsaw University of Technology); Mr MIEDZIK, Piotr (Institute of Electronic Systems, Warsaw University of Technology); Prof. POŹNIAK, Krzysztof (Institute of Electronic Systems, Warsaw University of Technology); Prof. ROMANIUK, Ryszard (Institute of Electronic Systems, Warsaw University of Technology); Dr SCHMIDT, Christian (GSI-Helmholtzzentrum für Schwerionenforschung GmbH); Mr SHITENKOV, Mikhail (Veksler and Baldin Laboratory of High Energy Physics, Joint Institute for Nuclear Research)

Presenter: Dr ZABOŁOTNY, Wojciech (Institute of Electronic Systems, Warsaw University of Technology)

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