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## 3D TSV Hybrid Pixel Detector Modules with ATLAS FE-I4 Readout Electronic Chip

The through silicon via (TSV) technology has been introduced in a wide range of electronic packaging applications. Hybrid pixel detectors for x-ray imaging and for high-energy physics (HEP) can benefit from this technology as well [1], [2]. A 3D TSV prototype using the ATLAS FE-I4 readout electronic chip is presented in this paper. This type of readout chip is already prepared for the TSV backside process providing a TSV landing pad in Metal1 of the backend-of-line (BEOL) layer stack. Based on this precondition a TSV backside via-last process is developed on ATLAS FE-I4 readout chip wafer.

The readout chip wafer is thinned to 100 $\mu\text{m}$  and 80 $\mu\text{m}$  final thickness using a temporary carrier wafer bonded onto the wafer CMOS side. Using the established BOSCH-process, straight sidewall vias with 60 $\mu\text{m}$  in diameter are etched into the silicon from wafer backside. An electroplated Cu-redistribution layer (RDL) forms the electrical interconnection to the Metal1-BEOL-layer. The deposition process includes the filling of the TSVs and the formation of the wafer backside interconnection to the next substrate level. A nickel-gold pad finish enables the electrical chip connection by wire bonding as well as by soldering. In addition to the backside chip RDL, TSV capacity test structures and daisy chain test structures are implemented in the TSV chip design and are characterized after the wafer TSV processing.

Fully processed ATLAS FE-I4 readout chips are successfully tested and tuned. In addition, hybrid pixel detector modules are flip chip bonded using ATLAS FE-I4 TSV readout chips and planar sensor chips. After mounting the bare modules onto a support PCB, the complete setup is characterized in a source scan and is showing very promising results.

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