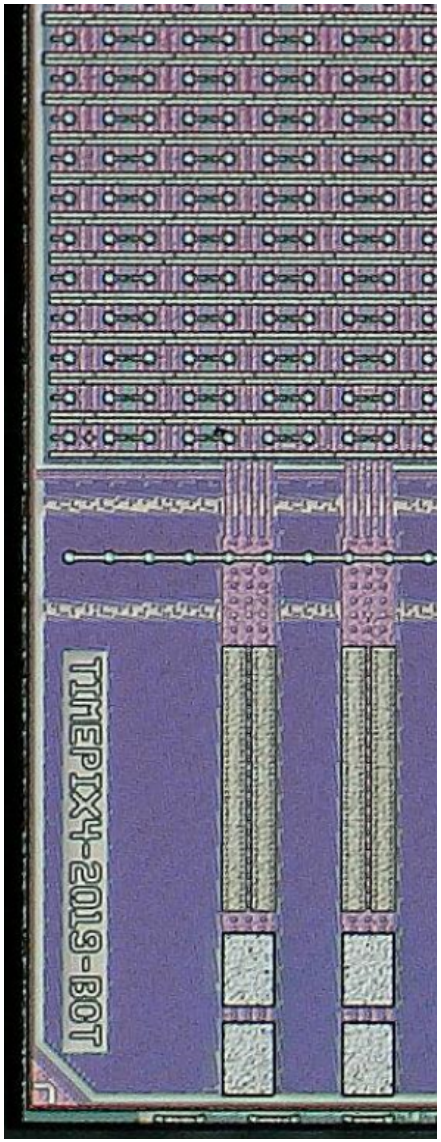


Timepix4, a large area pixel detector readout chip which can be tiled on 4 sides providing sub-200ps timestamp binning

Xavier Llopart[1], Jerome Alozy[1], Rafael Ballabriga[1], Michael Campbell[1], Raimon Casanova[2], Vladimir Gromov[3], Erik Heijne[1], Tuomas Poikela[1**], Edinei Santin[1***], Viros Sriskaran[1], Lukas Tlustos[1], Arseniy Vitkovskiy[3]

On behalf of the Medipix4 Collaboration

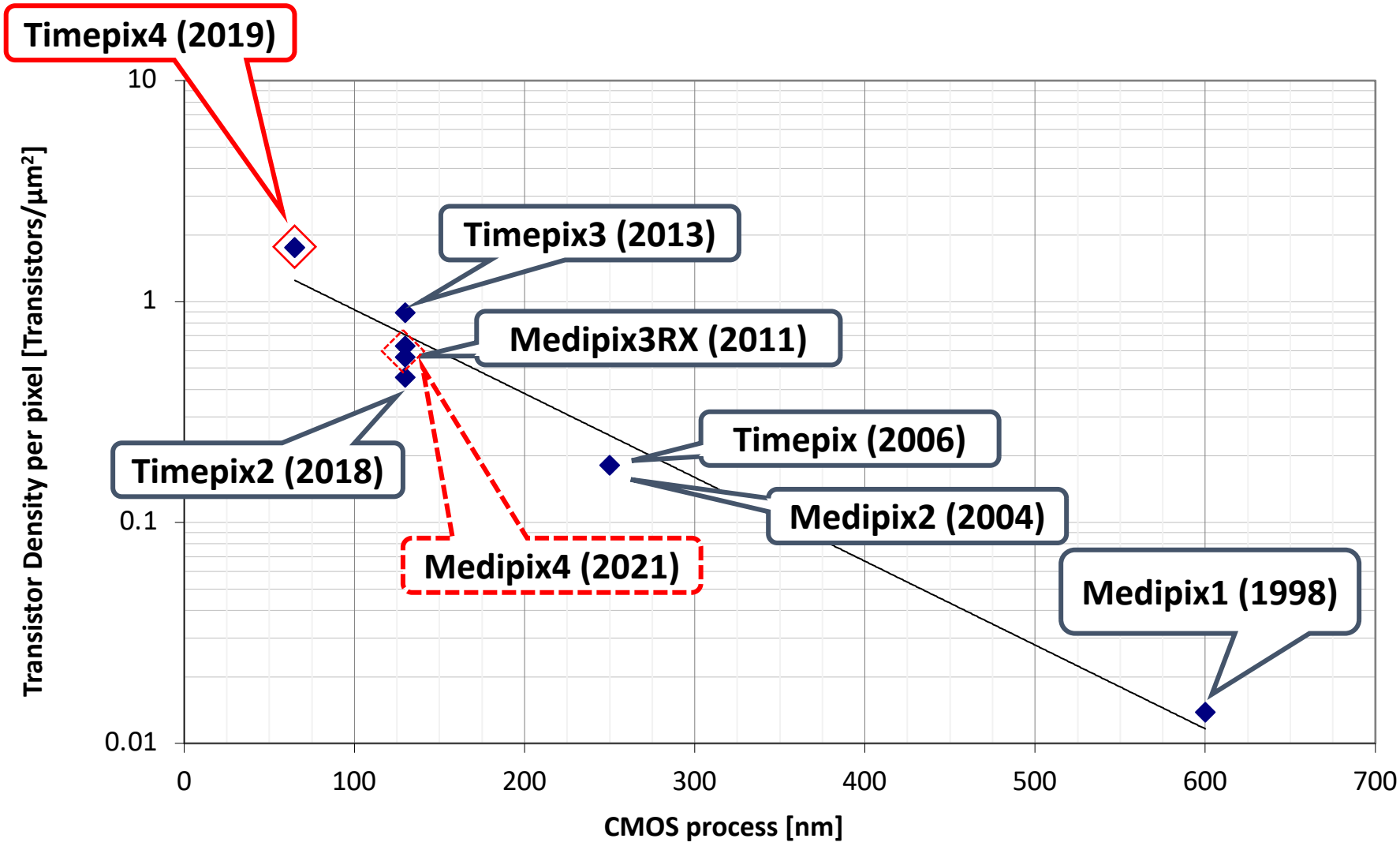
[1.] EP Department, CERN, 1211 Geneva 23, Switzerland
[2.] IFAE, Universitat Autònoma de Barcelona, E-08193 Bellaterra, Spain
[3.] NIKHEF, Science Park 105, 1098 XG Amsterdam, The Netherlands
** now with Nokia, Espoo, Finland
*** now with AlpsenTek, Zurich, Switzerland

Medipix4 Collaboration

- **Medipix4 Collaboration is set to provide the next generation of Medipix4 family chips (Medipix4 and Timepix4):**
  - Agreement signed on May 2016
  - 16 collaboration members
- **Timepix4 (2019)**
  - 65nm technology
  - Pixel matrix of 512 x 448 pixels (55 x 55 μm^2)
  - Particle identification and tracking (Data-driven and zero suppressed)
  - Imaging (frame based with CRW sequential readout)
  - Sub-ns time binning → ~195ps
  - Energy resolution → <1.5 KeV (FWHM, Si)
- **Medipix4 (2021)**
  - 130nm technology
  - Pixel matrix of 320 x 320 (75 x 75 μm^2) or 160 x 160 (150 x 150 μm^2)
  - Charge Summing architecture:
    - Dynamic range → to 140 KeV
    - Count Rate → to 10^8 ph/mm^2/s
    - Energy resolution < 2.2 KeV (FWHM, CdTe, CSM @ 60 KeV)
  - 2 thresholds @75 µm pixel or 8 thresholds @150 µm
- **Both chips will have a 4-side buttable architecture:**
  - Periphery integrated inside the pixel matrix
  - Prepare for readout using TSV (Through-Silicon-Vias)
  - Larger ASICs

- **CEA, Paris, France**
- **CERN, Geneva, Switzerland**
- **DESY, Hamburg, Germany**
- **Diamond Light Source, England, UK**
- **IEAP, Czech Technical University, Prague, Czech R.**
- **IFAE, Barcelona, Spain**
- **JINR, Dubna, Russian Federation**
- **NIKHEF, Amsterdam, The Netherlands**
- **University of California, Berkeley, USA**
- **University of Canterbury, Christchurch, New Zealand**
- **University of Geneva, Switzerland**
- **University of Glasgow, Scotland, UK**
- **University of Houston, USA**
- **University of Maastricht, The Netherlands**
- **University of Oxford, England, UK**
- **INFN, Italy**

Pixel detectors ASICs developed by Medipix Collaborations

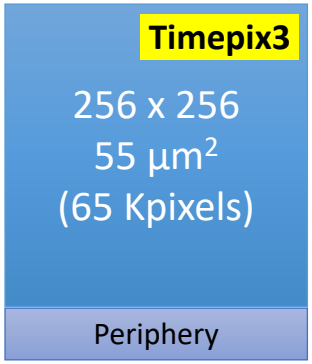


Timepix3 → Timepix4

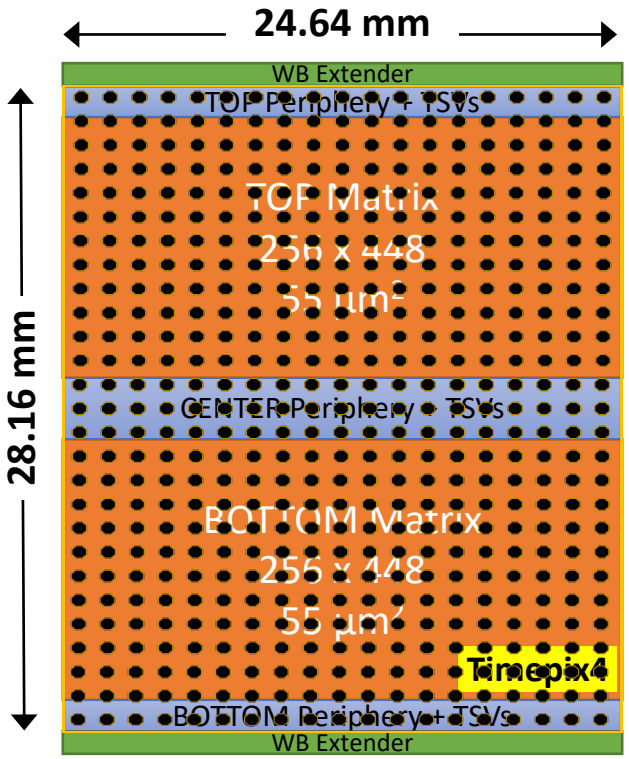
Timepix4: A 4-side tillable large single threshold particle detector chip with improved energy and time resolution and with high-rate imaging capabilities

			Timepix3 (2013)	Timepix4 (2019)	
Technology			130nm – 8 metal	65nm – 10 metal	
Pixel Size			55 x 55 µm	55 x 55 µm	
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448	**3.5x**
Sensitive area			1.98 cm^2	6.94 cm^2	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA		
		Event Packet	48-bit	64-bit	**33%**
		Max rate	0.43x10^6 hits/mm^2/s	**3.58x10^6 hits/mm^2/s**	**8x**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**	
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)	
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s	**6x**
TOT energy resolution			< 2KeV	< **1Kev**	**2x**
Time resolution			1.56ns	**195.3125ps**	**8x**
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	≤163.84 Gbps (16x @10.24 Gbps)	**32x**
Target global minimum threshold			<500 e^-	<500 e^-	

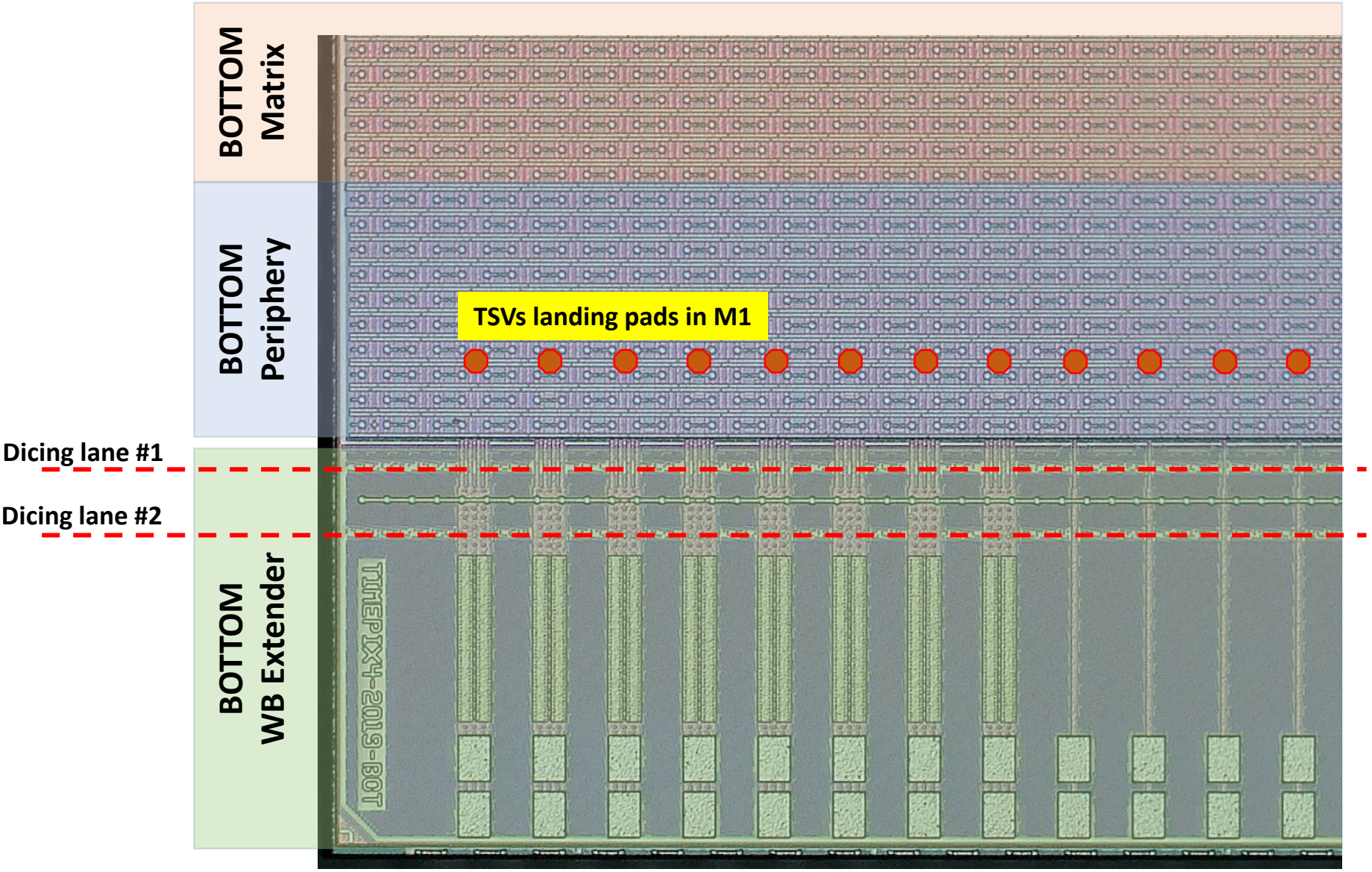
Timepix4 arrangement



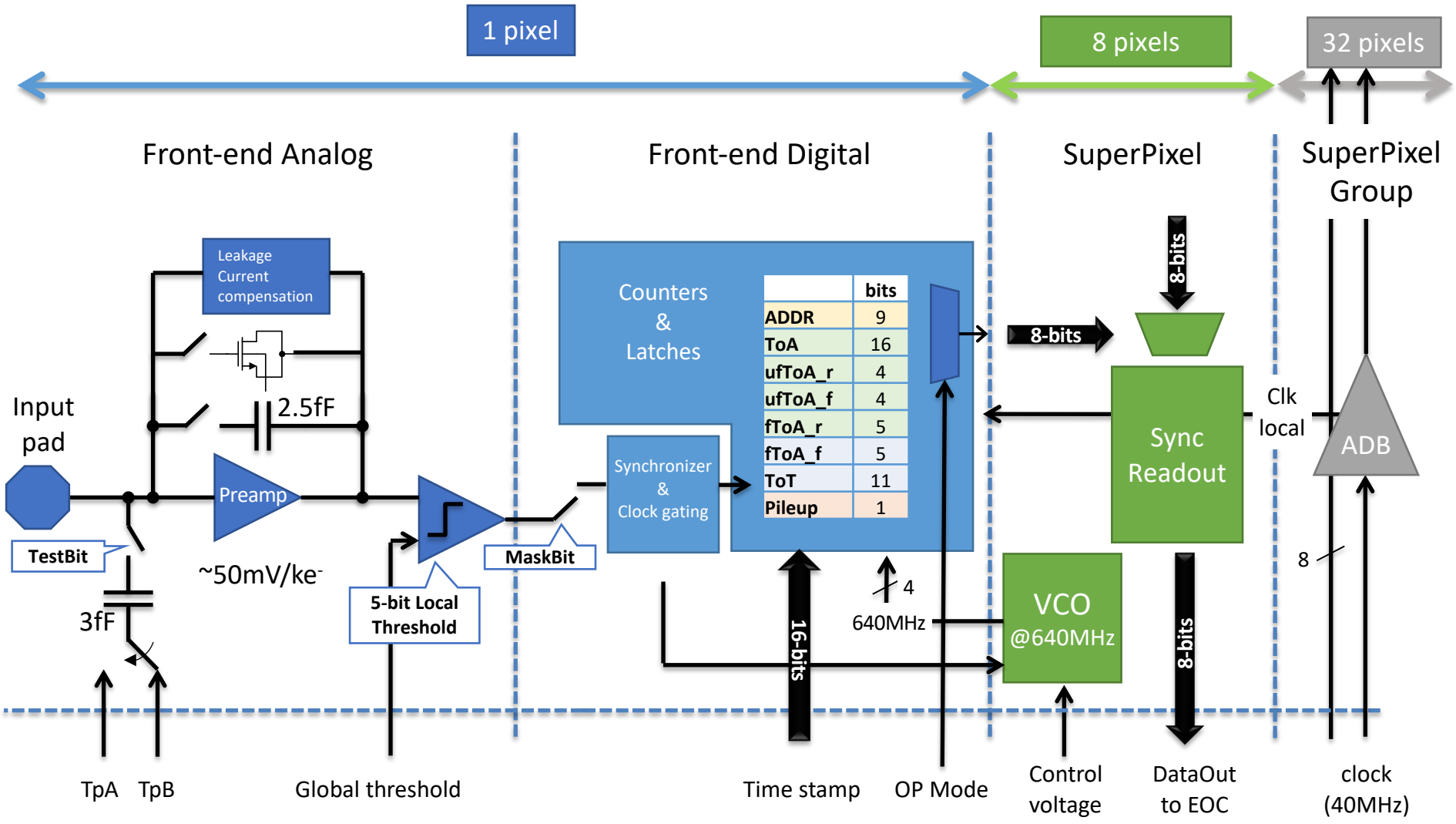
- 512 x 448 of 55 x 55 µm pixels
  - 2 Matrices (TOP and BOTTOM)
- 3 peripheries with TSV (Through-Silicon-Vias):
  - TOP, BOTTOM (TSV, WB): Data Readout (16x 10.24 Gbps Serializers)
  - CENTER (TSV): Analog Blocks (DACs, ADC, Band-Gap…)
- On-chip bump to pixel redistribution layer (RDL):
  - Pixel matrix pixels are shorter (51.4 µm) than sensor pixels (55 µm)
  - Equalized Cin for all pixels → ~46 fF increase for a 460 µm periphery
- Edge peripheries include 1mm Wire Bond Extender
- Dicing options:
  - With WB (Wire-Bonds Extenders): 29.96 mm x 24.7 mm
    - **>93.7%** active area (28.16mm x 24.64mm)
  - Without WB (TSV Only) : 28.22 mm x 24.7 mm
    - **>99.5%** active area (28.16mm x 24.64mm)
    - Through Silicon Vias (TSV) requires post processing at wafer level to create TSV and on the ASIC back sides RDL + BGA pads



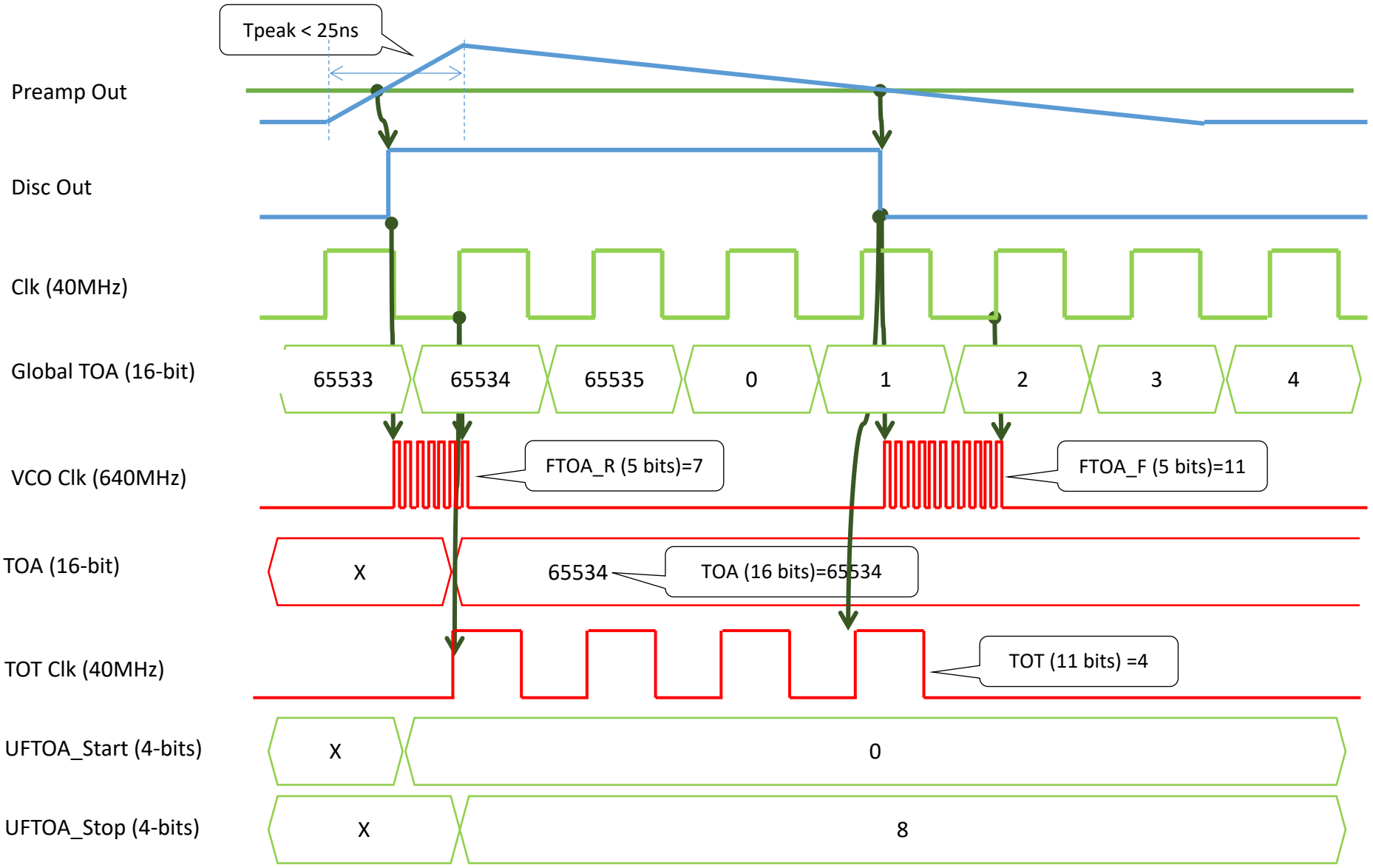
Timepix4 Bottom left detail



Timepix4 Pixel Schematic



Pixel Operation in TOA & TOT [DD]

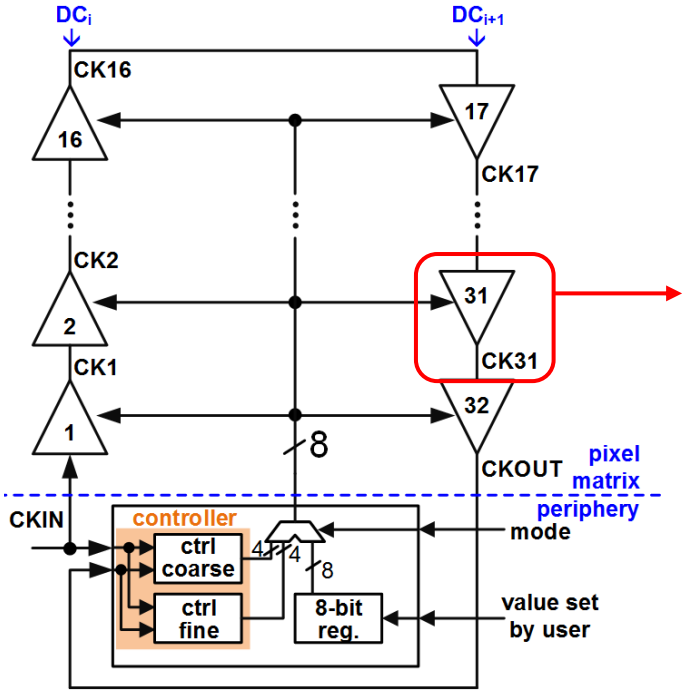


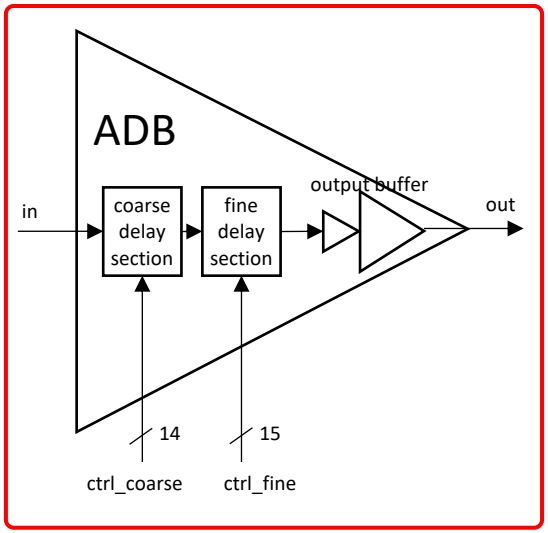
Full digital double column DLL

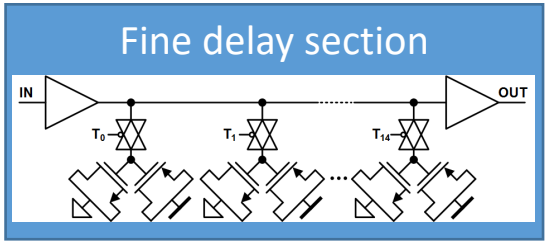
[448 dDLL: 224 Top Matrix and 224 Bottom Matrix]

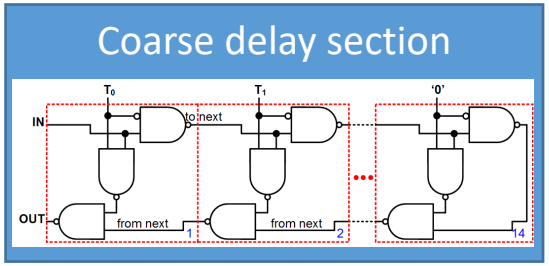
iWoRID 2018

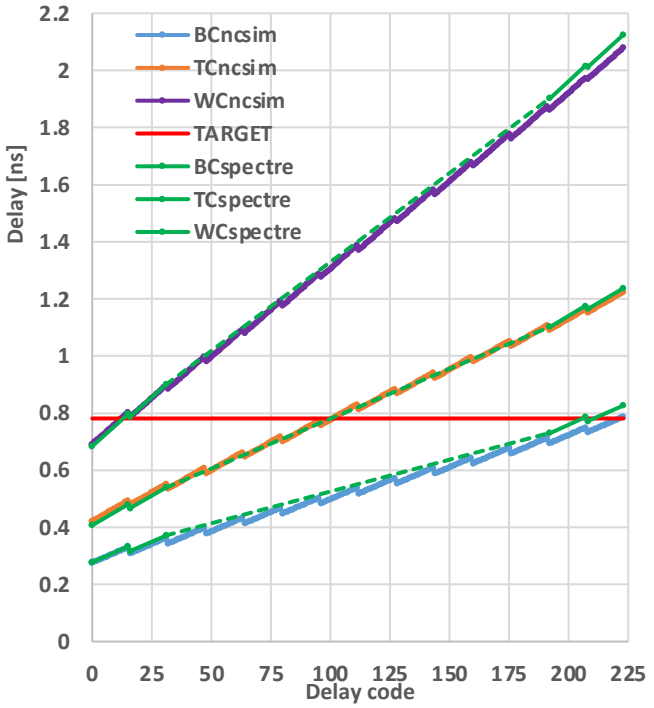
X. Llopart et al 2019 JINST 14 C01024







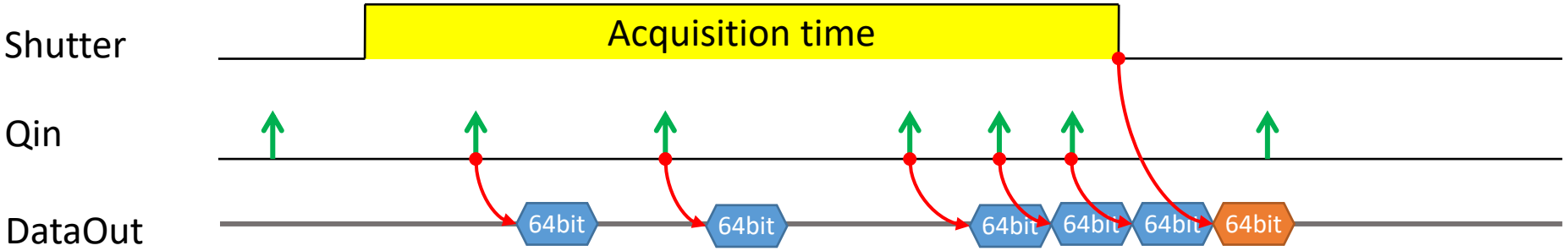




~22.7 mW/cm² to distribute a 40 MHz clock with a 100 ps_{rms}

Timepix4 Readout Modes : Data-Driven

- Zero-suppressed continuous data-driven
  - Output bandwidth from 40 Mbps (2.6 Hz/pixel) to 160 Gbps (10.8 KHz/pixel)
  - Uses Aurora 64b/66b standard encoding communication protocol



SPEC: Packet specifications ToA/ToT				
Name	**Width**	**MSB**	**LSB**	**Bits**
Top	1	63	63	[63:63]
EoC	8	62	55	[62:55]
SP	6	54	49	[54:49]
Pixel	3	48	46	[48:46]
ToA	16	45	30	[45:30]
ufToA_start	4	29	26	[29:26]
ufToA_stop	4	25	22	[25:22]
fToA_rise	5	21	17	[21:17]
fToA_fall	5	16	12	[16:12]
ToT	11	11	1	[11:1]
Pileup	1	0	0	[0:0]

Address: 18 bits

Time: 29 bits

Energy: 21 bits

Timepix4 Readout Modes : Frame-based

- Full frame readout with continuous read-write (CRW):
  - 8-bits or 16-bit counter depth
  - Uses Aurora 64b/66b standard encoding communication protocol
  - Frame rate limited by bandwidth (and probably power):
    - **Required Readout bandwidth before counter overflow:**
      - **8-bit @ 1Gc/mm^2/s >20.48 Gbps**
      - **16-bit @ 8Gc/mm^2/s >1.28 Gbps**
    - **Minimum → Maximum Frame Rates:**
      - **8-bit 338 fps @40Mbps → 86.5 Kfps @160 Gbps**
      - **16-bit 169 fps @40Mbps → 43.2 Kfps @160 Gbps**

16-bit frame

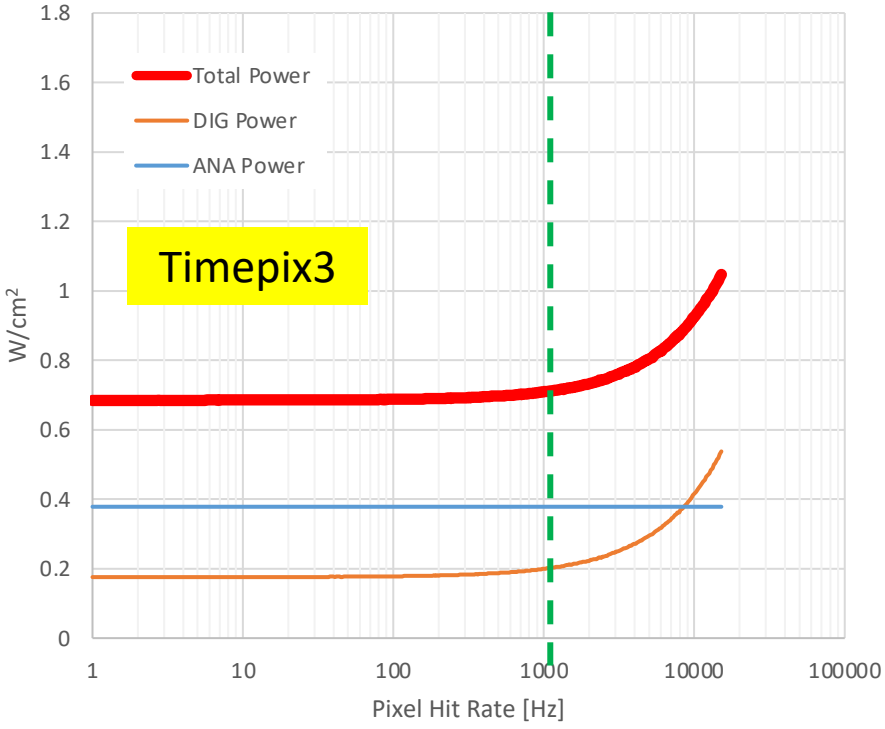
Name	Width	MSB	LSB	Bits
Pixel 3/7	16	63	48	[63:48]
Pixel 2/6	16	47	32	[47:32]
Pixel 1/5	16	31	16	[31:16]
Pixel 0/4	16	15	0	[15:0]

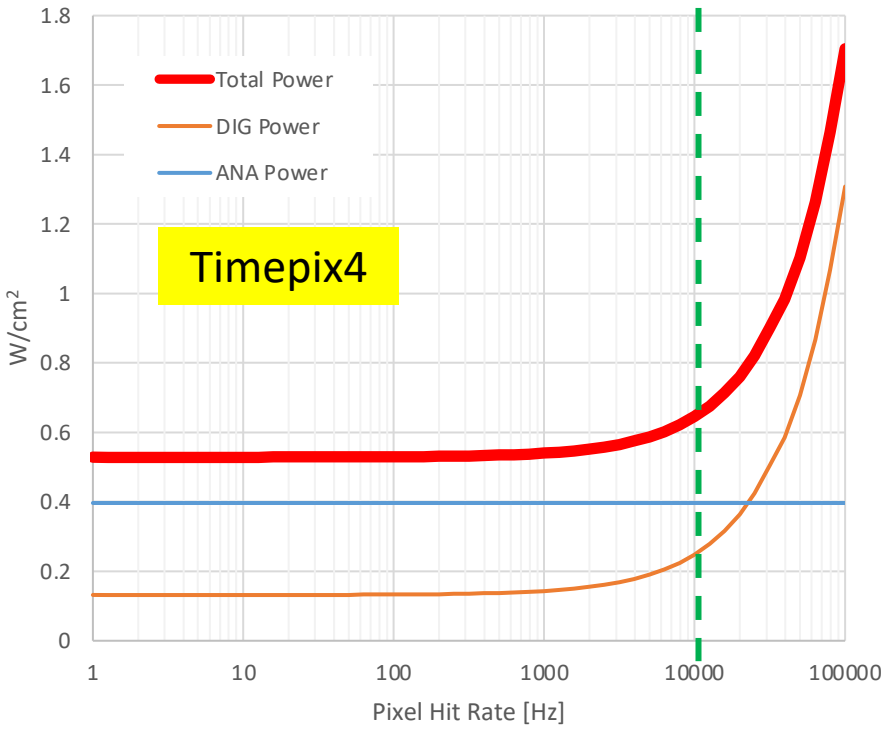
8-bit frame

Name	Width	MSB	LSB	Bits
Pixel 7	8	63	56	[63:56]
Pixel 6	8	55	48	[55:48]
Pixel 5	8	47	40	[47:40]
Pixel 4	8	39	32	[39:32]
Pixel 3	8	31	24	[31:24]
Pixel 2	8	23	16	[23:16]
Pixel 1	8	15	8	[15:8]
Pixel 0	8	7	0	[7:0]

Digital (dynamic) Power Consumption
[Data-Driven]

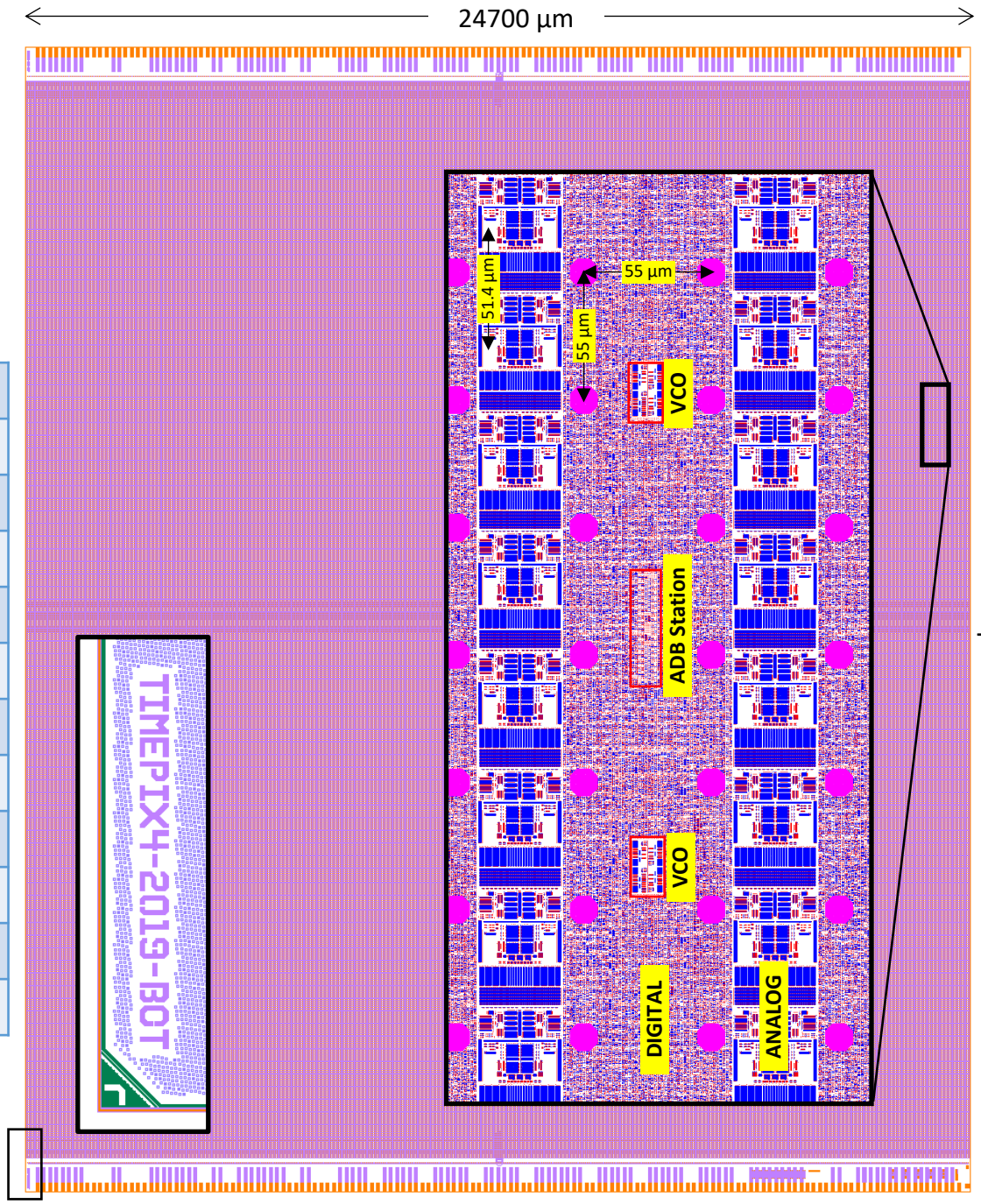
- Power consumption density is ~20 % less of Timepix3:
  - Digital power consumption 25% less
    - Improved clock distribution (dDLL)
    - 130nm → 65nm
  - Analog consumption is ~5% more
    - Minimize jitter → < 50ps
    - Compensate increase in input capacitance





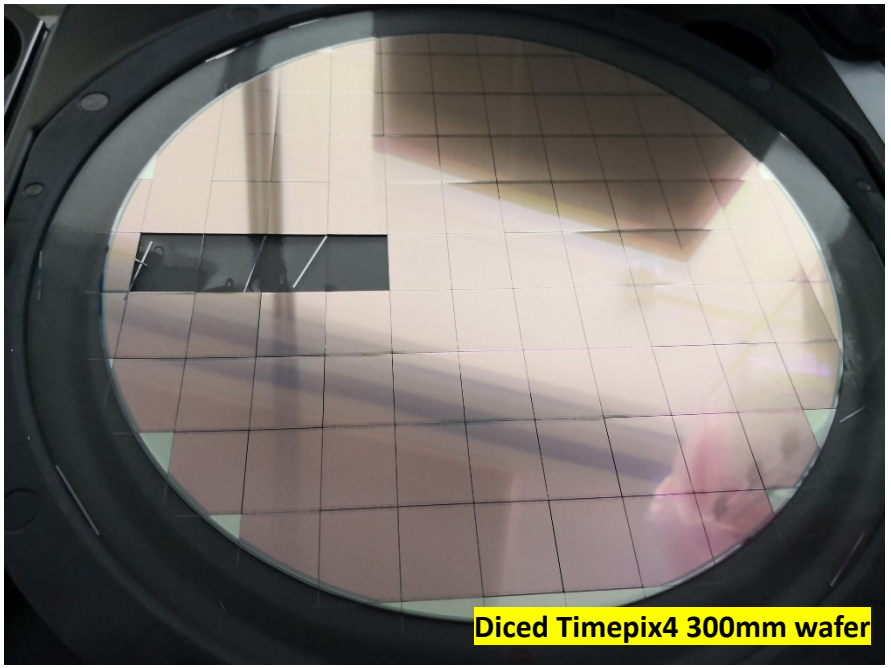
Timepix4 (November 2019)

Pixel size	55 x 55 µm
Array	512 x 448
Pixels	229376
aPLL	19
aDLL	16
10.24 Gbps serializers (Nikhef)	16
On-pixel VCO (Nikhef)	28672
dDLL Columns	448
Biasing DACs	13
ADC (IFAE)	1
Transistors in pixel	~6000
Transistors in chip	~1.5 bn

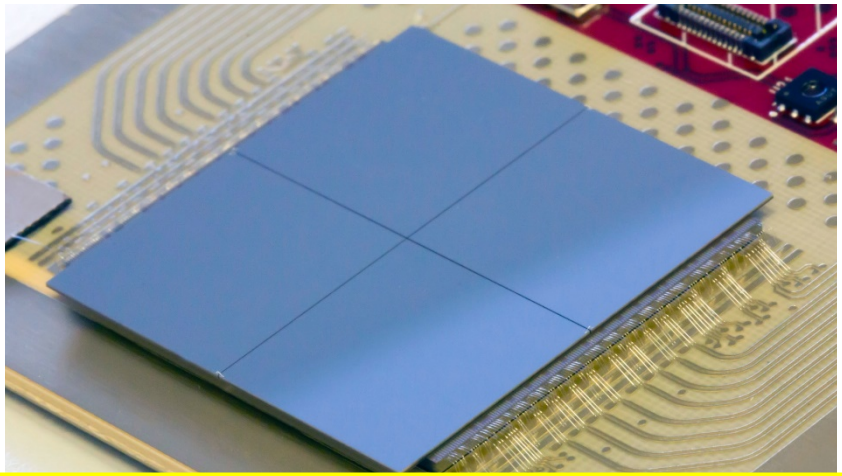


Timepix4 on Silicon

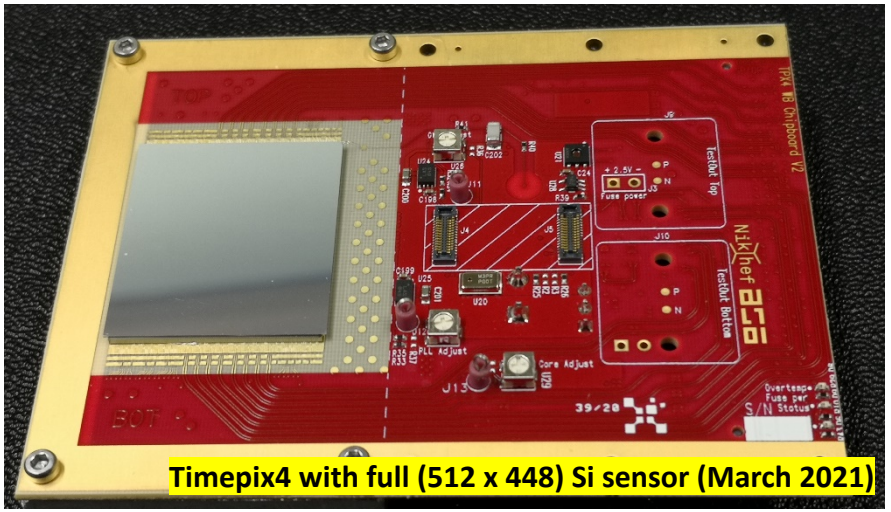
- First Timepix4 devices became available on the beginning of 2020 → chip debugging/characterization delayed by COVID19
- SPIDR4 readout system (Nikhef) used as a DAQ for initial chip debugging
- Testing of Timepix4 using the Wire Bond connections



Diced Timepix4 300mm wafer

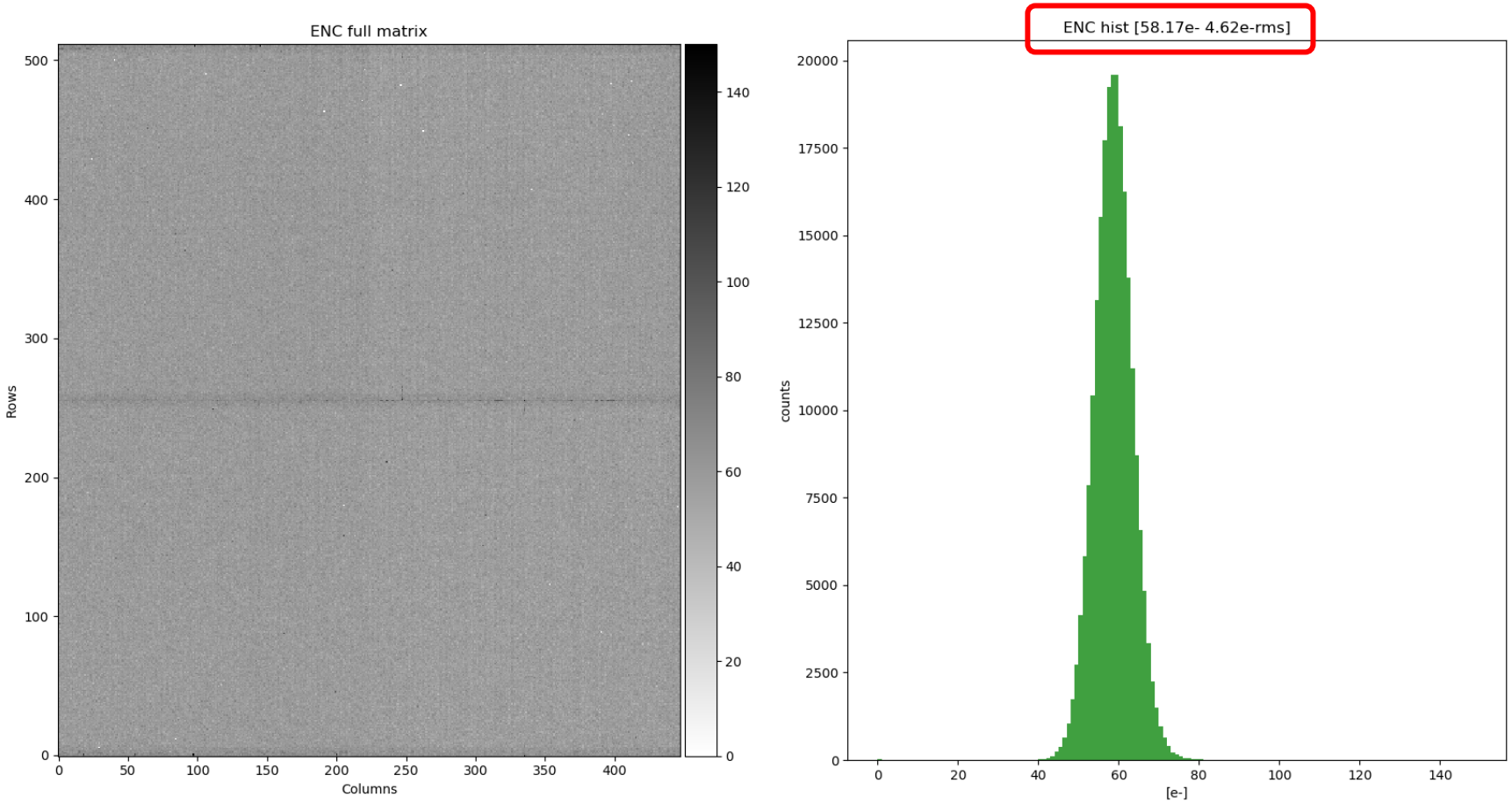


Timepix4 with 4x300 µm (256x256) edgeless Si sensor (August 2020)



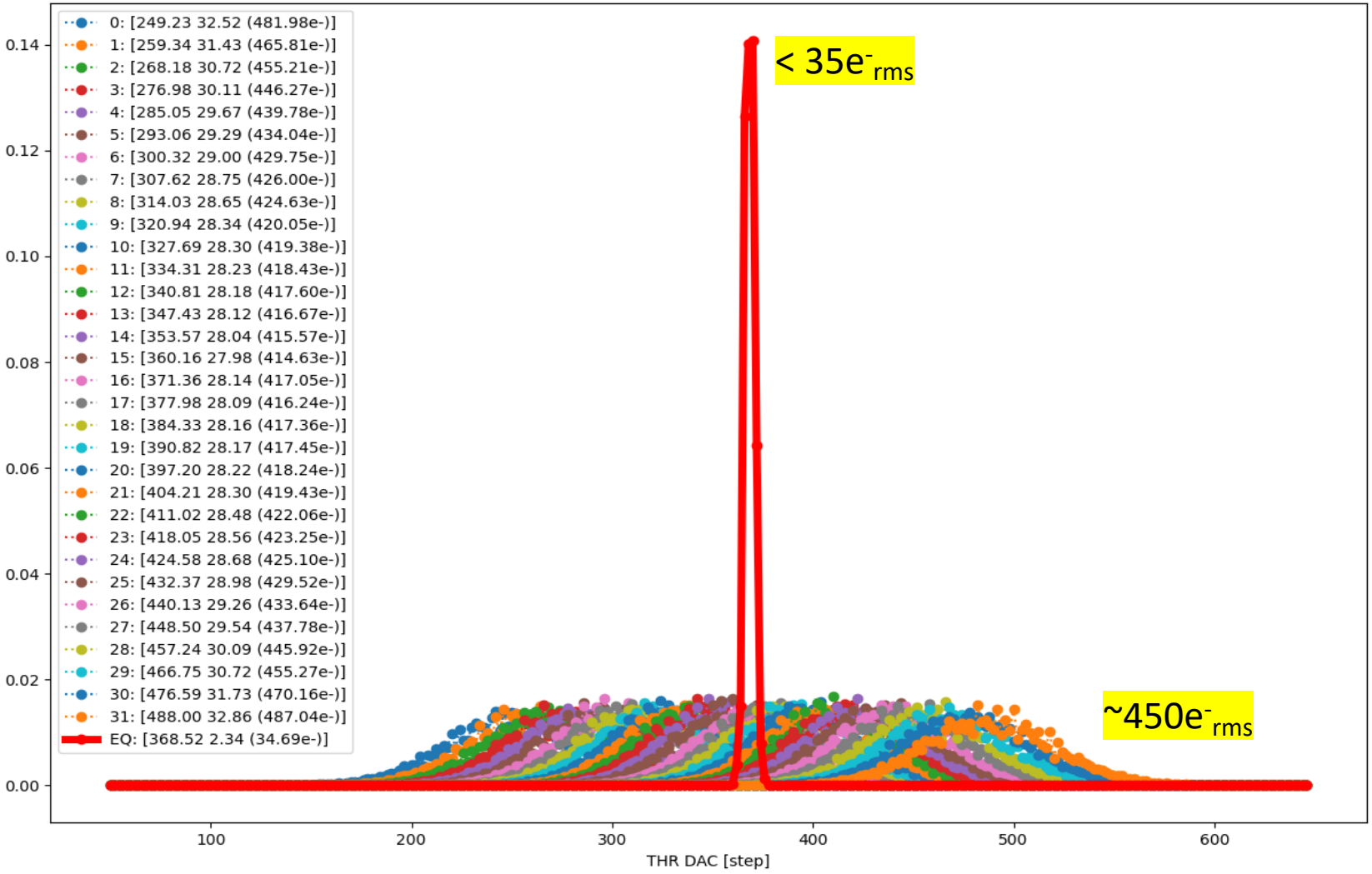
Timepix4 with full (512 x 448) Si sensor (March 2021)

Full matrix ENC [without sensor]



- Some mitigated degradation on pixels sitting on top of the active peripherial regions → doesn't affect the required minimum threshold (500e-)
- New version of Timepix4 should further improve the shielding on these areas
- With a Si sensor the noise slightly increase ~3e$^-$ / pixel

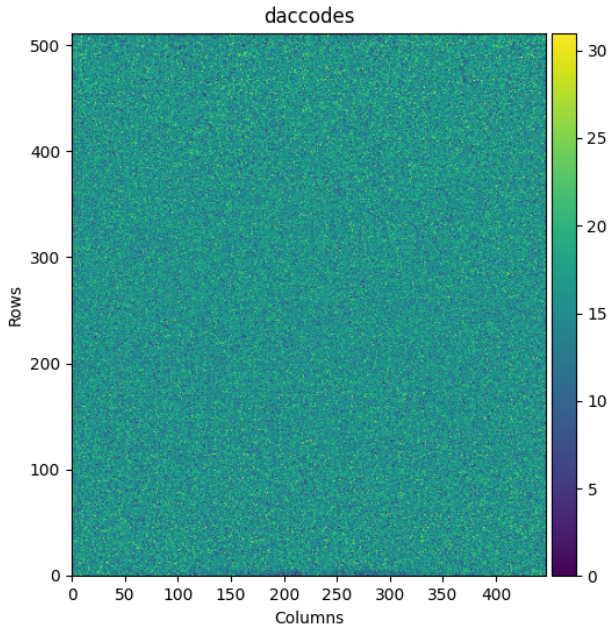
Timepix4 equalization

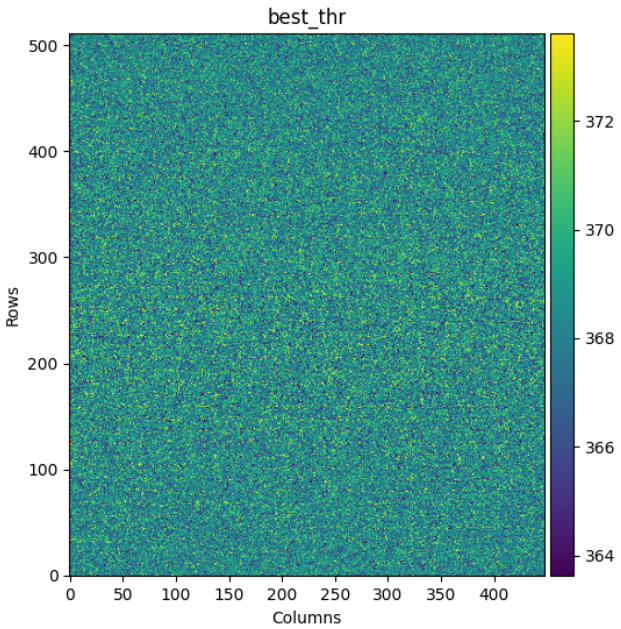


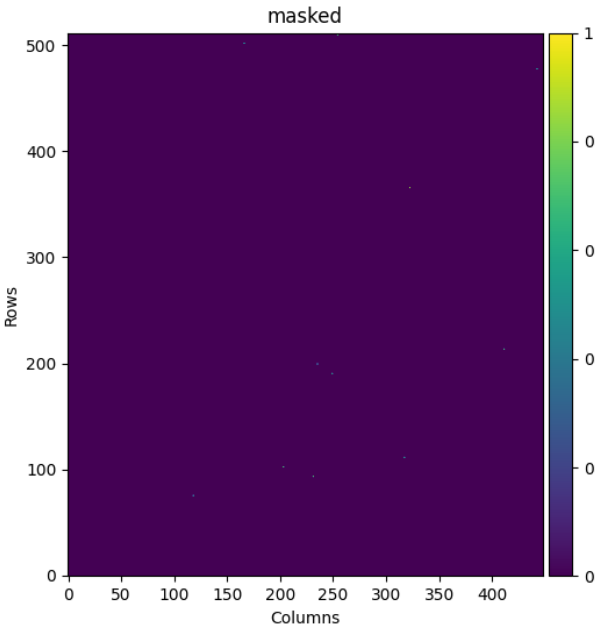
Equalization matrix

[PC24bit mode, e- collection high gain]

- All pixels responding (448x512) !
- 11 pixels masked
- No observable systematic across matrix

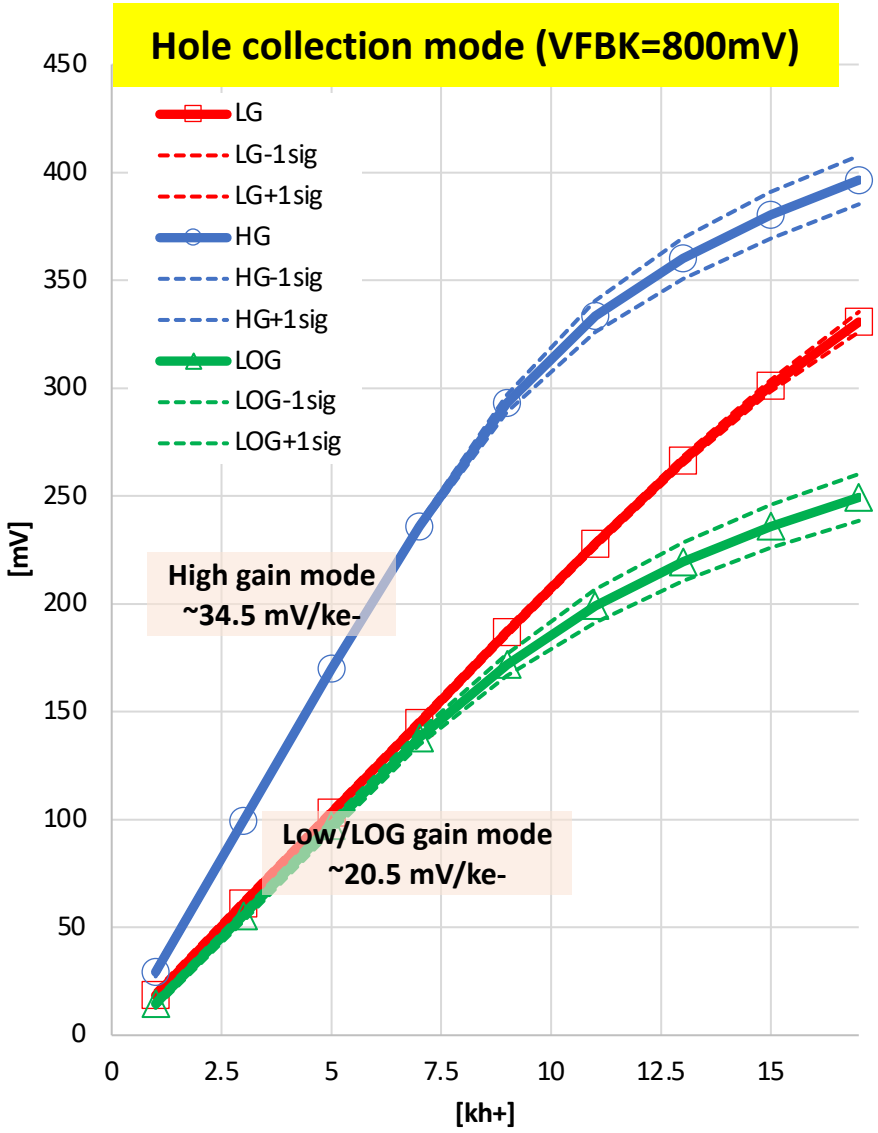


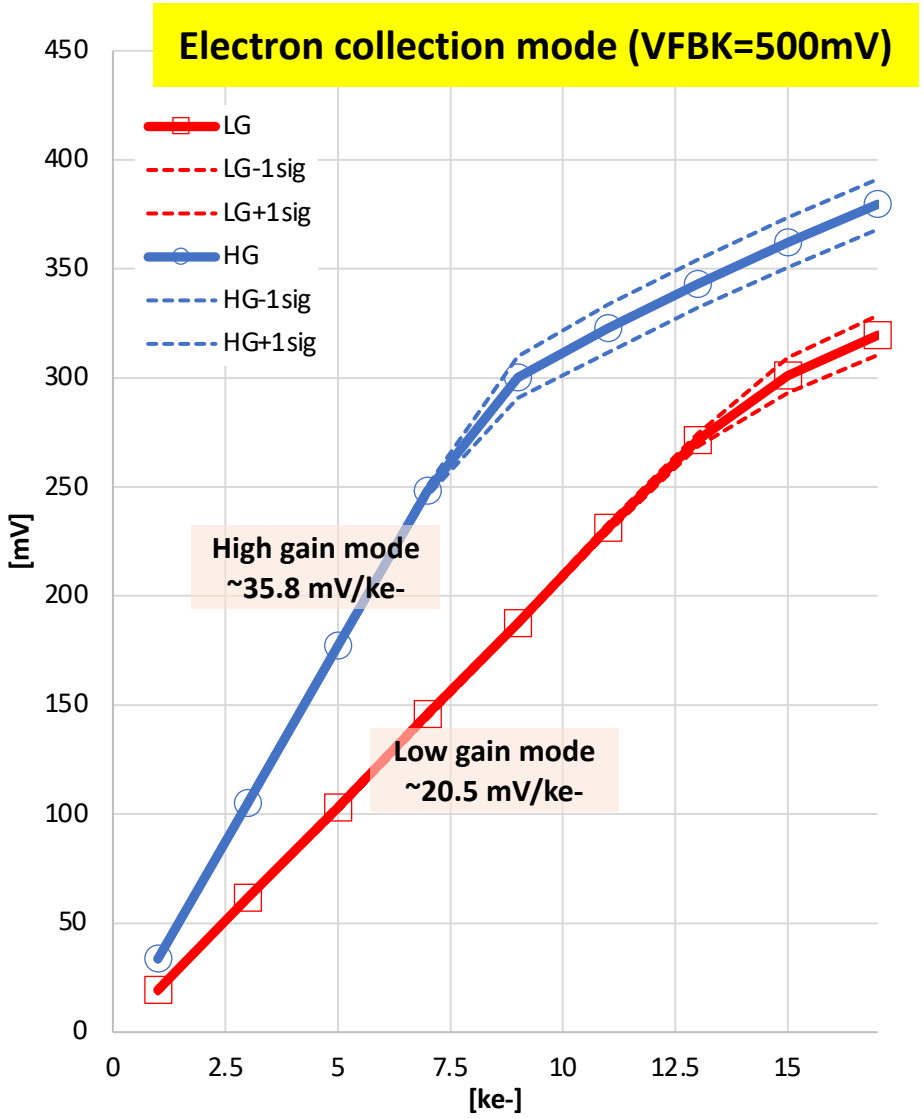




Gain slopes for different FE Gain

[TOA-TOT, ~200 pixels]

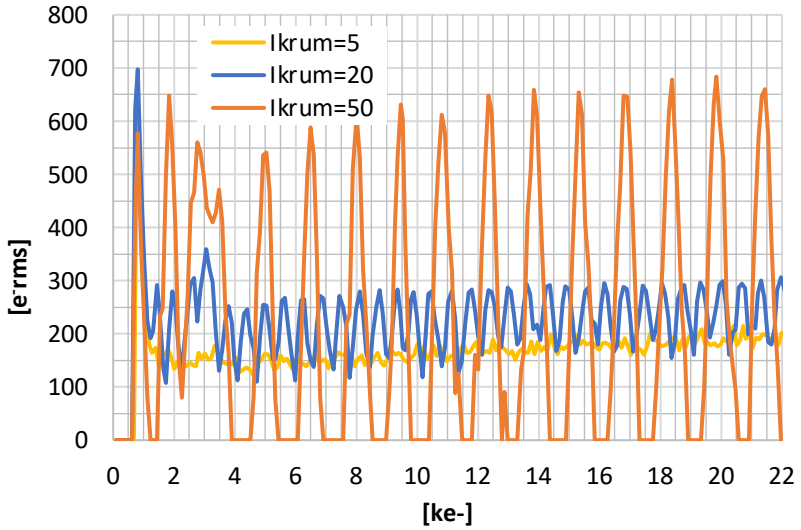


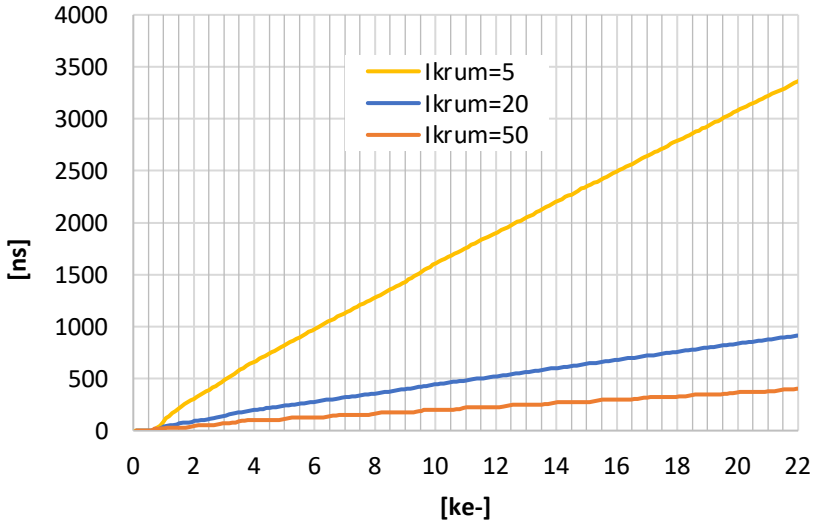


TOT Resolution

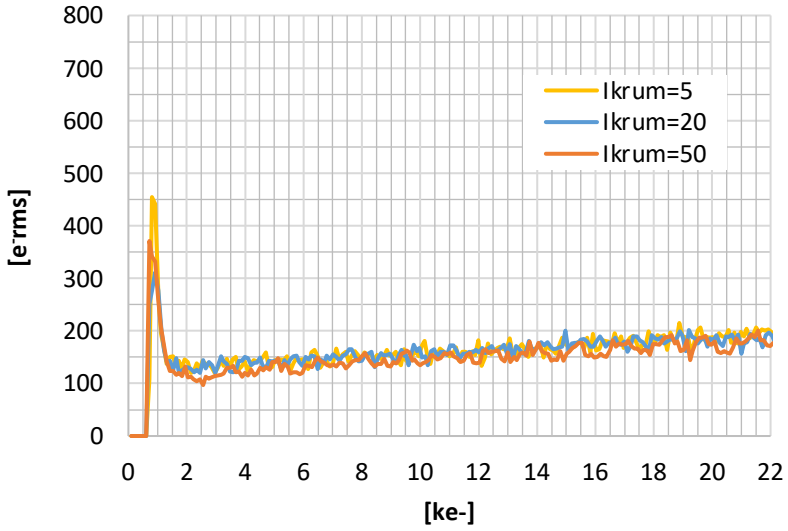
[Data-Driven 1 pixel, average of 200 events/TP, HG e-]

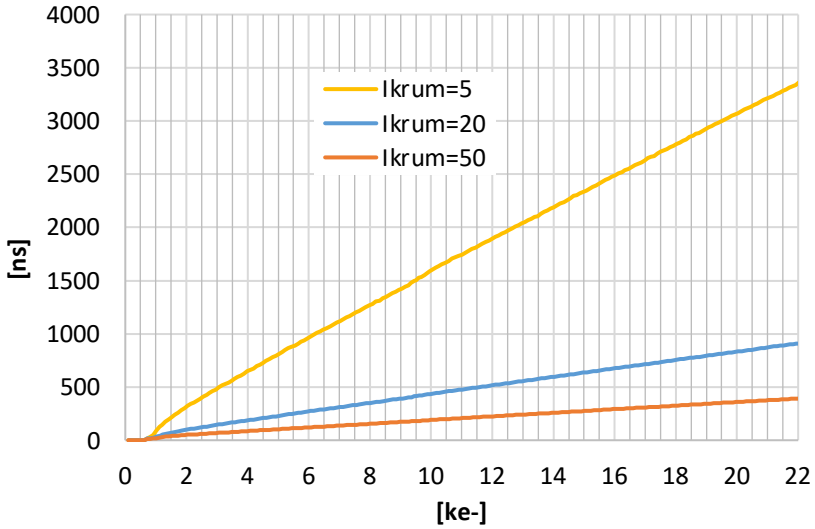
TOT (Timepix3)





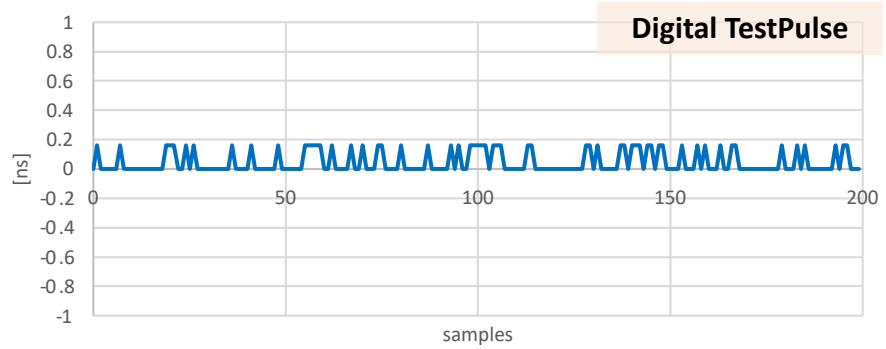
TOT-HD (Timepix4)

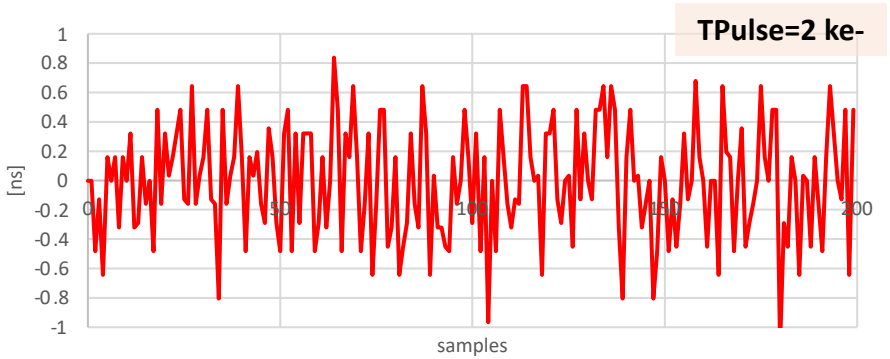


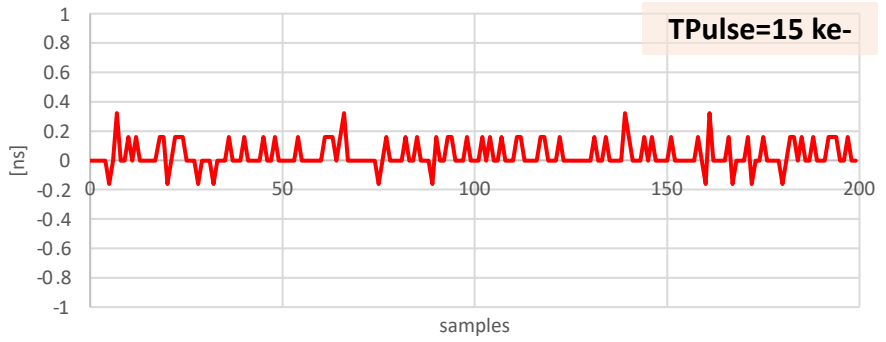


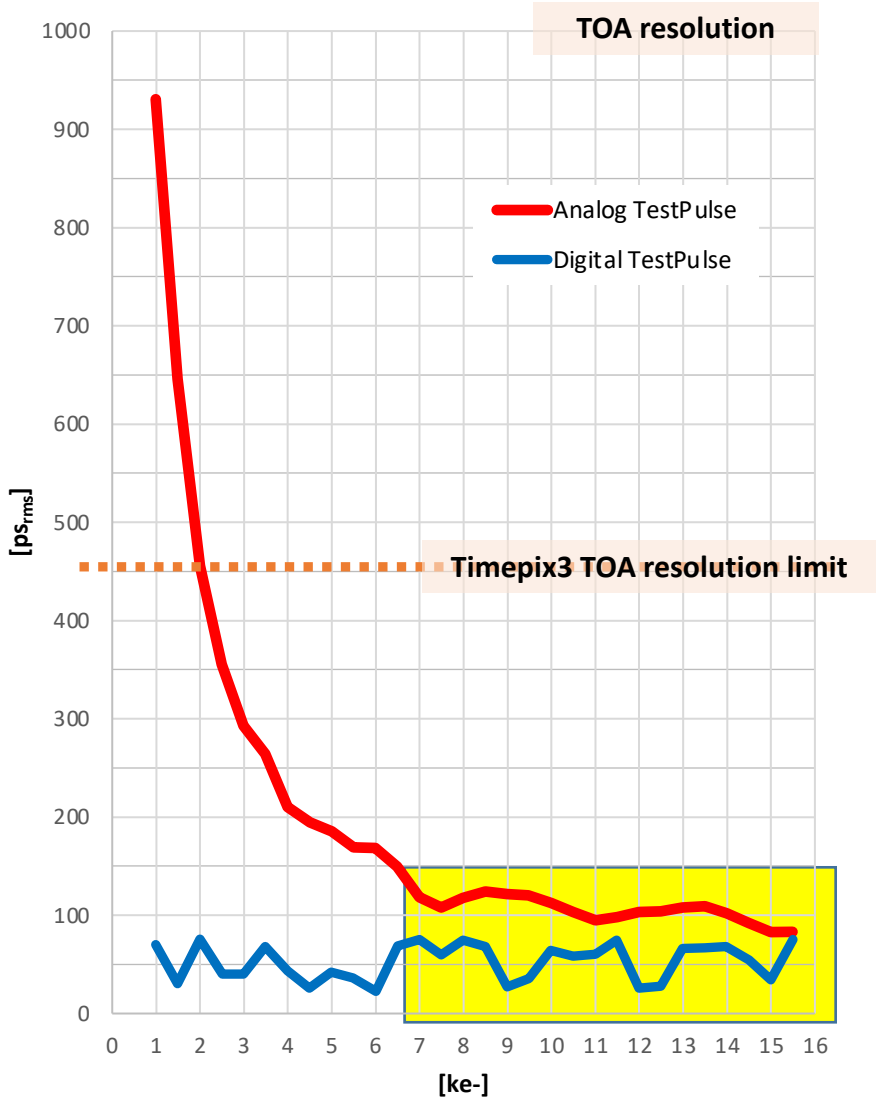
TOA Resolution

[TOA-TOT, 1 pixel, 10000 samples, HG e-]





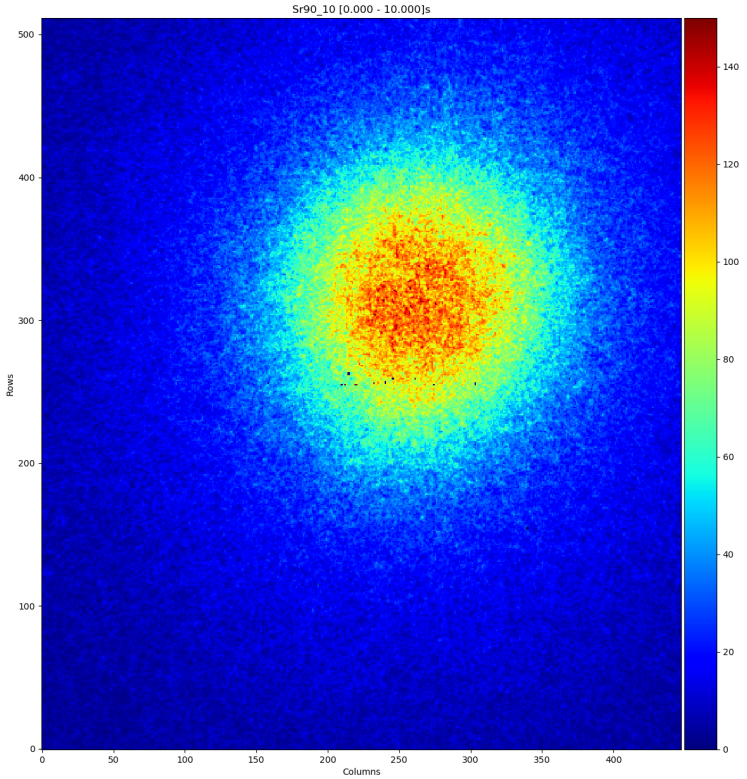




Timexpix4 in Data-Driven mode

[Thr=800e- with ~120 pixels masked]

- Timepix4 running at 2 x 2.56 Gbps links: 77 MHits/s
- ~6.1M packets received without errors: ~610 KHits/s

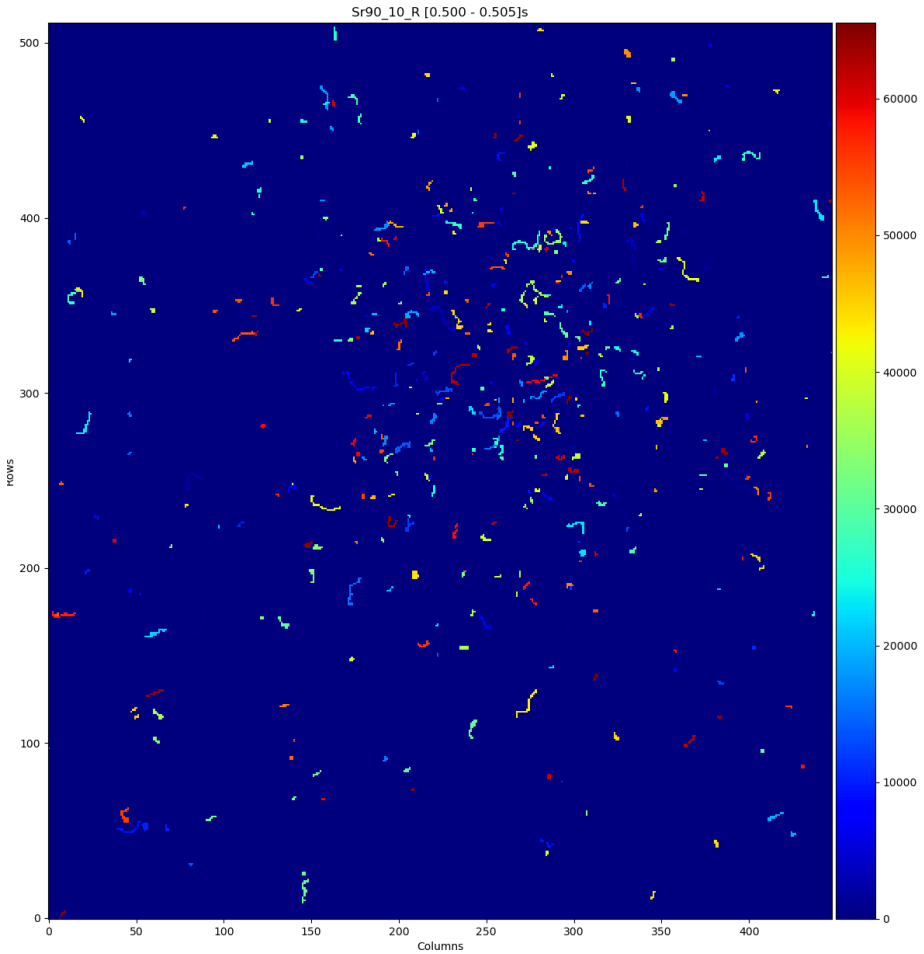


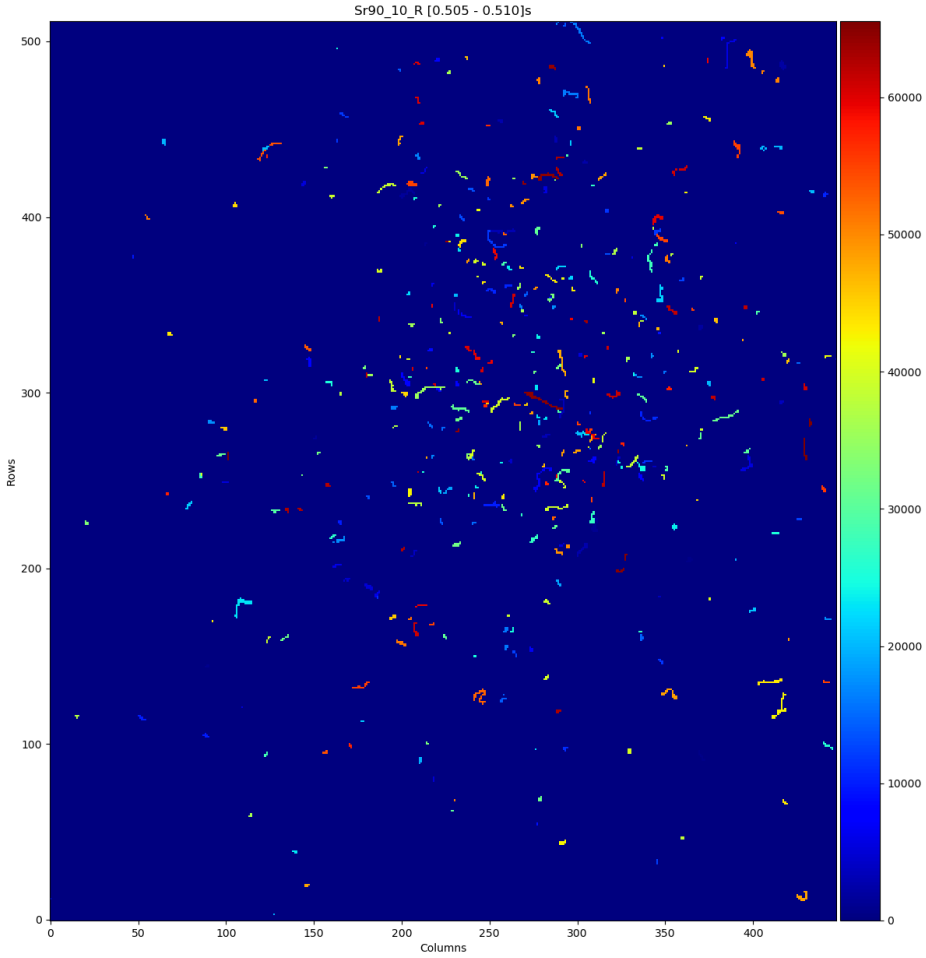
10s ^{90}Sr source
Photon Counting reconstruction

```
174579: SHUTTER_RISE T 36515
174580: top=1 eoc=5b pixnr=1fc toa=c9fe uftoa-sta/sto=1,f ftoa-f/r= 2, d tot=  0 pileup=0
174581: top=1 eoc=5b pixnr=1ff toa=c9ff uftoa-sta/sto=7,f ftoa-f/r= b, 4 tot=  1 pileup=0
174582: HEARTBEAT T 36870 (diff=1025)
174583: HEARTBEAT T 37895 (diff=1025)
174584: top=1 eoc=cd pixnr= ef toa=da1d uftoa-sta/sto=1,f ftoa-f/r= 6,15 tot= 14 pileup=0
174585: HEARTBEAT T 38920 (diff=1025)
174586: HEARTBEAT T 39945 (diff=1025)
174587: top=1 eoc=53 pixnr= cb toa=d622 uftoa-sta/sto=e,f ftoa-f/r= d, f tot=  8 pileup=0
174588: top=1 eoc=53 pixnr= d7 toa=d622 uftoa-sta/sto=c,1 ftoa-f/r= c, 6 tot=  0 pileup=0
174589: top=1 eoc=53 pixnr= d2 toa=d623 uftoa-sta/sto=0,e ftoa-f/r= 4, 4 tot= 10 pileup=0
174590: top=1 eoc=52 pixnr= cf toa=d622 uftoa-sta/sto=0,f ftoa-f/r= 6, f tot= 13 pileup=0
174591: top=1 eoc=53 pixnr= d0 toa=d623 uftoa-sta/sto=0,1 ftoa-f/r=10, 4 tot= 19 pileup=0
174592: top=1 eoc=52 pixnr= d4 toa=d623 uftoa-sta/sto=e,f ftoa-f/r=10, 3 tot= 2b pileup=0
174593: top=1 eoc=53 pixnr= d1 toa=d623 uftoa-sta/sto=0,f ftoa-f/r= 6, 5 tot= 15 pileup=0
174594: top=1 eoc=53 pixnr= d6 toa=d623 uftoa-sta/sto=0,7 ftoa-f/r= b, 5 tot= 3e pileup=0
174595: top=1 eoc=54 pixnr= d2 toa=d623 uftoa-sta/sto=0,f ftoa-f/r= 8, 4 tot= 51 pileup=0
174596: HEARTBEAT T 40970 (diff=1025)
174597: top=1 eoc=3b pixnr=14d toa=f0d6 uftoa-sta/sto=3,f ftoa-f/r=12,11 tot=  a pileup=0
174598: top=1 eoc=3b pixnr=147 toa=f0d6 uftoa-sta/sto=0,f ftoa-f/r= 1, 7 tot= 1a pileup=0
174599: top=1 eoc=3b pixnr=14c toa=f0d6 uftoa-sta/sto=3,8 ftoa-f/r= 5,11 tot= 22 pileup=0
174600: top=1 eoc=92 pixnr=1ef toa=f148 uftoa-sta/sto=1,3 ftoa-f/r= 9, d tot=  1 pileup=0
174601: top=1 eoc=94 pixnr=1f2 toa=f158 uftoa-sta/sto=1,f ftoa-f/r=10,14 tot=  1 pileup=0
174602: top=1 eoc=93 pixnr=1f5 toa=f148 uftoa-sta/sto=f,1 ftoa-f/r=15, 4 tot=  6 pileup=0
174603: top=1 eoc=92 pixnr=1f0 toa=f148 uftoa-sta/sto=e,f ftoa-f/r= 7, f tot=  7 pileup=0
174604: top=1 eoc=94 pixnr=1f7 toa=f148 uftoa-sta/sto=0,e ftoa-f/r= 8, 7 tot=  8 pileup=0
174605: top=1 eoc=94 pixnr=1f8 toa=f148 uftoa-sta/sto=3,f ftoa-f/r=14, 8 tot=  8 pileup=0
174606: top=1 eoc=93 pixnr=1f1 toa=f148 uftoa-sta/sto=e,f ftoa-f/r= a, 9 tot= 14 pileup=0
174607: top=1 eoc=92 pixnr=1ea toa=f148 uftoa-sta/sto=3,c ftoa-f/r= 6, a tot= 1f pileup=0
174608: top=1 eoc=93 pixnr=1fd toa=f148 uftoa-sta/sto=f,f ftoa-f/r= 3, 7 tot= 17 pileup=0
174609: top=1 eoc=94 pixnr=1f3 toa=f148 uftoa-sta/sto=1,f ftoa-f/r= a, 9 tot= 19 pileup=0
174610: top=1 eoc=92 pixnr=1f4 toa=f148 uftoa-sta/sto=f,f ftoa-f/r=12, f tot= 1c pileup=0
174611: top=1 eoc=94 pixnr=1fd toa=f148 uftoa-sta/sto=3,f ftoa-f/r= a, 4 tot=  8 pileup=0
174612: top=1 eoc=93 pixnr=1f6 toa=f148 uftoa-sta/sto=e,8 ftoa-f/r= a, 9 tot= 18 pileup=0
174613: top=1 eoc=94 pixnr=1f9 toa=f148 uftoa-sta/sto=7,1 ftoa-f/r= 2, 8 tot= 16 pileup=0
174614: top=1 eoc=93 pixnr=1fe toa=f148 uftoa-sta/sto=f,0 ftoa-f/r=15, 4 tot= 13 pileup=0
174615: top=1 eoc=94 pixnr=1fc toa=f148 uftoa-sta/sto=3,0 ftoa-f/r= 0, 8 tot= 27 pileup=0
174616: top=1 eoc=92 pixnr=1eb toa=f148 uftoa-sta/sto=3,f ftoa-f/r= 7,11 tot= 4c pileup=0
174617: HEARTBEAT T 41995 (diff=1025)
174618: top=1 eoc= 8 pixnr=  0 toa=f674 uftoa-sta/sto=1,f ftoa-f/r= 2, a tot= 13 pileup=0
174619: top=1 eoc= 7 pixnr=  5 toa=f674 uftoa-sta/sto=e,8 ftoa-f/r= 8, 6 tot= 1c pileup=0
174620: top=1 eoc= 7 pixnr=  4 toa=f674 uftoa-sta/sto=e,f ftoa-f/r= 9, d tot= 37 pileup=0
174621: top=1 eoc=3d pixnr=1a0 toa=f7a5 uftoa-sta/sto=7,f ftoa-f/r= 5,13 tot=  1 pileup=0
174622: top=1 eoc=3d pixnr=1a2 toa=f7ac uftoa-sta/sto=e,f ftoa-f/r= c,16 tot= 1b pileup=0
174623: top=1 eoc=3d pixnr=1a1 toa=f7ac uftoa-sta/sto=e,1 ftoa-f/r= c,13 tot= 2d pileup=0
174624: HEARTBEAT T 43020 (diff=1025)
174625: top=1 eoc=a7 pixnr=181 toa=fd24 uftoa-sta/sto=0,f ftoa-f/r=13,12 tot=  f pileup=0
174626: top=1 eoc=a8 pixnr=182 toa=fd25 uftoa-sta/sto=0,f ftoa-f/r=14, 5 tot= 13 pileup=0
174627: top=1 eoc=a7 pixnr=185 toa=fd25 uftoa-sta/sto=7,f ftoa-f/r= 5, 1 tot= 13 pileup=0
174628: top=1 eoc=a7 pixnr=182 toa=fd24 uftoa-sta/sto=0,f
174629: top=1 eoc=a7 pixnr=186 toa=fd25 uftoa-sta/sto=7,8
```

Raw Data-Driven data

Previous data with 5ms time slices

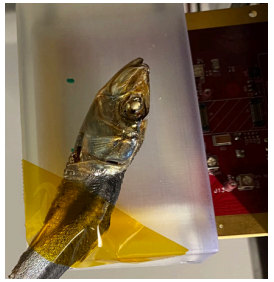


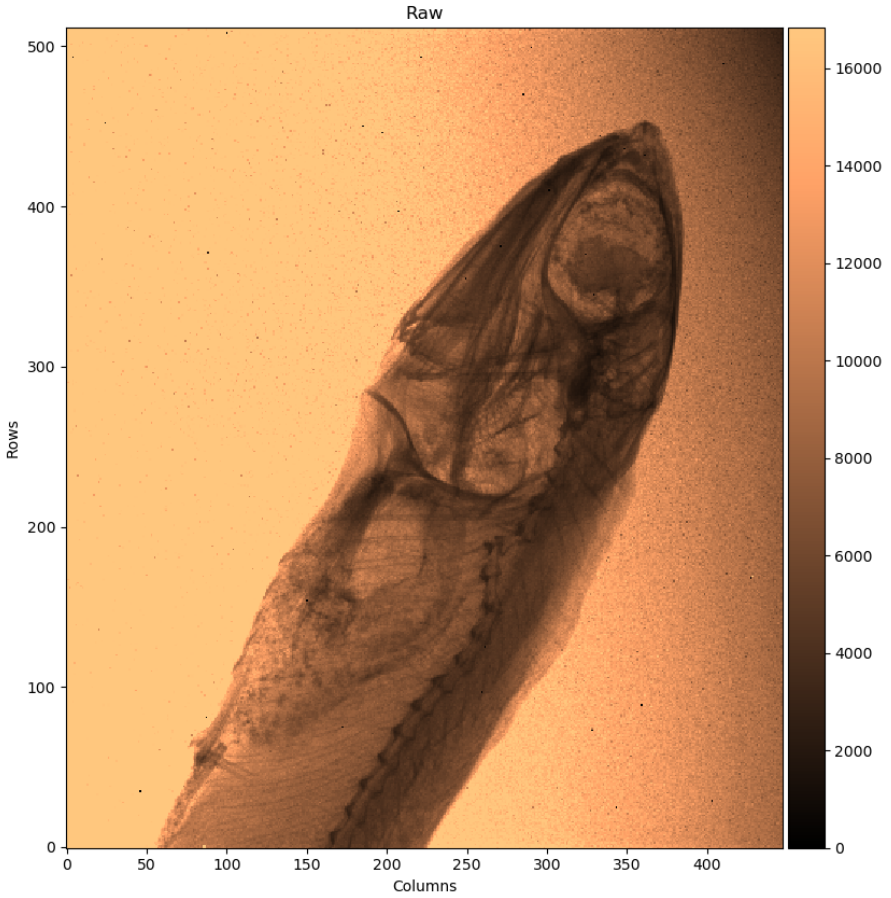


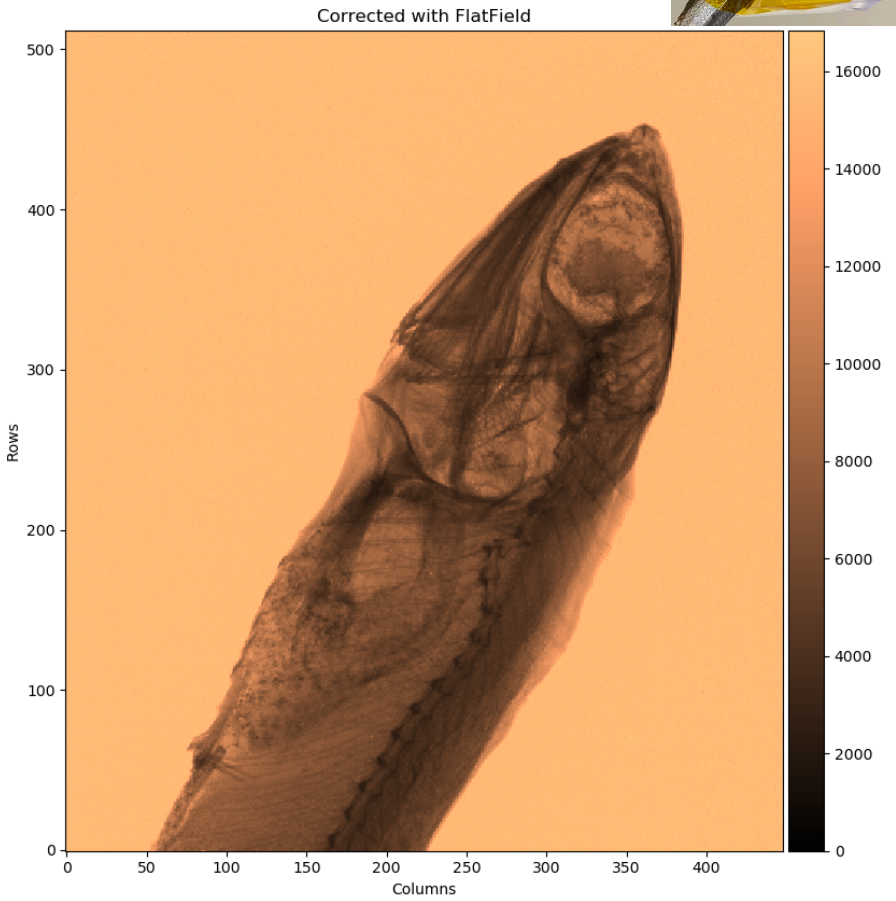
Color coding indicates arrival time (TOA)

Timepix4 with 300 µm Si Sensor Full sensor
[CRW 16-bit Frame Based mode, Thr ~1 ke-]

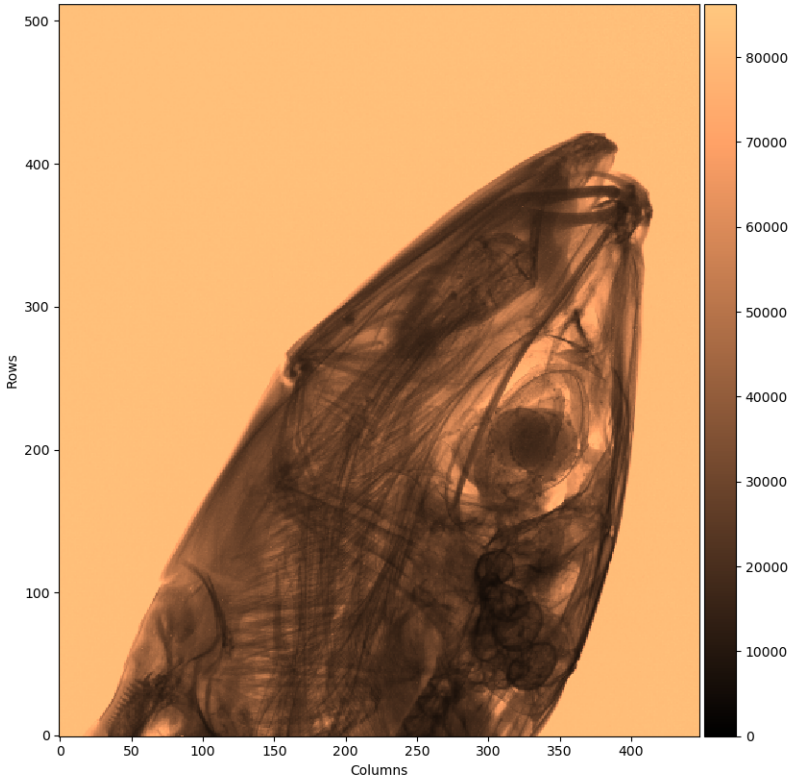
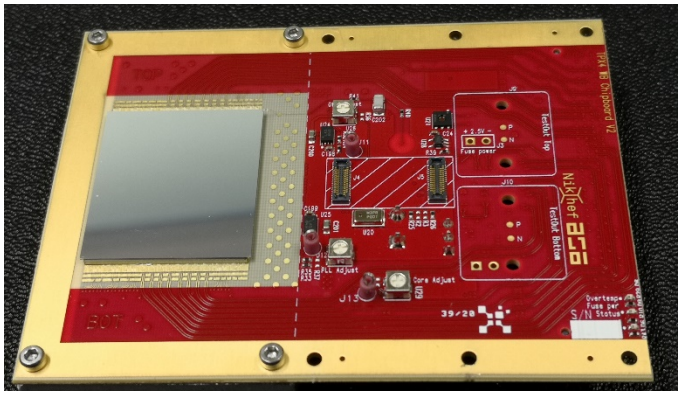
- 2s acquisition X-ray source, Cu target @30kVp
- 20 Flatfield acquisition used for correction
- Excellent bumping! Only 6 unconnected pixels (99.997% good pixels)







Conclusions

- Timepix4 is the new particle-tracker and photon counting hybrid pixel detector designed with the support of the **Medipix4 collaboration**:
  - Large area hybrid pixel detector with **6.94 cm^2** sensitive area
  - 4-side buttable with **<0.5% dead area**
  - TOA: **23-bit dynamic range (1.6ms) with 195 ps LSB**
  - TOT: **15-bit dynamic range with ~200 e$^-$rms resolution**
  - PC: **8-bit or 16-bit CRW up to 5*10^9 hits/mm^2/s**
  - Readout: **Up to 160 Gbps readout bandwidth**
  - **Very configurable architecture** to accommodate a large number of different applications

- Next steps:
  - Different test beams planned to extract Timepix4 timing & energy resolution (MCP, LGADs,…)
  - Just submitted a Timepix4 mask change revision to further improve the pixel shielding on top of peripheral areas
  - First TSV devices by the end of 2021
  - Medipix4 submission scheduled by the end of 2021