Timepix4, a large area pixel detector readout chip which can be tiled on 4 sides providing sub-200ps timestamp binning

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On behalf of the Medipix4 Collaboration

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* now with Nokia, Espoo, Finland
*** now with AlpsenTek, Zurich, Switzerland
Medipix4 Collaboration

- Medipix4 Collaboration is set to provide the next generation of Medipix4 family chips (Medipix4 and Timepix4):
  - Agreement signed on May 2016
  - 16 collaboration members

- Timepix4 (2019)
  - 65nm technology
  - Pixel matrix of 512 x 448 pixels (55 x 55 µm²)
  - Particle identification and tracking (Data-driven and zero suppressed)
  - Imaging (frame based with CRW sequential readout)
  - Sub-ns time binning → ~195ps
  - Energy resolution → <1.5 KeV (FWHM, Si)

- Medipix4 (2021)
  - 130nm technology
  - Pixel matrix of 320 x 320 (75 x 75 µm²) or 160 x 160 (150 x 150 µm²)
  - Charge Summing architecture:
    - Dynamic range → to 140 KeV
    - Count Rate → to 10⁸ ph/mm²/s
    - Energy resolution < 2.2 KeV (FWHM, CdTe, CSM @ 60 KeV)
  - 2 thresholds @75 µm pixel or 8 thresholds @150 µm

- Both chips will have a 4-side buttable architecture:
  - Periphery integrated inside the pixel matrix
  - Prepare for readout using TSV (Through-Silicon-Vias)
  - Larger ASICs

- CEA, Paris, France
- CERN, Geneva, Switzerland
- DESY, Hamburg, Germany
- Diamond Light Source, England, UK
- IEAP, Czech Technical University, Prague, Czech R.
- IFAE, Barcelona, Spain
- JINR, Dubna, Russian Federation
- NIKHEF, Amsterdam, The Netherlands
- University of California, Berkeley, USA
- University of Canterbury, Christchurch, New Zealand
- University of Geneva, Switzerland
- University of Glasgow, Scotland, UK
- University of Houston, USA
- University of Maastricht, The Netherlands
- University of Oxford, England, UK
- INFN, Italy
Pixel detectors ASICs developed by Medipix Collaborations

Transistor Density per pixel [Transistors/µm²] vs. CMOS process [nm]

- **Timepix4 (2019)**
- **Timepix3 (2013)**
- **Medipix3RX (2011)**
- **Timepix2 (2018)**
- **Medipix4 (2021)**
- **Timepix (2006)**
- **Medipix2 (2004)**
- **Medipix1 (1998)**
**Timepix3 → Timepix4**

Timepix4: A 4-side tillable large single threshold particle detector chip with improved energy and time resolution and with high-rate imaging capabilities.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>130nm – 8 metal</td>
<td>65nm – 10 metal</td>
</tr>
<tr>
<td><strong>Pixel Size</strong></td>
<td>55 x 55 µm</td>
<td>55 x 55 µm</td>
</tr>
<tr>
<td><strong>Pixel arrangement</strong></td>
<td>3-side buttable</td>
<td>4-side buttable</td>
</tr>
<tr>
<td><strong>Sensitive area</strong></td>
<td>1.98 cm²</td>
<td>6.94 cm²</td>
</tr>
<tr>
<td><strong>Readout Modes</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data driven (Tracking)</td>
<td></td>
<td><strong>TOT and TOA</strong></td>
</tr>
<tr>
<td>Event Packet</td>
<td>48-bit</td>
<td>64-bit</td>
</tr>
<tr>
<td>Max rate</td>
<td>0.43x10⁶ hits/mm²/s</td>
<td><strong>3.58x10⁶ hits/mm²/s</strong></td>
</tr>
<tr>
<td>Max Pix rate</td>
<td>1.3 KHz/pixel</td>
<td><strong>10.8 KHz/pixel</strong></td>
</tr>
<tr>
<td>Frame based (Imaging)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mode</td>
<td>PC (10-bit) and iTOT (14-bit)</td>
<td>CRW: PC (8 or 16-bit)</td>
</tr>
<tr>
<td>Frame</td>
<td>Zero-suppressed (with pixel addr)</td>
<td>Full Frame (without pixel addr)</td>
</tr>
<tr>
<td>Max count rate</td>
<td>~0.82 x 10⁹ hits/mm²/s</td>
<td>~5 x 10⁹ hits/mm²/s</td>
</tr>
<tr>
<td><strong>TOT energy resolution</strong></td>
<td>&lt; 2KeV</td>
<td>&lt; 1Kev</td>
</tr>
<tr>
<td><strong>Time resolution</strong></td>
<td>1.56ns</td>
<td><strong>195.3125ps</strong></td>
</tr>
<tr>
<td><strong>Readout bandwidth</strong></td>
<td>≤5.12Gb (8x SLVS@640 Mbps)</td>
<td>≤163.84 Gbps (16x @10.24 Gbps)</td>
</tr>
<tr>
<td><strong>Target global minimum threshold</strong></td>
<td>&lt;500 e⁻</td>
<td>&lt;500 e⁻</td>
</tr>
</tbody>
</table>
Timepix4 arrangement

- 512 x 448 of 55 x 55 µm pixels
  - 2 Matrices (TOP and BOTTOM)

- 3 peripheries with TSV (Through-Silicon-Vias):
  - TOP, BOTTOM (TSV, WB): Data Readout (16x 10.24 Gbps Serializers)
  - CENTER (TSV): Analog Blocks (DACs, ADC, Band-Gap...)

- On-chip bump to pixel redistribution layer (RDL):
  - Pixel matrix pixels are shorter (51.4 µm) than sensor pixels (55 µm)
  - Equalized Cin for all pixels $\rightarrow$ ~46 fF increase for a 460 µm periphery

- Edge peripheries include 1mm Wire Bond Extender

- Dicing options:
  - With WB (Wire-Bonds Extenders): 29.96 mm x 24.7 mm
    - >93.7% active area (28.16mm x 24.64mm)
  - Without WB (TSV Only) : 28.22 mm x 24.7 mm
    - >99.5% active area (28.16mm x 24.64mm)
  - Through Silicon Vias (TSV) requires post processing at wafer level to create TSV and on the ASIC back sides RDL + BGA pads
Timepix4 Bottom left detail

- **BOTTOM Matrix**
- **BOTTOM Periphery**
  - TSVs landing pads in M1
- **Dicing lane #1**
- **Dicing lane #2**
- **BOTTOM WB Extender**
Timepix4 Pixel Schematic

Front-end Analog

- Input pad
- TestBit
- 3fF
- ~50mV/ke
- 2.5fF
- Preamp
- MaskBit
- 5-bit Local Threshold
- Leak Current compensation

Global threshold

TpA TpB

Front-end Digital

- Counters & Latches
- Synchronizer & Clock gating

Counter & Latches

<table>
<thead>
<tr>
<th>Bits</th>
<th>ADDR</th>
<th>ToA</th>
<th>ufToAr</th>
<th>ufToAf</th>
<th>fToAr</th>
<th>fToAf</th>
<th>ToT</th>
<th>Pileup</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>9</td>
<td>16</td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>5</td>
<td>11</td>
<td>1</td>
</tr>
</tbody>
</table>

- VCO @640MHz
- Time stamp
- OP Mode
- Control voltage
- DataOut to EOC
- Clock (40MHz)
- 4 640MHz
- 8-bits
- 8-bits

SuperPixel

- Sync Readout
- 8-bits

SuperPixel Group

- ADB
- Clock local
- 8

1 pixel

8 pixels

32 pixels
Pixel Operation in TOA & TOT [DD]

- **Tpeak < 25ns**
- **Preamp Out**
- **Disc Out**
- **Clk (40MHz)**
- **Global TOA (16-bit)**
  - 65533
  - 65534
  - 65535
  - 0
  - 1
  - 2
  - 3
  - 4
- **VCO Clk (640MHz)**
- **TOA (16-bit)**
  - X
  - 65534
  - TOA (16 bits) = 65534
- **TOT Clk (40MHz)**
- **UFTOA_Start (4-bits)**
  - X
  - 0
- **UFTOA_Stop (4-bits)**
  - X
  - 8

**FTOA_R (5 bits) = 7**

**FTOA_F (5 bits) = 11**

**TOT (11 bits) = 4**

xavier.llopart@cern.ch
22nd iWoRID
Full digital double column DLL

[448 dDLL: 224 Top Matrix and 224 Bottom Matrix]

~22.7 mW/cm² to distribute a 40 MHz clock with a 100 ps_{rms}
Timepix4 Readout Modes: Data-Driven

- Zero-suppressed continuous data-driven
  - Output bandwidth from 40 Mbps (2.6 Hz/pixel) to 160 Gbps (10.8 KHz/pixel)
  - Uses Aurora 64b/66b standard encoding communication protocol

### SPEC: Packet specifications ToA/ToT

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>MSB</th>
<th>LSB</th>
<th>Bits</th>
</tr>
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<tbody>
<tr>
<td>Top</td>
<td>1</td>
<td>63</td>
<td>63</td>
<td>[63:63]</td>
</tr>
<tr>
<td>EoC</td>
<td>8</td>
<td>62</td>
<td>55</td>
<td>[62:55]</td>
</tr>
<tr>
<td>SP</td>
<td>6</td>
<td>54</td>
<td>49</td>
<td>[54:49]</td>
</tr>
<tr>
<td>Pixel</td>
<td>3</td>
<td>48</td>
<td>46</td>
<td>[48:46]</td>
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<tr>
<td>ToA</td>
<td>16</td>
<td>45</td>
<td>30</td>
<td>[45:30]</td>
</tr>
<tr>
<td>uToA_start</td>
<td>4</td>
<td>29</td>
<td>26</td>
<td>[29:26]</td>
</tr>
<tr>
<td>uToA_stop</td>
<td>4</td>
<td>25</td>
<td>22</td>
<td>[25:22]</td>
</tr>
<tr>
<td>fToA_rise</td>
<td>5</td>
<td>21</td>
<td>17</td>
<td>[21:17]</td>
</tr>
<tr>
<td>fToA_fall</td>
<td>5</td>
<td>16</td>
<td>12</td>
<td>[16:12]</td>
</tr>
<tr>
<td>ToT</td>
<td>11</td>
<td>11</td>
<td>1</td>
<td>[11:1]</td>
</tr>
<tr>
<td>Pileup</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>[0:0]</td>
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</tbody>
</table>

- Address: 18 bits
- Time: 29 bits

Energy: 21 bits
Timepix4 Readout Modes: Frame-based

• Full frame readout with continuous read-write (CRW):
  • 8-bits or 16-bit counter depth
  • Uses Aurora 64b/66b standard encoding communication protocol
  • Frame rate limited by bandwidth (and probably power):
    • **Required Readout bandwidth before counter overflow:**
      • 8-bit @ 1Gc/mm²/s > 20.48 Gbps
      • 16-bit @ 8Gc/mm²/s > 1.28 Gbps
    • **Minimum → Maximum Frame Rates:**
      • 8-bit 338 fps @ 40 Mbps → 86.5 Kfps @ 160 Gbps
      • 16-bit 169 fps @ 40 Mbps → 43.2 Kfps @ 160 Gbps

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>MSB</th>
<th>LSB</th>
<th>Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel 3/7</td>
<td>16</td>
<td>63</td>
<td>48</td>
<td>[63:48]</td>
</tr>
<tr>
<td>Pixel 2/6</td>
<td>16</td>
<td>47</td>
<td>32</td>
<td>[47:32]</td>
</tr>
<tr>
<td>Pixel 1/5</td>
<td>16</td>
<td>31</td>
<td>16</td>
<td>[31:16]</td>
</tr>
<tr>
<td>Pixel 0/4</td>
<td>16</td>
<td>15</td>
<td>0</td>
<td>[15:0]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>MSB</th>
<th>LSB</th>
<th>Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel 7</td>
<td>8</td>
<td>63</td>
<td>56</td>
<td>[63:56]</td>
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<tr>
<td>Pixel 6</td>
<td>8</td>
<td>55</td>
<td>48</td>
<td>[55:48]</td>
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<tr>
<td>Pixel 5</td>
<td>8</td>
<td>47</td>
<td>40</td>
<td>[47:40]</td>
</tr>
<tr>
<td>Pixel 4</td>
<td>8</td>
<td>39</td>
<td>32</td>
<td>[39:32]</td>
</tr>
<tr>
<td>Pixel 3</td>
<td>8</td>
<td>31</td>
<td>24</td>
<td>[31:24]</td>
</tr>
<tr>
<td>Pixel 2</td>
<td>8</td>
<td>23</td>
<td>16</td>
<td>[23:16]</td>
</tr>
<tr>
<td>Pixel 1</td>
<td>8</td>
<td>15</td>
<td>8</td>
<td>[15:8]</td>
</tr>
<tr>
<td>Pixel 0</td>
<td>8</td>
<td>7</td>
<td>0</td>
<td>[7:0]</td>
</tr>
</tbody>
</table>
Digital (dynamic) Power Consumption
[Data-Driven]

• Power consumption density is ~20 % less of Timepix3:
  • Digital power consumption 25% less
    • Improved clock distribution (dDLL)
    • 130nm → 65nm
  • Analog consumption is ~5% more
    • Minimize jitter → < 50ps
    • Compensate increase in input capacitance
**Timepix4 (November 2019)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size</td>
<td>55 x 55 µm</td>
</tr>
<tr>
<td>Array</td>
<td>512 x 448</td>
</tr>
<tr>
<td>Pixels</td>
<td>229376</td>
</tr>
<tr>
<td>aPLL</td>
<td>19</td>
</tr>
<tr>
<td>aDLL</td>
<td>16</td>
</tr>
<tr>
<td>10.24 Gbps serializers (Nikhef)</td>
<td>16</td>
</tr>
<tr>
<td>On-pixel VCO (Nikhef)</td>
<td>28672</td>
</tr>
<tr>
<td>dDLL Columns</td>
<td>448</td>
</tr>
<tr>
<td>Biasing DACs</td>
<td>13</td>
</tr>
<tr>
<td>ADC (IFAE)</td>
<td>1</td>
</tr>
<tr>
<td>Transistors in pixel</td>
<td>~6000</td>
</tr>
<tr>
<td>Transistors in chip</td>
<td>~1.5 bn</td>
</tr>
</tbody>
</table>
Timepix4 on Silicon

- First Timepix4 devices became available on the beginning of 2020 → chip debugging/characterization delayed by COVID19
- SPIDR4 readout system (Nikhef) used as a DAQ for initial chip debugging
- Testing of Timepix4 using the Wire Bond connections

Diced Timepix4 300mm wafer

Timepix4 with 4x300 µm (256x256) edgeless Si sensor (August 2020)

Timepix4 with full (512 x 448) Si sensor (March 2021)
Some mitigated degradation on pixels sitting on top of the active peripheral regions → doesn’t affect the required minimum threshold (500e-)

New version of Timepix4 should further improve the shielding on these areas

With a Si sensor the noise slightly increase ~3e- / pixel
Timepix4 equalization

< 35e⁻ rms

~450e⁻ rms

EQ: [368.52 2.34 (34.69e⁻)]
Equalization matrix
[PC24bit mode, e- collection high gain]

- All pixels responding (448x512)!
- 11 pixels masked
- No observable systematic across matrix
Gain slopes for different FE Gain

[TOA-TOT, ~200 pixels]

**Hole collection mode (VFBK=800mV)**

- LG
- LG-1sig
- LG+1sig
- HG
- HG-1sig
- HG+1sig
- LOG
- LOG-1sig
- LOG+1sig

**Electron collection mode (VFBK=500mV)**

- LG
- LG-1sig
- LG+1sig
- HG
- HG-1sig
- HG+1sig
- LOG
- LOG-1sig
- LOG+1sig

**Electron collection mode (VFBK=500mV)**

- Low gain mode
  - ~34.5 mV/ke-
- High gain mode
  - ~35.8 mV/ke-

**Hole collection mode (VFBK=800mV)**

- Low/LOG gain mode
  - ~20.5 mV/ke-
- High gain mode
  - ~34.5 mV/ke-
TOT Resolution [Data-Driven 1 pixel, average of 200 events/TP, HG e-]

TOT (Timepix3)

TOT-HD (Timepix4)
TOA Resolution
[TOA-TOT, 1 pixel, 10000 samples, HG e-]
Timexpix4 in Data-Driven mode
[Thr=800e- with ~120 pixels masked]

- Timeexpix4 running at 2 x 2.56 Gbps links: 77 MHits/s
- ~6.1M packets received without errors: ~610 KHits/s

10s $^{90}\text{Sr}$ source
Photon Counting reconstruction

Raw Data-Driven data
Previous data with 5ms time slices

Color coding indicates arrival time (TOA)
Timepix4 with 300 µm Si Sensor Full sensor
[CRW 16-bit Frame Based mode, Thr ~1 ke-]

- 2s acquisition X-ray source, Cu target @30kVp
- 20 Flatfield acquisition used for correction
- Excellent bumping! Only 6 unconnected pixels (99.997% good pixels)
Conclusions

• Timepix4 is the new particle-tracker and photon counting hybrid pixel detector designed with the support of the Medipix4 collaboration:
  • Large area hybrid pixel detector with 6.94 cm² sensitive area
  • 4-side buttable with <0.5% dead area
  • TOA: 23-bit dynamic range (1.6ms) with 195 ps LSB
  • TOT: 15-bit dynamic range with ~200 e- rms resolution
  • PC: 8-bit or 16-bit CRW up to 5*10⁹ hits/mm²/s
  • Readout: Up to 160 Gbps readout bandwidth
  • Very configurable architecture to accommodate a large number of different applications

• Next steps:
  • Different test beams planned to extract Timepix4 timing & energy resolution (MCP, LGADs,...)
  • Just submitted a Timepix4 mask change revision to further improve the pixel shielding on top of peripheral areas
  • First TSV devices by the end of 2021
  • Medipix4 submission scheduled by the end of 2021