

## Introduction

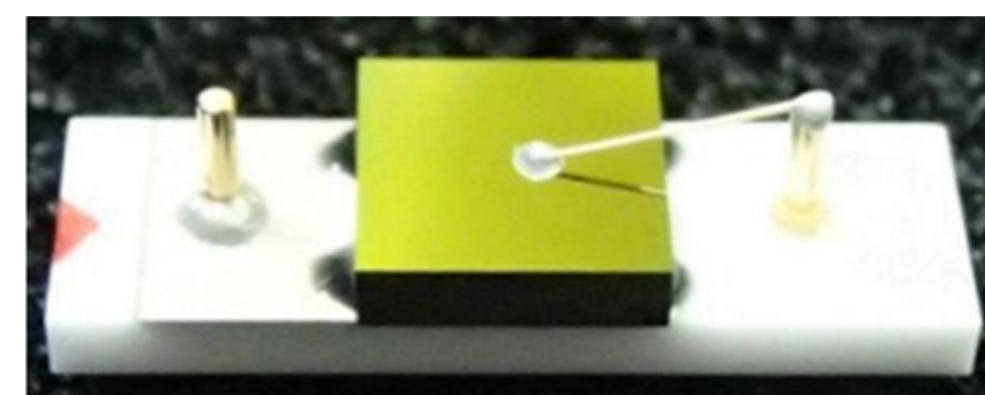
### ■ Spectral X-ray Photon-counting imaging

- Noise suppression
- Image quality
- Material discrimination

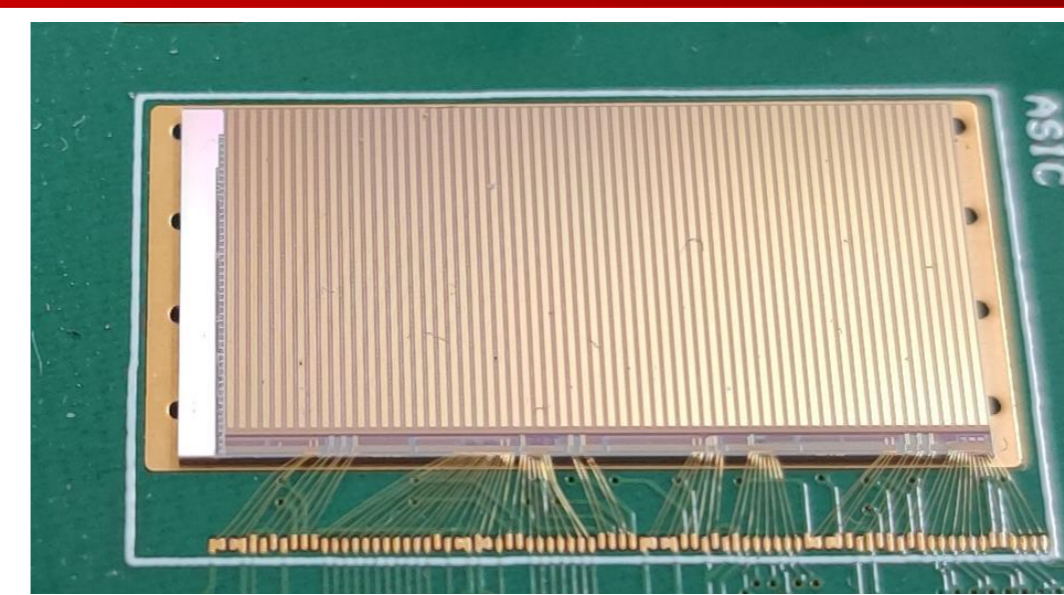
### ■ Cadmium Telluride(CdTe)

- High atomic number
- Proper band-gap energy
- Operational at room temperature
- Ideal for hard X-ray and gamma-ray detection

### ■ Pixelated readout ASIC

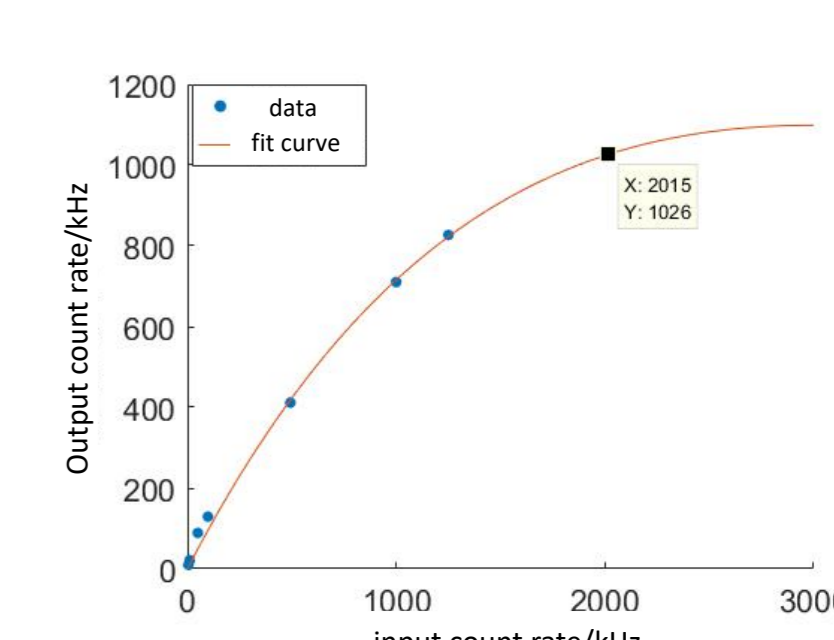
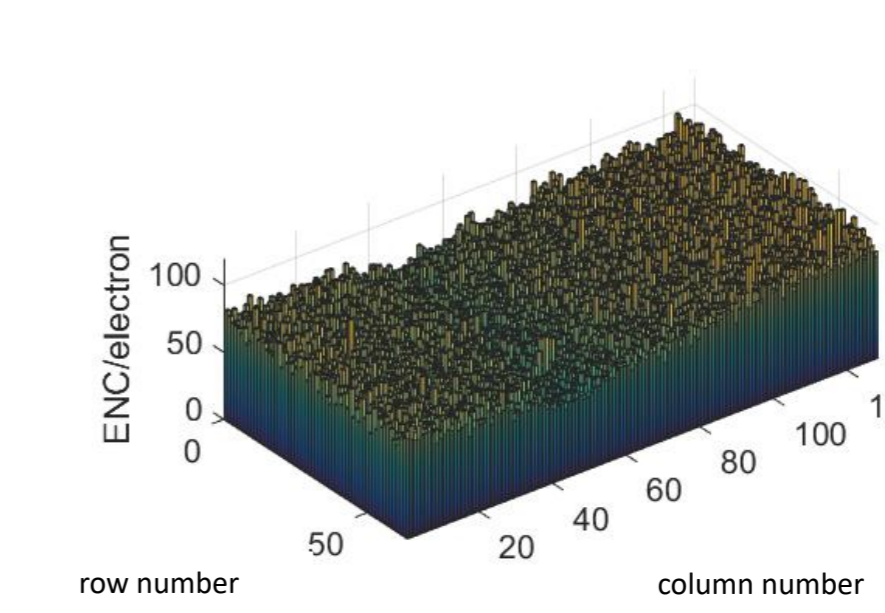
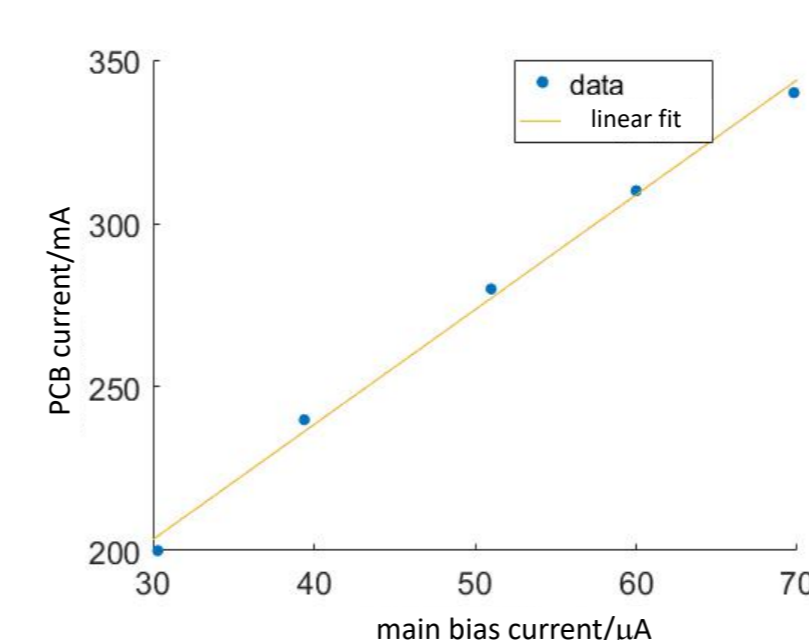


## Test Systems



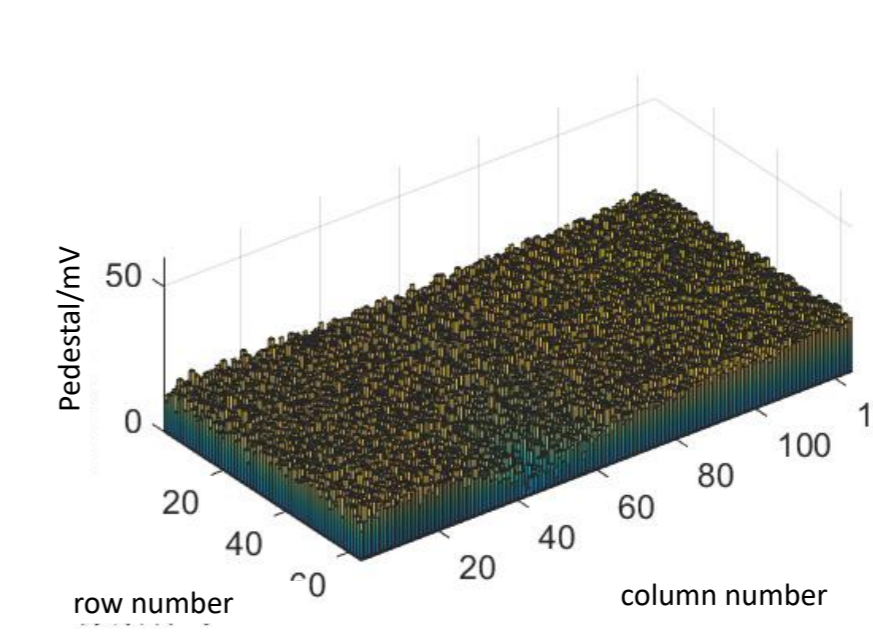
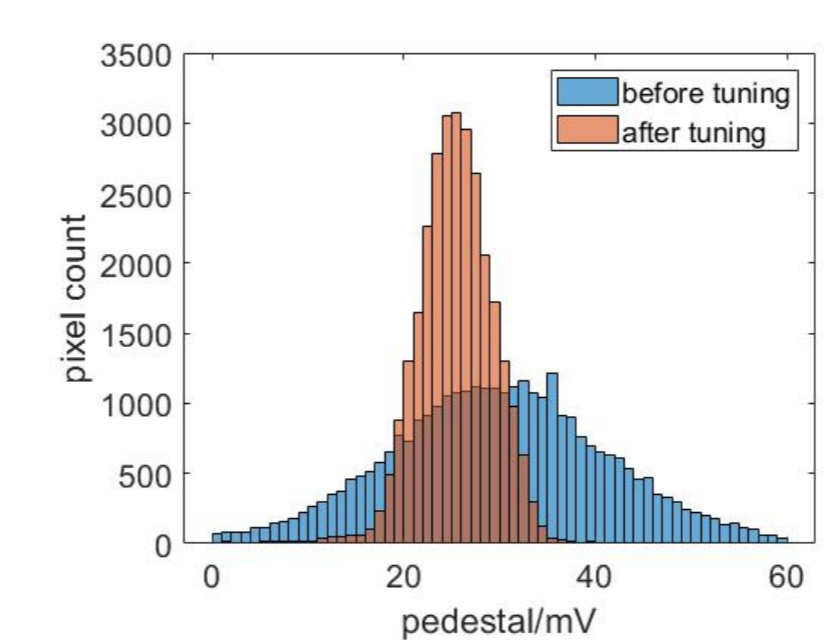
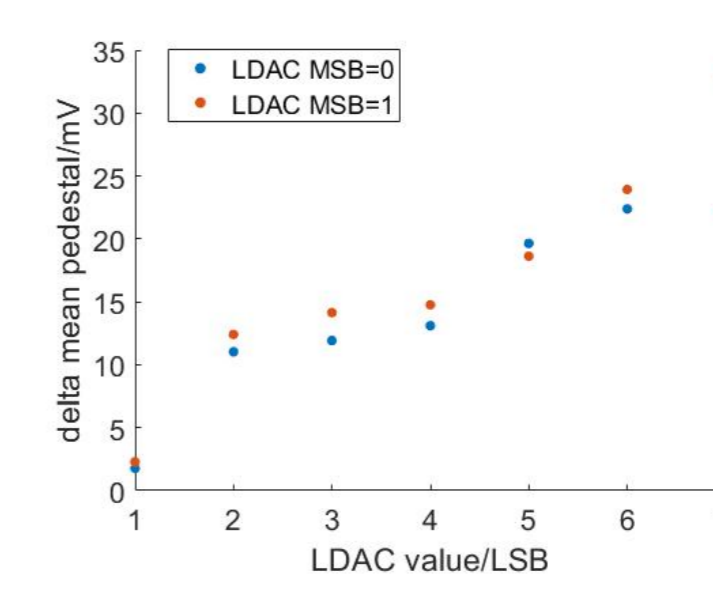
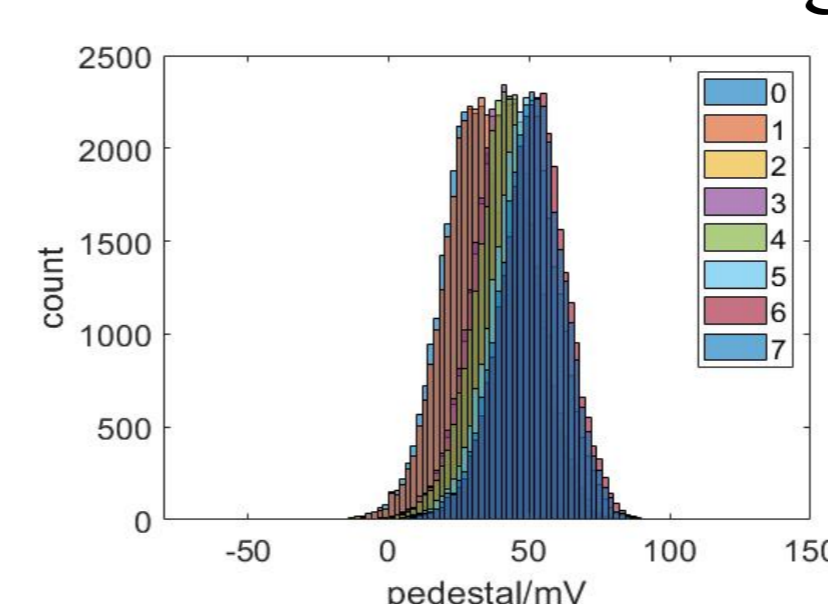
## Test Results

### ■ Electrical test results



- The power consumption is measured to be 60  $\mu$ W per pixel.
- The ENC in the worst case is measured to be less than 100 electrons.
- 2MHz input count rate (poisson distribution) is compatible.

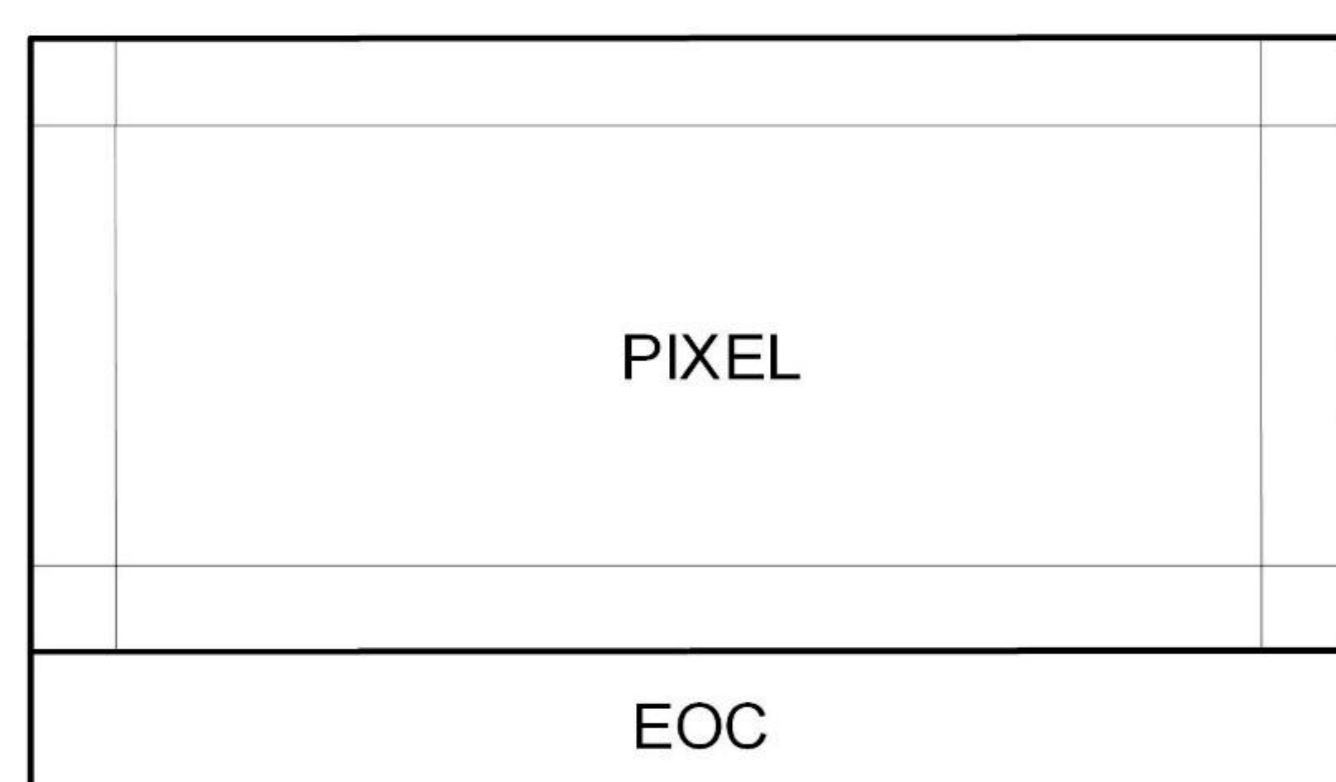
### ➢ Threshold tuning



- The threshold distribution of the pixel comparators can be measured by scanning global DAC values and the injected charge.
- The local DAC tuning step of each pixel can be obtained by scanning the local tuning DAC values and repeating the measurement of the corresponding threshold distribution.
- Proper local DAC tuning values of all the pixels can then be calculated according the tuning step-tuning DAC value table.
- The threshold distribution standard variation of all four comparators can be reduced from 10 mV to 3.5 mV.

## Architecture and Specification

### ■ Overall architecture



### ■ Main design specifications

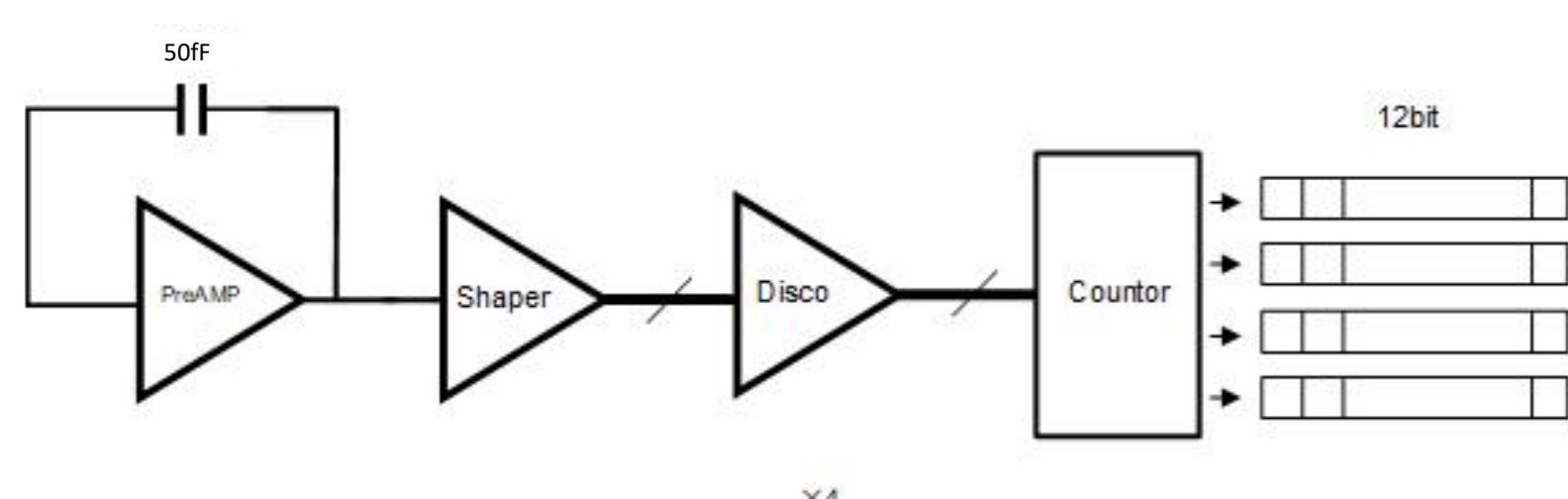
design specification	value
pixel size	150 $\mu$ m $\times$ 150 $\mu$ m
array	64 $\times$ 128
power consumption	100 $\mu$ W/pixel
gain	70 mV/fC
dynamic range	10 fC
ENC	<100e <sup>-</sup> @C <sub>in</sub> =100 fF
pulse width	200 ns
energy window	2/4
counter	24 bit/12 bit
readout frame rate	1 kHz

- the pixel array makes the majority of the ASIC;
- End-Of-Column(EOC) circuit is placed on the bottom so the chip is three-side buttable;

## ASIC Design

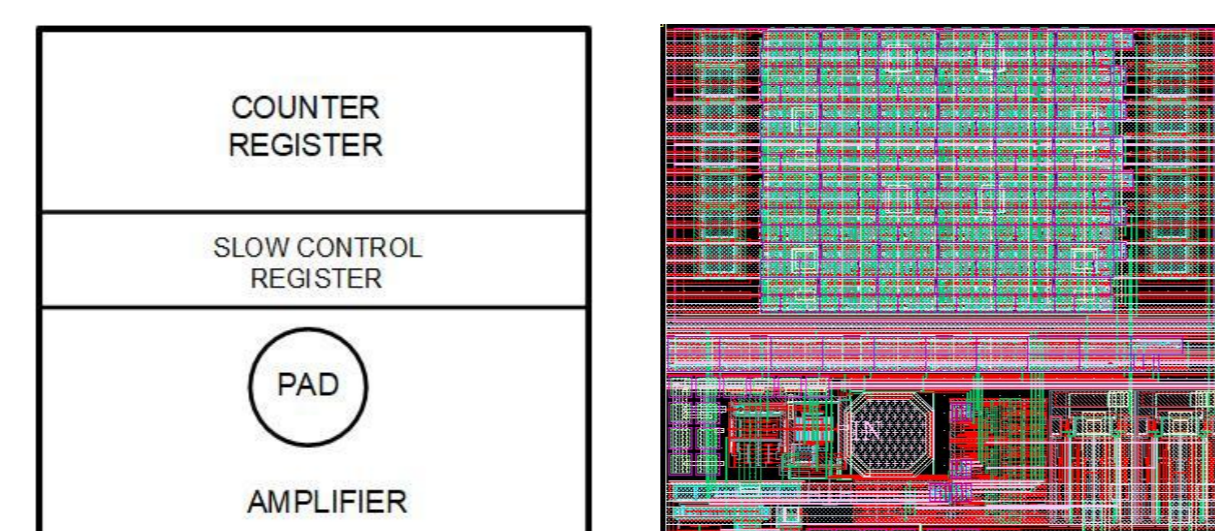
### ■ Pixel circuit

#### ➢ Block diagram



- One low-noise charge sensitive preamplifier
- One CR-RC shaper
- Four discriminators
- Four 12-bit counters
- Two operation modes

#### ➢ Layout

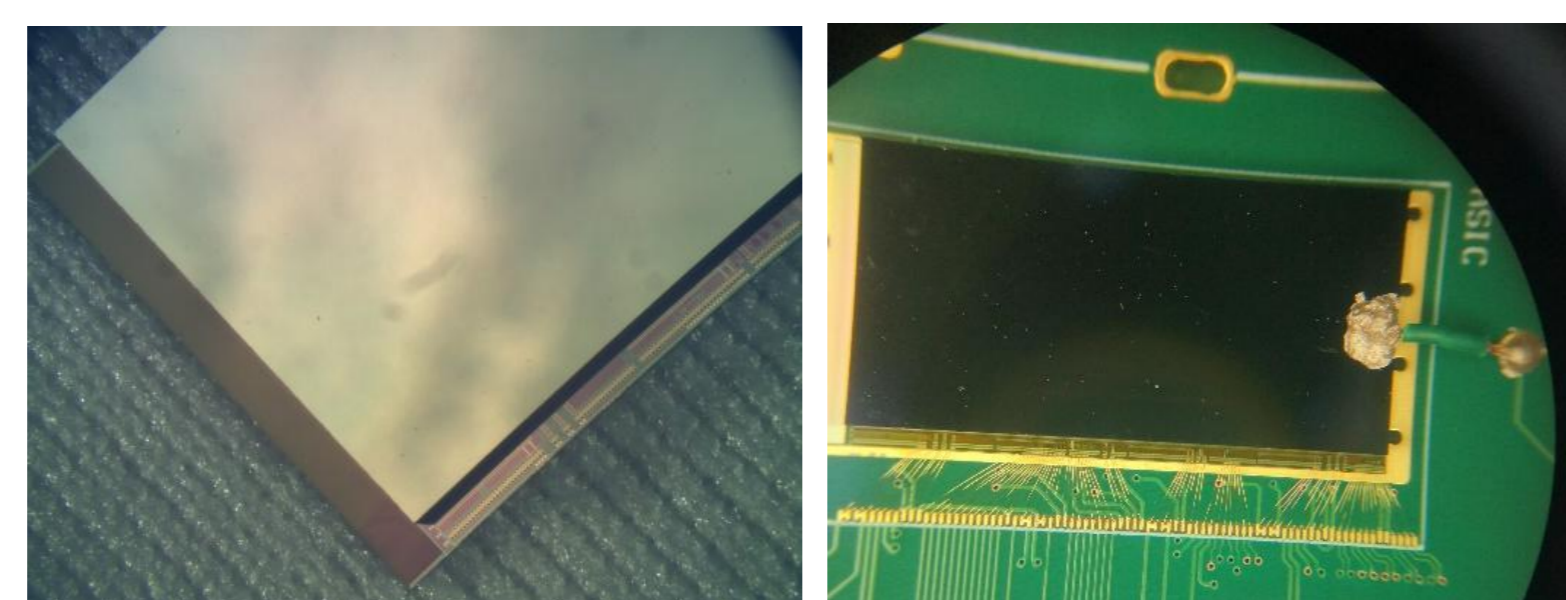
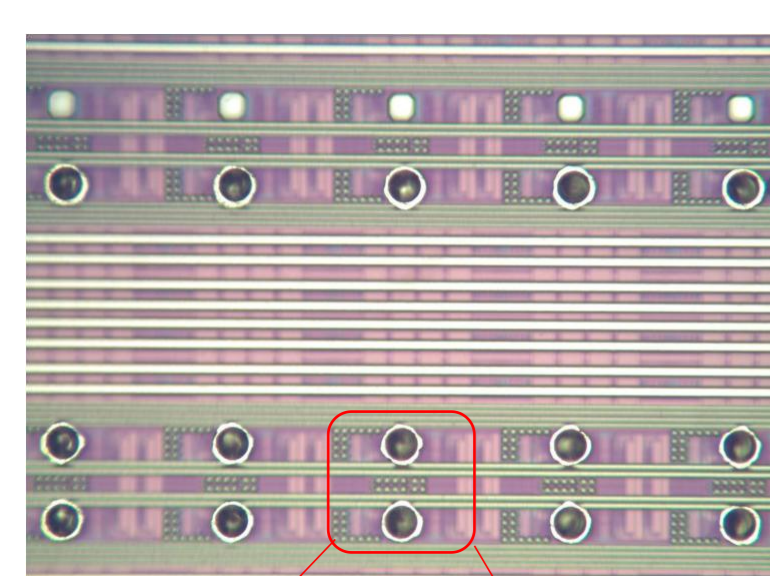


- The analog part and the digital part are divided by slow control registers to prevent digital interference inside the pixel
- Two adjacent columns of pixels are placed on symmetric arrangement to prevent digital interference outside the pixel

### ■ EOC circuit

- The EOC circuit contains bias generation, slow control and data readout control circuit.

## Module Assembly



Detector Parameter	Value
Area	19.515 mm x 9.915 mm
Thickness	1 mm
Electrode	Pt Ohmic/ Schottky

- CdTe semiconductor detectors are provided by Arcorad Corporation;
- Flip chip assembly service is provided by Polymer Assembly Technology;

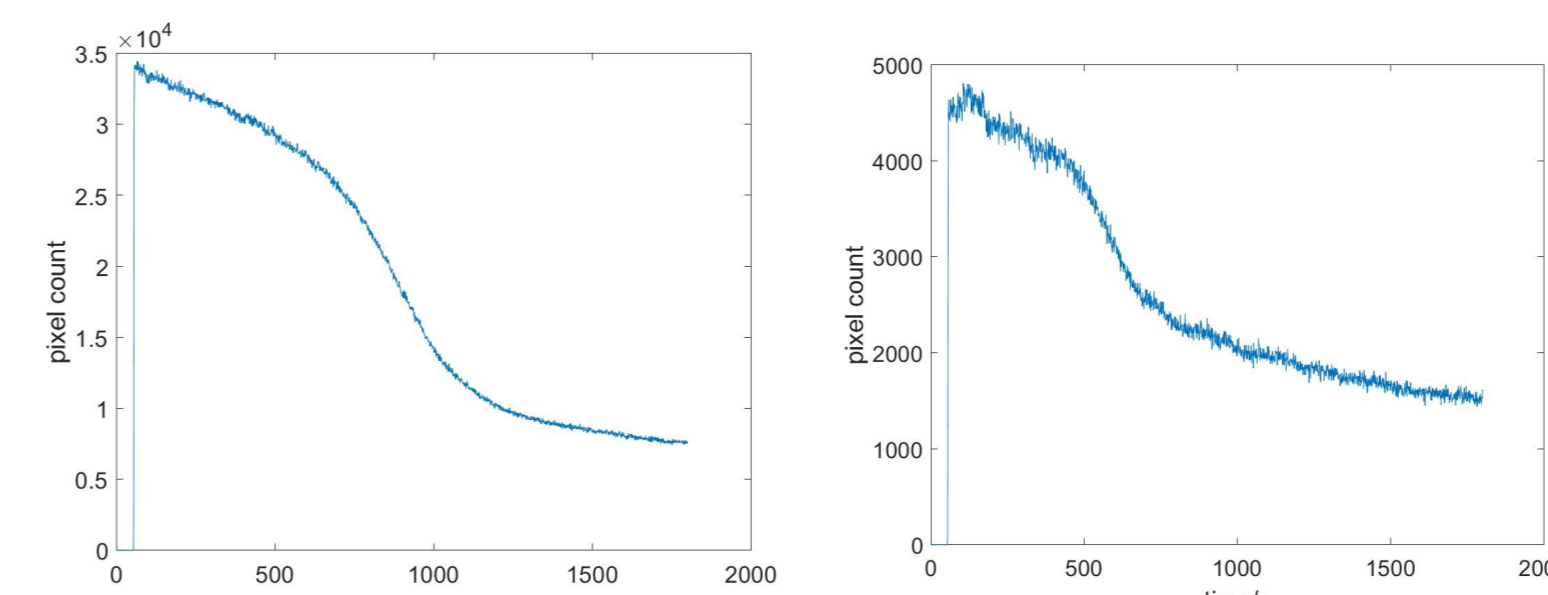
## Contact Information

Xuezhi Wang, PhD candidate, [wang-xz18@mails.tsinghua.edu.cn](mailto:wang-xz18@mails.tsinghua.edu.cn)

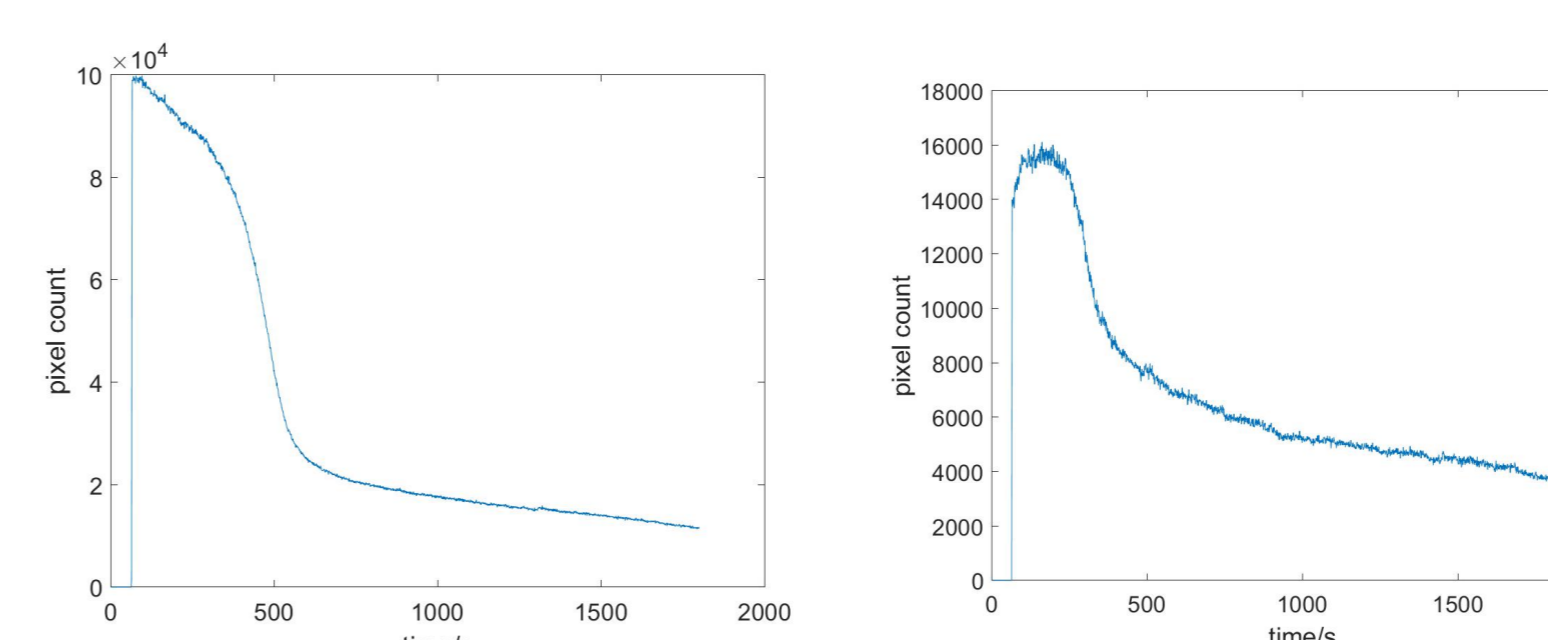
Zhi Deng, Associate Professor, [dengz@mail.tsinghua.edu.cn](mailto:dengz@mail.tsinghua.edu.cn)

### ■ Detector module test results

#### ➢ Polarization effect

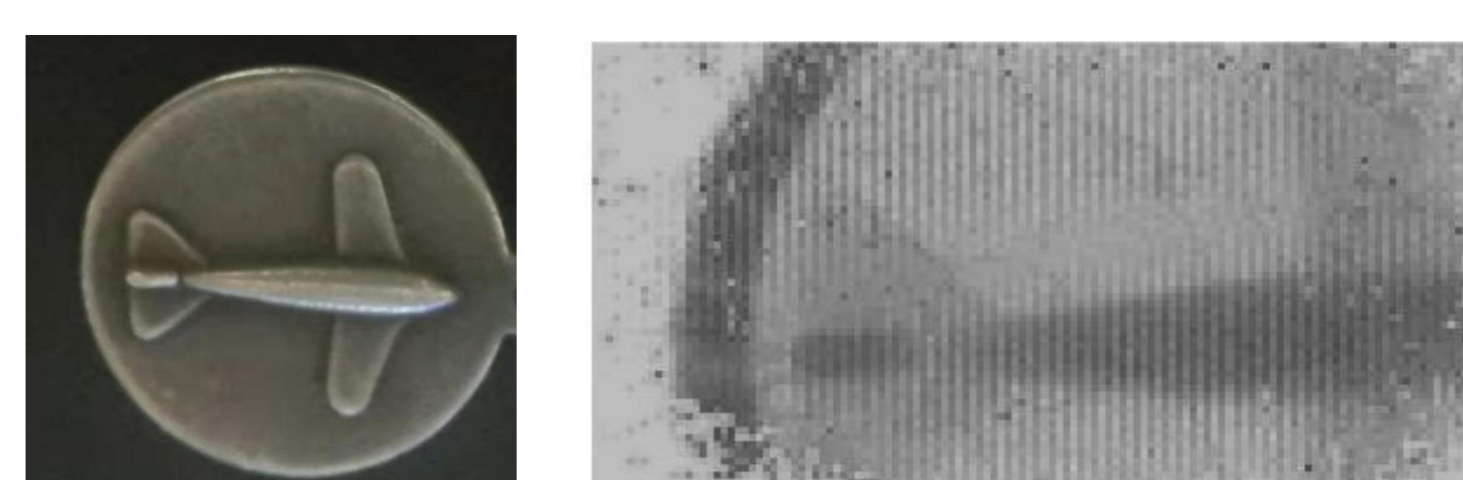


- The polarization effect can be observed.



- The detector tended to stabilize faster under higher count rate.

#### ➢ First imaging test



- The spatial uniformity of the detectors was analyzed.
- the flat field correction was conducted to improve image quality.

## Summary

- A pixelated photon-counting ASIC was developed. The prototype chip was evaluated.
- The detector module consisting of our prototype ASIC and the CdTe detector was tested and the imaging function was preliminarily verified.