Vernier Time-to-Digital Converter with Ring Oscillators for in-Pixel Time-of-Arrival and Time-over-Threshold Measurement in 28 nm CMOS

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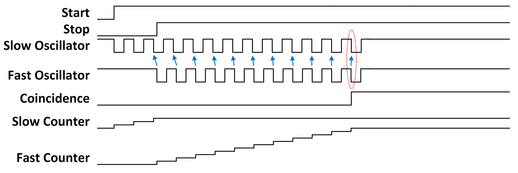
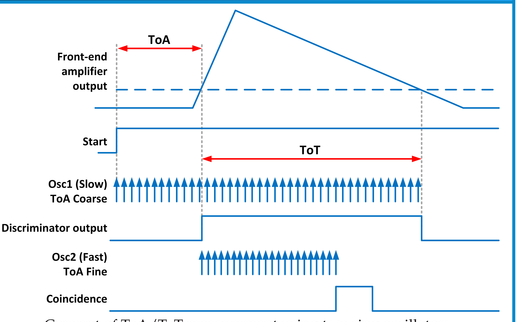
ToA/ToT measurement with high resolution

Hybrid pixel detectors for radiation imaging suitable for 3-D particle tracking and reconstruction offer the capability of high-resolution measurement of Time-of-Arrival (ToA) parameter. ToA is the amount of time between the discriminator first edge and the moment when the shutter closes. Possible applications include electron microscopy and antimatter research [1]. For example, 1.58 ns ToA accuracy of Timepix3 chip allowed for determining the parameters of antiproton annihilations [2]. Its precursors, GOSSIPO-3 and GOSSIPO-4 chips, offered TDC resolution on the order of 1.7 ns, and its successor, Timepix4 chip is planned to have 200 ps ToA resolution [3, 4, 5]. Timepix chips also include the possibility to measure Time-over-Threshold (ToT), which allows for indirect measurement of particle energy without the need to implement a separate ADC.

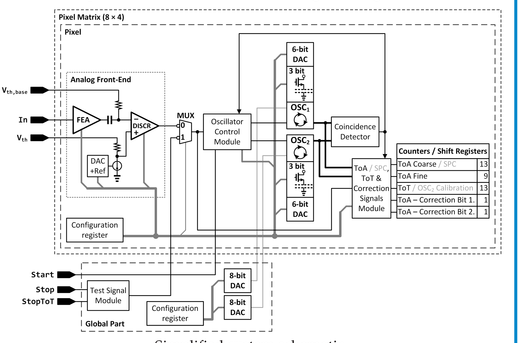
Our aim is to improve the ToA resolution further in nanometer technologies. This is a continuation of previous work on the development of readout integrated circuits for hybrid pixel detectors [6, 7, 8, 9]. Vernier TDC architecture with two ring oscillators may offer resolution even on the order of 5.1 ps and should be suitable for this project [10, 11]. Its operating principle is like the one of a caliper. Using two oscillators, slow and fast, whose frequencies slightly differ, a time resolution equal to the difference of their oscillation periods may be achieved.



We are introducing a chip prototype consisting of a matrix of 8x4 pixels with 50 μm pitch. Each pixel consists of analog front-end and digital part with two ring oscillators. Vernier TDC can process either the signal from the output of the discriminator or a signal generated from external Stop and StopToT signals. The chip may work in ToA/ToT mode or single photon counting (SPC) mode. Global and local DACs and capacitance banks are used to calibrate the oscillators' frequencies. Oscillators consist of three stages built from current-starved gates. IC is designed in 28 nm CMOS technology and is currently in fabrication.

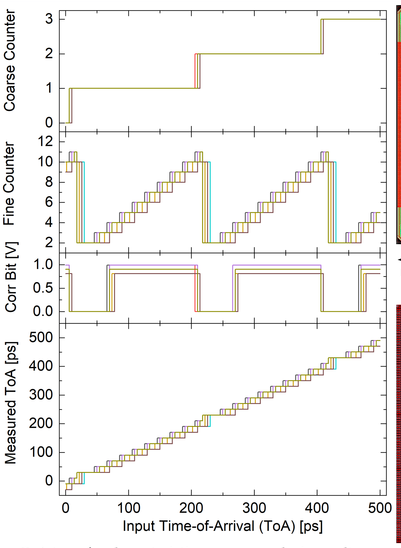


Concept of ToA/ToT measurement using two ring oscillators

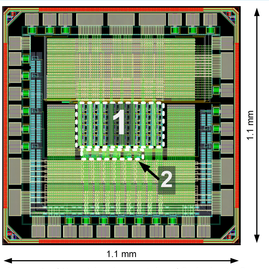


Simplified system schematic

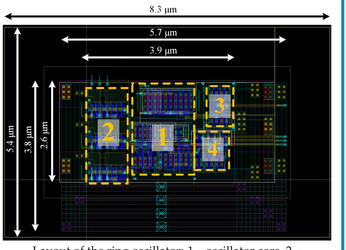
Chip Layout and Simulation Results



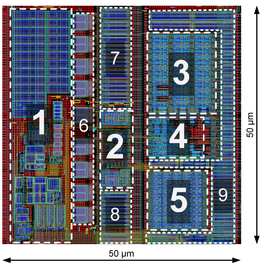
ToA transfer characteristics: corner analysis result



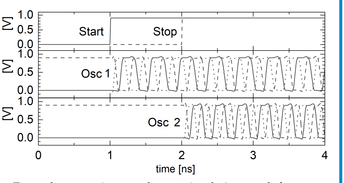
Layout of the chip: 1 – matrix of 8x4 pixels, 2 – global part



Layout of the ring oscillator: 1 – oscillator core, 2 – capacitance bank, 3 – enable signal buffer, 4 – skewed output buffers



Layout of the pixel: 1 – analog front-end and references, 2 – oscillators and trimming DACs, 3 – counters/shift registers, 4 – logic and coincidence circuit, 5 – configuration register, 6–9 – decoupling capacitors



Exemplary transient postlayout simulation result for two oscillators with slightly different frequencies

Conversion Parameters

TDC resolution T_{LSB} is equal to the difference between slow and fast oscillators' periods (T_{Slow} and T_{Fast}, respectively):

$$T_{LSB} = T_{Slow} - T_{Fast} \quad (1)$$

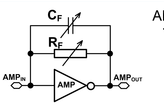
Conversion time t_{cmax} decreases with the increase of oscillators' output signal frequencies:

$$t_{cmax} \approx \frac{T_{Slow}^2}{T_{LSB}} \quad (2)$$

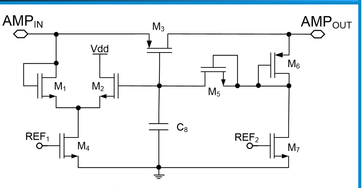
OSC$_1$ f_{Slow} [GHz]	OSC$_2$ f_{Fast} [GHz]	Coarse CTR [bits]	Fine CTR [bits]	OSC$_1$ T_{Slow} [ps]	OSC$_2$ T_{Fast} [ps]	T_{Range} [µs]	ToA T_{LSB} [ps]	ToA T_{Conv} [ns]	ToT T_{LSB} [ps]
1	1.02	13	6	1000	980	8.2	19.6	51.0	1000
2	2.08	13	5	500	481	4.1	19.2	13.0	500
3	3.19	13	5	333	313	2.7	19.9	5.6	333
4	4.34	13	4	250	230	2.0	19.6	3.2	250
5	5.55	13	4	200	180	1.6	19.8	2.0	200

Conversion parameters for several configurations of oscillator frequencies

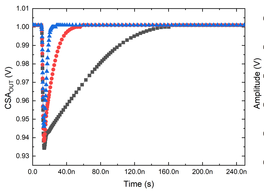
Analog Front-End Design



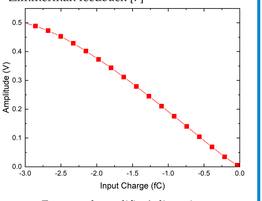
Inverter-based analog front-end



Zimmerman feedback [7]



Front-end amplifier's output response for different feedback settings



Front-end amplifier's linearity

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Bibliography

[1] R. Ballabriga *et al.*, "Asic developments for radiation imaging applications: The medipix and timepix family," *Nucl. Instruments Methods A*, vol. 878, pp. 10–23, 2018.
[2] N. Pacifico *et al.*, "Direct detection of antiprotons with the Timepix3 in a new electrostatic selection beamline," *Nucl. Instruments Methods A*, vol. 831, pp. 12–17, 2016, proceedings of the 10th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors.
[3] A. Kruth *et al.*, "GOSSIPO-3: measurements on the prototype of a read-out pixel chip for Micro-Pattern Gaseous Detectors," *J. Instrum.*, vol. 5, no. 12, p. C12005, 2010.
[4] F. Zappon *et al.*, "GOSSIPO-4: an array of high resolution TDCs with a PLL control," *J. Instrum.*, vol. 7, no. 01, p. C01081, 2012.
[5] R. Ballabriga *et al.*, "An introduction to the Medipix family ASICs," *Radiation Measurements*, p. 106271, 2020.
[6] P. Kmon *et al.*, "Design of analog pixels front-end active feedback," *J. Instrum.*, vol. 13, no. 1, p. P01018, Jan. 2018.
[7] P. Kmon *et al.*, "Active feedback with leakage current compensation for charge sensitive amplifier used in hybrid pixel detector," *IEEE Trans. Nucl. Sci.*, vol. 66, pp. 664–673, 2019.
[8] G. A. Carini *et al.*, "Hybridized MAPS with an in-pixel A-to-D conversion readout ASIC," *Nucl. Instruments Methods A*, vol. 935, pp. 232 – 238, 2019.
[9] L. A. Kadłubowski and P. Kmon, "Pomiar krótkich odcinków czasu z wykorzystaniem przetwornika czas-cyfra w architekturze verniera z oscylatorami pierścieniowymi w technologii CMOS 28 nm," *Przegląd Elektrotechniczny*, no. 12, pp. 115–118, 2020.
[10] N. Roy *et al.*, "Low power and small area, 6.9 ps RMS time-to-digital converter for 3-D digital SiPM," *IEEE Trans. Radiation Plasma Medical Sci.*, vol. 1, no. 6, pp. 486–494, Nov. 2017.
[11] F. Nolet *et al.*, "22 μW, 5.1 ps LSB, 5.5 ps RMS jitter Vernier time-to-digital converter in CMOS 65 nm for single photon avalanche diode array," *Electronics Letters*, vol. 56, no. 9, pp. 424–426, 2020.