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Vernier Time-to-Digital Converter with Ring Oscillators for in-Pixel Time-of-Arrival and Time-over-Threshold measurement in 28 nm CMOS

Hybrid pixel detectors for radiation imaging suitable for 3-D particle tracking and reconstruction offer the capability of high-resolution measurement of Time-of-Arrival (ToA) parameter. ToA is the amount of time between the discriminator first edge and the moment when the shutter closes. Possible applications include electron microscopy and antimatter research [1]. For example, 1.58 ns ToA accuracy of Timepix3 chip allowed for determining the parameters of antiproton annihilations [2]. Its precursors, GOSSIPO-3 and GOSSIPO-4 chips, offered TDC resolution on the order of 1.7 ns, and its successor, Timepix4 chip is planned to have 200 ps ToA resolution [3-5]. Timepix chips also include the possibility to measure Time-over-Threshold (ToT), which allows for indirect measurement of particle energy without the need to implement a separate ADC.

Our aim is to improve the ToA resolution further in nanometer technologies. This is a continuation of previous work on the development of readout integrated circuits for hybrid pixel detectors [6-8]. Vernier TDC architecture with two ring oscillators may offer resolution even on the order of 5.1 ps and should be suitable for this project [9,10]. Its operating principle is like the one of a caliper. Using two oscillators, slow and fast, whose frequencies slightly differ, a time resolution equal to the difference of their oscillation periods may be achieved. Figure 1 shows how two oscillators can be configured to measure ToA using Vernier method and ToT, gating the signal from the slow oscillator.

We are developing a chip prototype without an analog front-end that consists of Vernier TDC for in-pixel integration. Simplified schematic is shown in Figure 2. External Stop and StopToT signals represent the rising and falling edge of a discriminator, respectively. In normal mode, the slow oscillator (OSC1) is started by the Start signal, and the fast oscillator (OSC2) is started by the Stop signal. Global and local DACs and capacitance banks are used to calibrate the oscillators' frequencies. Oscillators consist of three stages built from current-starved gates (NAND gate for enable signal and two inverters). Signals for the counters (whose resolutions are given in the figure) are generated in the coincidence and counter control block. Additionally, two correction signals are generated to compensate the uncertainty of the moment when the coarse counter increments with respect to the fine counter. Figure 3 summarizes the exemplary configurations of oscillators' frequencies and counters' depths and the resulting range and resolution of ToA and ToT. Moreover, the maximum ToA conversion time T_{Conv} is estimated for each case. Currently, layout of the chip is under development. IC will be fabricated in 28 nm CMOS technology in the following months. Figure 4 presents the layout of one of the two ring oscillators with the capacitance bank.

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Figure. 1. Concept of ToA/ToT measurement using two ring oscillators.

Figure. 2. Simplified system schematic.

Figure. 3. Measurement parameters for several configurations of oscillator frequencies.

Figure. 4. Ring oscillator layout: (1) oscillator core with current starving, (2) capacitance bank, (3) enable signal buffer, (4) output buffers. Dimensions are given for three variants including transistor structures, supply wiring and separate N-well.

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