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An 8-bit low-power and small-area column-parallel ADC in the MAPS for beam imaging

To handle the increasing number of cancer patients, China has built its carbon ion therapy facility, in which the beam monitoring system ensures the beam energy deposition can accurately cover the dedicated tumor region. The full image of the beam energy deposition is needed for accurate beam calibration, thus a Monolithic Active Pixel Sensor (MAPS), which can provide the energy deposition in each pixel, is being designed in a 130nm CMOS process. As the key part in realizing full-image output, an 8-bit column-parallel ADC has been designed to serve the pixels in every four adjacent columns.

To satisfy the restricted constraints on power, size and speed, a novel structure has been designed. The sub-ADC generates 1.5-bit in each conversion step, which simplifies the circuits of the comparators and improves the tolerance to the offset of the reference voltage. The multiplying digital-to-analog converter (MDAC) is realized by only one amplifier and six capacitors. The amplifier is shared by the multiply-by-two circuit and sample-and-hold circuit. These actions significantly reduce the power consumption and chip area. Also, the MDAC reduces the conversion duration by combining the conversion phase and reset phase. The well-optimized timing for the switches also decreases the charge injection effect and eliminates the influence of charge left from the last conversion, which benefits the resolution.

Each column-parallel ADC covers a small area of 100μ m x 300 μm and consumes a low power of ˜5mW at 3.3V supply. Lab tests have been performed on the taped out column-parallel ADC array, the DNL and INL are measured to be 0.16/-0.18 LSB and 0.11/-0.10 LSB, respectively. The ENOB is measured to be 8.07bit at the sampling rate of 1MSPS and 6.63bit at the sampling rate of 5MSPS.

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