SparkPix-ED: a readout ASIC with 1 MHz frame-rate for rare event experiments at LCLS-II

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Motivation: from LCLS to LCLS-II...

Linear Coherent Light Source II:

- Second generation of X-ray Free Electron Laser @ SLAC
- Rep-rate: 1 MHz, evenly spaced
- Many novel detectors needed to meet science requirements
SLAC long-term X-ray detector development plan

Bigger, Faster, Higher resolution and Higher Energies

ePix (2013-2018)
• In use at LCLS

ePixHR (2016-2022)
• 5kHz for LCLS-II first light
• ePixHR10k for tender Imaging
• ePixM for soft Imaging

SparkPix (2020-2025)
• Revolutionary, experiment-specific X-ray Cameras
• Information extraction at full rate (1MHz CW, 3GHz burst)
• Advanced features:
  • Triggering
  • Sparsification
  • Zero suppression
  • etc…

ePixHR2.5D (2019-2025)
• Full frame 25kHz for HE first light
• Sensors for hard X-rays

ePixUHR (2019-2028)
• Full frame 100kHz-1MHz
• “General purpose” cameras
• Efficient information extraction
  (Advanced Calibration / Edge-ML)
SparkPix = ePix + information extraction engines

- ePix energy module
- timing module
- counting module
- full frame readout engine

SparkPix-S

- ePix energy module
- SparkPix Sparsification engine
SparkPix-ED: applications

Rare events in X-ray scattering experiments

- **Science case:** capture interesting events happening at random, stochastic times that make their observation difficult
- **Requirements:** record $N$ high-resolution images at closely spaced times around the rare event

Beam diagnostics

- **Science case:**
  - Analysis of the spectral content of the incident beam
  - Analysis of performance of beam kickers
  - Enable advanced modes of operations, e.g. beam dithering
- **Requirements:** pulse-by-pulse diagnostic tool at 1 MHz
1. Low-resolution images are continuously sent to the EDGE computing layer @ 1 MHz
2. $N$ images are continuously recorded in the detector in a ring-buffer
3. EDGE analyzes data for rare events and generates a trigger when one is detected
4. The trigger starts the readout of the high-res $N$ images recorded around the event
Operation modes

Fast trigger read-out: 1 MHz stream
- Sum signal of 9 pixels, resulting in a SuperPixel (SP) of 300*300 µm²
- Sum operation in analog domain reduces SNR by $\sqrt{9}$

High-resolution read-out
- The ring-buffers in each pixel are read-out
- Read-out rate: $1 \text{ MHz} / (N \times 9)$
- Read-out rate in 1st prototype: 25 kHz ($N=4$)
- Can be run in “CW imager” mode: 100 kHz
## Requirements

<table>
<thead>
<tr>
<th>Detector</th>
<th>ePixHR10k</th>
<th>SparkPix-ED</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mode</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pixel Pitch [um]</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>Frame rate [kHz]</td>
<td>7</td>
<td>100</td>
</tr>
<tr>
<td>Matrix size</td>
<td>192 x 144</td>
<td>&gt; 192 x 144</td>
</tr>
<tr>
<td>Read Noise [e(^{-}) rms]</td>
<td>75</td>
<td>100</td>
</tr>
<tr>
<td>Well depth [4keV photons]</td>
<td>&gt; 2\cdot10^4</td>
<td>10^4</td>
</tr>
<tr>
<td>Power consumption [W/cm(^2)]</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Data rate [Gb/s]</td>
<td>3</td>
<td>44</td>
</tr>
<tr>
<td>CMOS tech node [nm]</td>
<td>250 nm</td>
<td>130 nm</td>
</tr>
</tbody>
</table>

### Many design challenges:

- Pixel operation from \(~7\) kHz → 1 MHz
- Maintain similar noise performance, linearity, dynamic range, power
- ADCs and digital logic distributed across pixel matrix, in the same die

\[*\] 10^5 assuming photons are equally distributed over 9 pixels
Integration and read-out phases are pipelined
Circular buffers act as local memory, storing $N$ images ($N=4$ in the first prototype).
Final memory depth t.b.d. based on estimated trigger latency ($\sim 10 \, \mu s$)
Fast-trigger path: signal sent to summing node, in parallel with memory write
Optimized gain-switching circuitry:
  • Correlated pre-charging $\rightarrow$ reduce excess noise after gain switching [1]
  • Current-mode gain switching $\rightarrow$ fast switching in presence of large input signal

## Overall architecture

### Pixel
- 100x100 µm
- Operates at 1 MHz
- CW mode: 100 kHz
- Stores N high-res images

### Super-Pixel
- 300x300 µm
- Sum signal from 9 pixels
- Controls gain switching of individual pixels

### Cluster
- 600x1200 µm
- 8 Super-Pixels → 1 ADC
- Sampling rate: 8 MSPS
- Digital logic for pixel configuration and readout

### ASIC
- 2400x2400 µm
- ASIC Balcony includes:
  - Analog biasing
  - Digital read-out logic
  - Fast transmitters

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**ePixHR back-end LVDS out**

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<th>Cluster</th>
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**Operates at 1 MHz**

**CW mode: 100 kHz**

**Stores N high-res images**

**Sum signal from 9 pixels**

**Controls gain switching of individual pixels**

**8 Super-Pixels → 1 ADC**

**Sampling rate: 8 MSPS**

**Digital logic for pixel configuration and readout**

**ANALOG BALCONY**

**Digital logic for pixel configuration and readout**

**Fast transmitters**
Cluster ADC

Hybrid Successive Approximation Register (SAR) topology

- 12b @ 8 MSPS
- Small area:
  - 8b CDAC + 4b RDAC
  - First prototype with MIM and MOM caps to study matching
- Power efficient:
  - VCM based switching scheme
  - Dynamic latched comparator with preamplification
- Large number of ADCs in matrix:
  - built-in ADC reference [1]
- Area: 200x600 µm²

SparkPix-ED: 1\textsuperscript{st} prototype

First ASIC submitted in December 2020 features:

- Re-distribution of pixel inputs on-ASIC
  - No need for dedicated Si sensor
- 4 \textit{in-pixel} memories
  - 4 µs total “available latency” for triggering
- ASIC takes ~2 µs from integration to serialization
- 2 µs left for FPGA to analyze image stream at 1 MHz and send a readout trigger to the ASIC
  - Can prove the concept with 1\textsuperscript{st} prototype
  - Memory depth in final version will depend on the algorithms running in EDGE layer
Preliminary results

Demonstrated:
- Charge injection at pixel input
- Gain switching in both modes
- Hi-resolution mode @ 100 kHz
- Fast-sum mode @ 1 MHz
- Trigger on the FPGA to close the loop and prove the concept
- Event-driven (triggered) read-out

On-going measurements:
- Noise
- Linearity
Videoss

**Sum: 1 MHz**

Charge injected with calibration pulse every 10 frames

**Hi-res: 0.1 MHz**
Trigger mode

ASIC

... 

FPGA

Trigger condition: >20 pixels in low-gain

DAQ

Fast images not stored (data reduction)

Switch to memories readout

Inject at frame 8

Triggered on frame 8

Frame 6

Frame 7

Frame 8

Frame 9
Conclusion

Next steps:
- Characterize performance with Si sensor
- Development of ~5 Gb/s IOs has started → scale up to full-reticle ASIC
- Evaluate latency of EDGE computing layer algorithms → tune memory depth
- Leverage SparkPix-ED blocks to develop ePixUHR
  - Optimize for “CW” operation at 100 kHz / 1 MHz

The SparkPix-ED team:

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PIs
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