Development of an On-Chip Data Transmission Link for Monolithic Active Pixel Sensor

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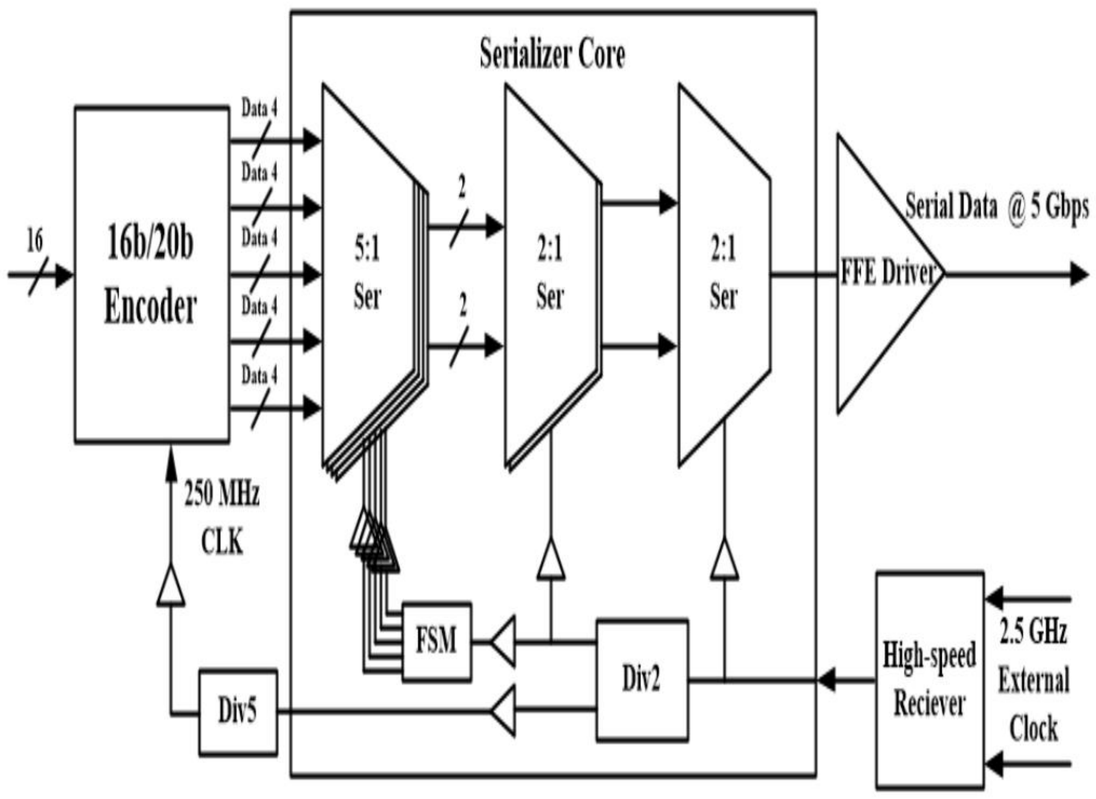

Figure 1 The architecture of the whole data transmission link

Introduction

The development of CMOS pixel detector technology provides an unprecedented signal-to-noise ratio, spatial resolution, material budget, and readout speed for vertex and tracking detectors in particle experiments [1]. The commonly used CMOS pixel detector is the Monolithic Active Pixel Sensor (MAPS), which collects the charge deposited by the particles that pass through the detector.

The data transmission link is a key part of the MAPS. Thus a 5Gbps on-chip data transmission link has been designed for Monolithic Active Pixel Sensor (MAPS). The link converts the parallel data from the column ADCs into high-speed serial data and accomplishes the data transmission. The serial link is designed in a commercial 130nm CMOS technology with the power supply of 1.2 V. The architecture of the whole data transmission link is shown in Fig.1. It consists of a 16b/20b encoder, a 20:1 serializer, a Feed Forward Equalization (FFE) driver, and a high-speed receiver to deal with the external clock. Aiming to reduce the working frequency, the 16b/20b encoder has been designed in a parallel coding structure. The customized multi-level structure in the serializer core guarantees the timing margin between the data and the clock. The FFE driver is designed to drive the serial transmission via low mass cables. The data link is also compatible with MAPS with the data rate lower than 5Gbps. The power consumption of the whole data transmission link is 51 mW. This paper will discuss the design and performance of the data transmission link.

16b/20b Encoder Design

The parallel encoder apparatus includes an upper encoder and two lower 8b/10b encoders. The upper encoder has an upper encoded output and a corresponding upper running disparity. The two lower encoders generate lower encoded outputs synchronously using different running disparity state. A multiplexer multiplexes the two lower encoded outputs based on the upper running disparity. This parallel encoder structuer can achieve wider data paths with lower clock rate.

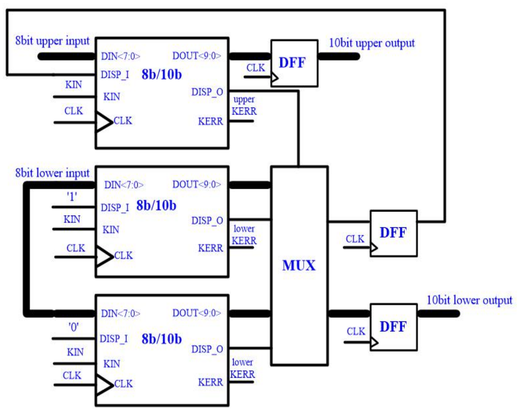

Figure 2 The structure of 16b/20b encoder

20:1 Serializer Design

The 20:1 serializer uses four 5:1 multi-phase structures as the first stage, the second and the last stage employ 2:1 tree structures. At the first stage, the input data rate is 250 Mbps for each parallel channel, and the sampling clock is 1.25 GHz provided by finite state machine(FSM).
In order to provde three taps for FFE driver, the last stage adopts a more complicated 2:1 tree structure than the second stage[2]. This structure working at 2.5 GHz clock, provides a complementary signal and it is copid with one and two bit-period delay to FFE driver. The three taps of differential outputs are controled by NOR gates.

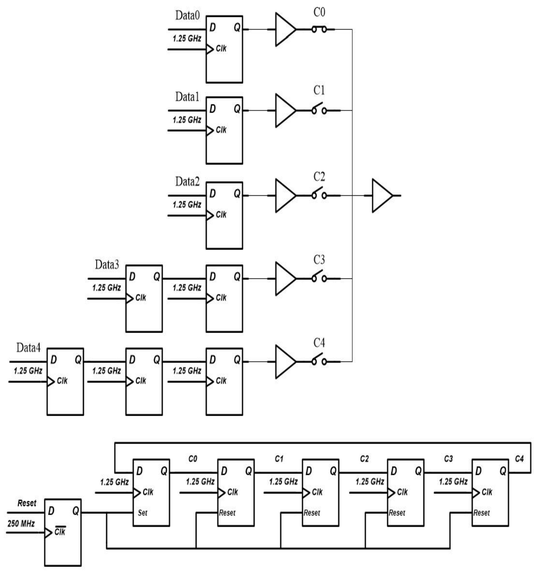

Figure 3(a) The first stage of the serializer

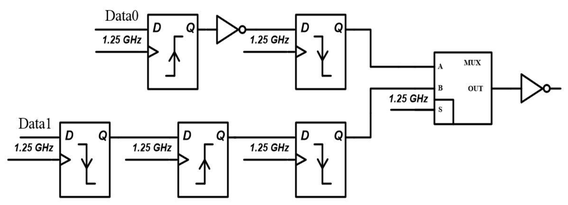

Figure 3(b) The second stage of the serializer

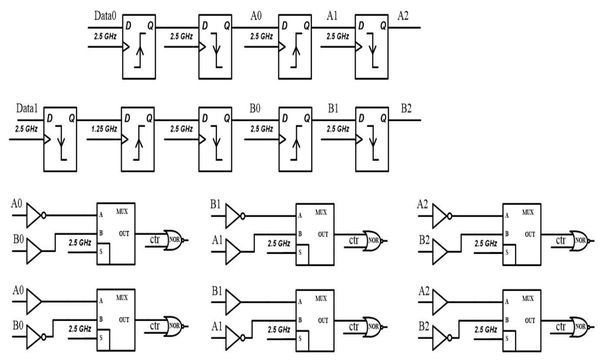

Figure 3(c) The last stage of the serializer

FFE Driver Design

The FFE driver follows conventional designs[3] with two 50-Ω pull-up resistors as the load and the termination. The tail current sources of the driver are programmable via digital slow control module. By tuning the tail current sources, the total current of the FFE driver are a constant of 16 mA to a maximum swing of 400 mV. The maximum pre-emphasis can reach 6 dB.

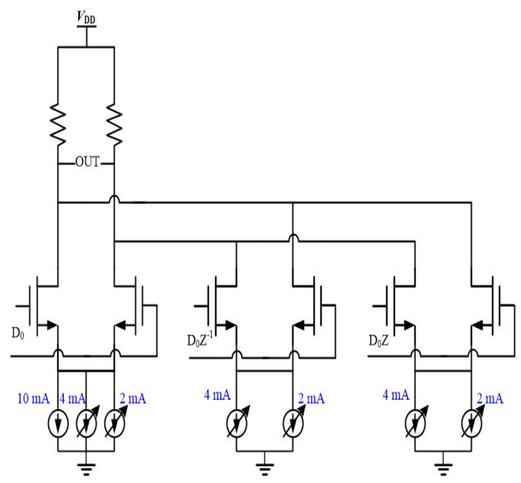

Figure 4 The structure of FFE driver

The Chip Die Layout

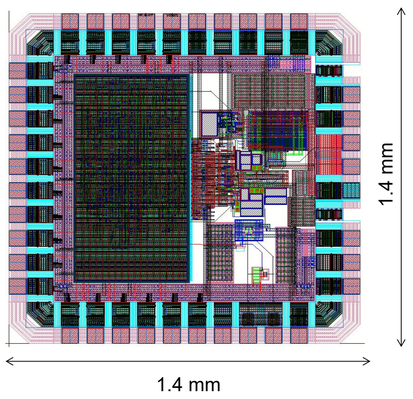

Figure 5 The die layout of the data transmission link

Post-layout Results

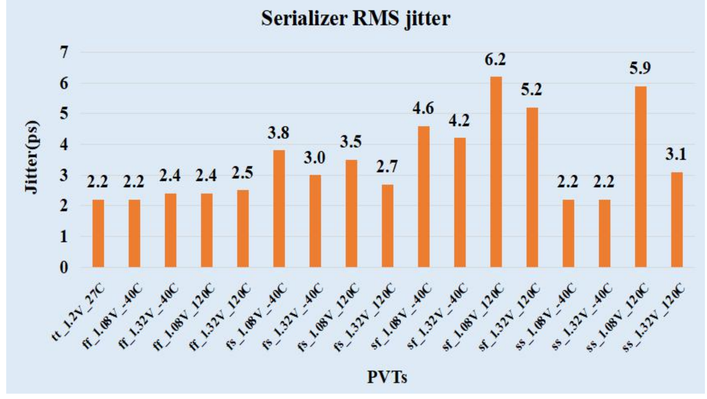

Figure 6(a) The RMS jitter of the serializer under different PVTs

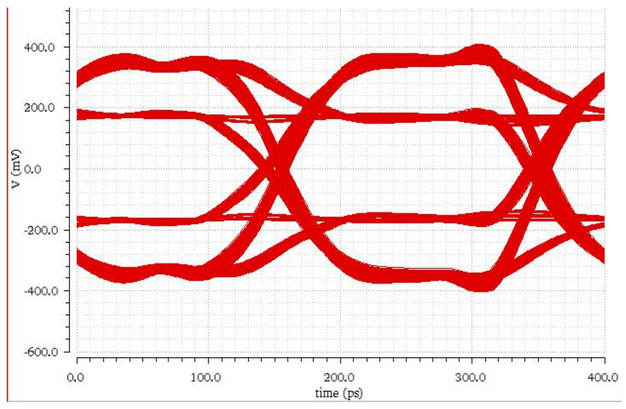

Figure 6(b) Eye diagrams with a 6 dB pre-emphasis at the typical case

Acknowledgments

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