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## Development of an On-Chip Data Transmission Link for Monolithic Active Pixel Sensor

The development of CMOS pixel detector technology provides an unprecedented signal-to-noise ratio, spatial resolution, material budget, and readout speed for vertex and tracking detectors in particle experiments [1]. The commonly used CMOS pixel detector is the Monolithic Active Pixel Sensor (MAPS), which collects the charge deposited by the particles that pass through the detector.

The data transmission link is a key part of the MAPS. Thus a 5Gbps on-chip data transmission link has been designed for Monolithic Active Pixel Sensor (MAPS). The link converts the parallel data from the column ADCs into high-speed serial data and accomplishes the data transmission. The serial link is designed in a commercial 130nm CMOS technology with the power supply of 1.2 V. The architecture of the whole data transmission link is shown in Fig.1. It consists of a 16b/20b encoder, a 20:1 serializer, a Feed Forward Equalization (FFE) driver, and a high-speed receiver to deal with the external clock. Aiming to reduce the working frequency, the 16b/20b encoder has been designed in a parallel coding structure. The customized multi-level structure in the serializer core guarantees the timing margin between the data and the clock. The FFE driver is designed to drive the serial transmission via low mass cables. The data link is also compatible with MAPS with the data rate lower than 5Gbps. The power consumption of the whole data transmission link is 51 mW. This paper will discuss the design and performance of the data transmission link.

**Authors:** Prof. ZHAO, Chengxin (Institute of Modern Physics, CAS); Dr YANG, Ping (Central China Normal University); Dr ZHOU, Wei (Institute of Modern Physics, Chinese Academy of Sciences); Dr NIU, Xiaoyang (Institute of Modern Physics, Chinese Academy of Sciences); Dr WANG, Yao (Institute of Modern Physics, Chinese Academy of Sciences); Mr WANG, Qilin (Institute of Modern Physics, Chinese Academy of Sciences)

**Presenter:** Dr ZHOU, Wei (Institute of Modern Physics, Chinese Academy of Sciences)

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