

AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

8 b 10 MS/s Differential SAR ADC in 28 nm CMOS for Precise Energy Measurement

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Motivation

- Possible Approach
- Proposed Solution

Designed ADC

- Requirements
- Comparator and Offset Calibration
- Chip Layout
- Measurements
- Summary
- Future Plans



Why is X-ray imaging so popular	2 and more energies
 Availability 	 Contrast enhancement
 Low cost 	 Easier material identification
 High spatial resolution 	Some difficulties in medicine
 Fast acquisition 	 Multiple expositions imply
Exemplary applications	higher dose
 Crystallography 	 Take additional time
Medicine	Patient movements between
Industry	degradation
 Airport security 	
•	(McCollough et al., 2015)

(Ballabriga et al., 2020) Kaczmarczyk, Kmon (AGH UST) 8

8 b 10 MS/s Differential SAR ADC in 28 nm CMOS ...



Colorful (multienergy) scan

- All data is collected during a single exposition
- A hybrid single photon counting detector is applied
- Photons are "binned" according to their energy



Figure: Binning of detected x-rays into six energy windows (McCollough et al., 2015)



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- Usually 2–4 discriminators
- Each for one energy level
- Globally set thresholds
- e.g.: 4 energy levels in MPIX (Gryboś et al., iWoRiD 2021) 8 energy levels in Medipix3RX (Ballabriga et al., 2013)



Figure: Simplified readout channel of an *N*-energy levels detecting system



- 2^{bits} energy levels recognition
- No information about the intensity stored in ASIC

e.g. 8b in ERPC (Meng et al., 2009)



Figure: Simplified readout channel with an ADC



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Figure: Proposed pixel readout channel of an 2^N -energy levels detector

- Discriminator for triggering the ADC and cutting off the background noise
- 2^N energy levels recognition
- Counters store both intensity and energy of incoming photons (energy spectrum)
- SAR architecture seems to be a reasonable choice
 - Iow power consumption
 - sufficient conversion rate possibilities

(Peizerat et al., 2017)



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Figure: Simplified ADC architecture with a serial output register

Table: General specification for X-ray imaging and computed tomography (Anastasio and La Riviere, 2012)

Count rate	Pixel pitch	Energy range
$Gcps/mm^2$	μm	keV
0.05	typ. 85	28-40
0.001-0.5	typ. 150	70-120
1	55-1000	80-140
	Count rate Gcps/mm ² 0.05 0.001-0.5 1	Count rate Pixel pitch Gcps/mm ² μm 0.05 typ. 85 0.001-0.5 typ. 150 1 55-1000

- 8 bits
- 10 MS/s
- Differential
- CMOS 28 nm
- $V_{DD} = 1 V$



- Limited power
 - Dynamic comparator (van Elzakker et al., 2010)
- Limited area
- Small capacitive DAC
- Small unit capacitance
 - Custom MOM Cunit=0.5 fF
- Small input pair dimensioning
- Higher input offset voltage
 - Time-domain offset compensation (Yang et al., 2019)



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Classical Compensation Methods

- Increasing input pair dimensions
- Additional node capacitance

- Area increase
- Power increase
- Speed decrease





(Kaczmarczyk and Kmon, 2020)

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Figure: Mesurement setup



Figure: PCB front



Figure: PCB back



Figure: Setup connections

Measurements: Static Parameters – Single IC





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Measurements: Static Parameters – Summary

	INL _{min}	INL _{max} DNL _{min}		DNL _{max}
	LSB	LSB	LSB	LSB
Chip 1	-0.23	0.41	-0.24	0.14
Chip 2	-0.39	0.46	-0.33	0.11
Chip 3	-0.49	0.63	-0.41	0.13
Chip 4	-1.05	0.67	-0.23	0.13
Chip 5	-0.31	0.36	-0.23	0.17
Chip 6	-0.33	0.31	-0.26	0.11
Chip 7	-0.25	0.21	-0.23	0.14
Chip 8	-0.81	0.63	-0.26	0.23
Mean	-0.48	0.46	-0.27	0.15





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- We have designed and tested the 8-bit differential SAR ADC in 28 nm CMOS node
- Time-domain offset compensation has been positively evaluated
- The core size, sampling frequency and power consumption allows for placement in a small pixel enabling energy-resolved imaging

	INL	DNL	Area	Cunit	$\mathbf{f}_{\mathbf{s}}$	ENOB	Power	Other
	LSB	LSB	μm^2	fF	MS/s	bits	μW	
This work	<0.5	<0.3	30×60	0.5	9.1	>7	~45	SAR with offset compensation in time
(Meng et al., 2009)	?	?	in 350 \times 350 pixel	?	0.4	?	390 per whole pixel	TDC and 4 to 8-bit DAC
(Peizerat et al., 2017)	?	?	$\sim 250{\times}250$?	10	?	10 000 per whole pixel	8-bit SAR ADC



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- The area occupancy can still be decreased by reducing the unit capacitance (here 0.5 fF), or by applying another switching scheme and changing the capacitor array.
- Power can be saved by getting rid of the clock and applying self-clocking logic.
- Offset calibration would be more efficient when implemented with capacitively delayed buffers instead of supply regulation.
- Linearity can be improved by replacing the input transition gate with a bootstrap switch.



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Thank you for your attention

Questions are welcome

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