Contribution ID: **206** Type: **Oral presentation**

8b 10MS/s Differential SAR ADC in 28 nm CMOS for Precise Energy Measurement

Wednesday 30 June 2021 15:30 (20 minutes)

In this article we present an 8-bit differential Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC), designed and manufactured in 28 nm CMOS process.

Radiation imaging is an essential part of medical diagnostics. Although integrating detectors are still widely used, more and more medical institutes have already switched to single photon counting (SPC) devices. The next step is colorful imaging, where each color represents the energy of the acquired photon, and the intensity –the number of hits in the pixel in the given time [1]. This could break new ground in medical imaging, reducing the number of exposures and thus the total irradiation dose. In the literature, there are examples of well-characterized detectors with two levels of energy discrimination [2]. However, in older technologies it was difficult to combine high spatial and energy resolution, maintaining a high count rate and low power consumption. Our aim is to enable fast imaging with the resolution of 256 energy levels, placing an ADC in each of the thousands of 100 µm × 100 µm pixels.

The SAR ADC presented in this article allows to distinguish 256 levels of energy and is capable of converting 10 MS/s. The Integrated Circuit (IC) (Fig. 1.) is currently under measurement and preliminary results show the INL and DNL of about ±0.5 LSB and ±0.6 LSB, respectively. Importantly, the proposed ADC's comparator input offset voltage correction in the time domain allows to effectively compensate mismatches without affecting the conversion rate as reported in [3-4]. Here, by changing the delay buffer voltage, the transfer characteristic can be shifted within the range of about 45 mV (Fig. 2.).

The whole IC area is 400 µm × 450 µm, while the core of the ADC occupies only 30 µm × 60 µm, and this can still be decreased by reducing the unit capacitance (here 0.5 fF), or by applying another switching scheme and changing the capacitor array. Nevertheless, such an ADC is able to fit into a considered pixel and to enable fast imaging with high energy resolution, while maintaining the spatial one at a fine level.

[1] K. Taguchi and J. S. Iwanczyk, Med. Phys. 40 (2013), 100901
[2] P. Gryboś et al., IEEE Trans. Nucl. Sci. 63 (2016), 1155–1161
[3] X. Yang et al., ESSCIRC 2019, 305-308
[4] P. Kaczmarczyk and P. Kmon, Przegląd Elektrotechniczny 96 (2020), 119-122

The authors acknowledge funding from the Ministry of Education and Science of Poland for the research project under the 'Diamond Grant'program (0071/DIA/2018/47).

Authors: KACZMARCZYK, Piotr (AGH University of Science and Technology); KMON, Piotr (AGH University of Science and Technology)

Presenter: KACZMARCZYK, Piotr (AGH University of Science and Technology)

Session Classification: Oral presentations

Track Classification: Front end electronics and readout