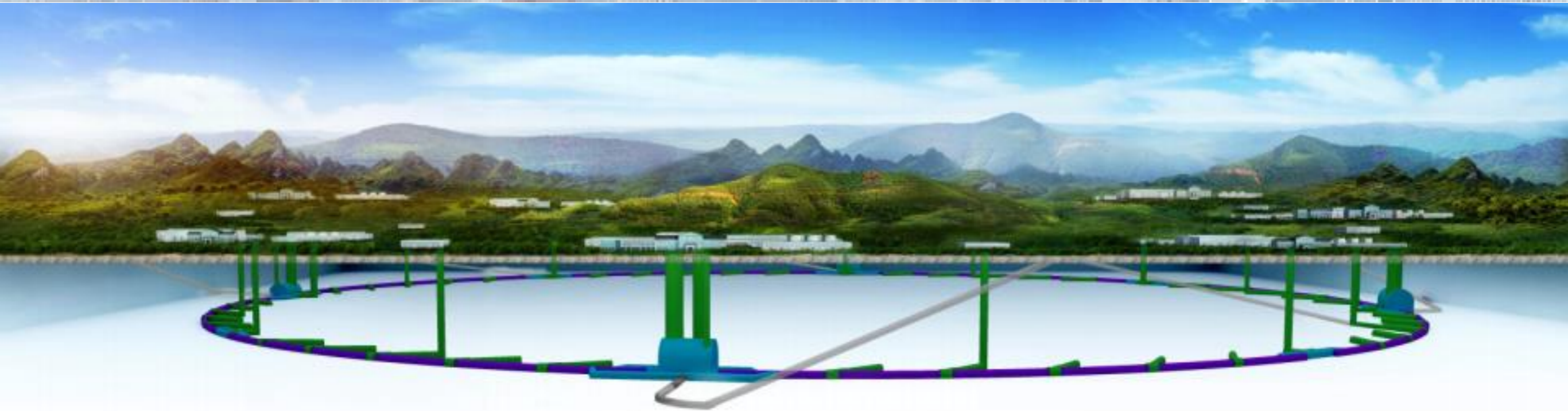


CEPC workshop
Chicago, 17/09/2019

CEPC Tracking R&D

Paolo Giacomelli
INFN Bologna



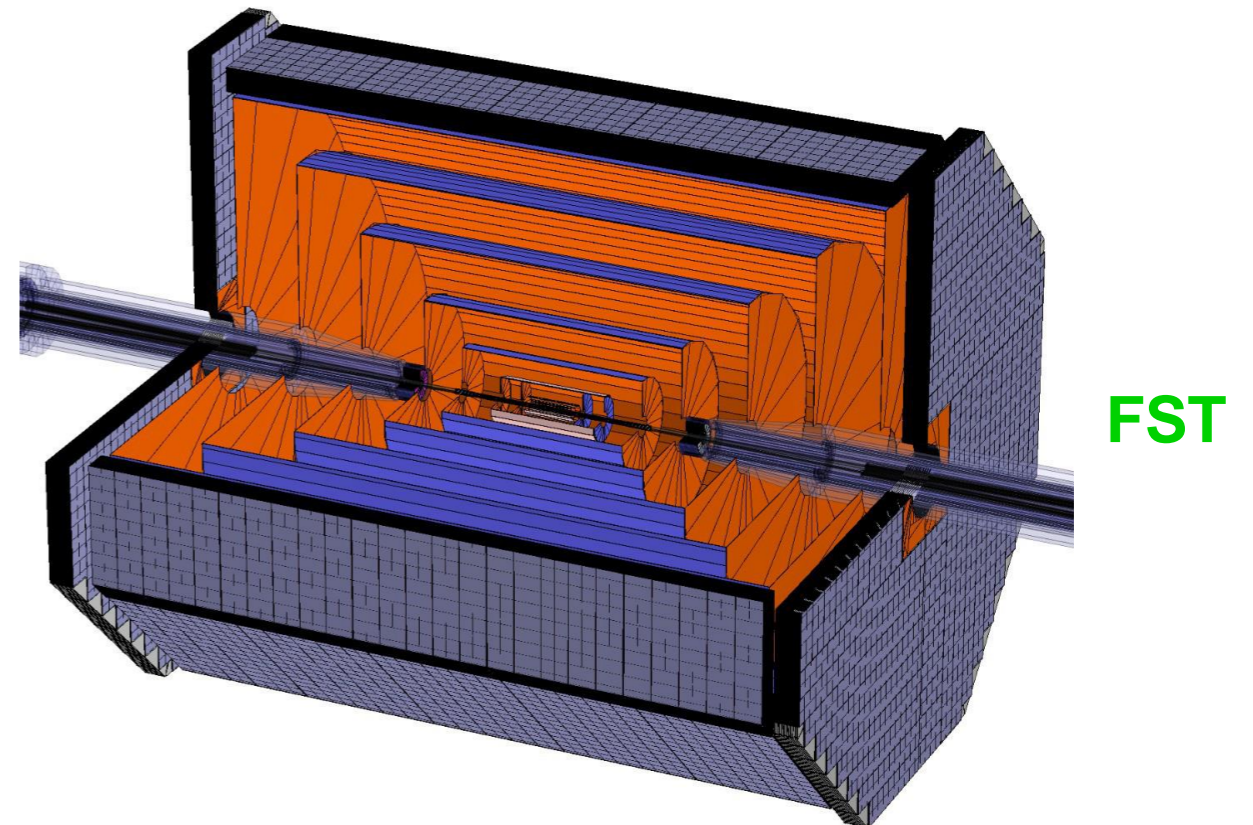
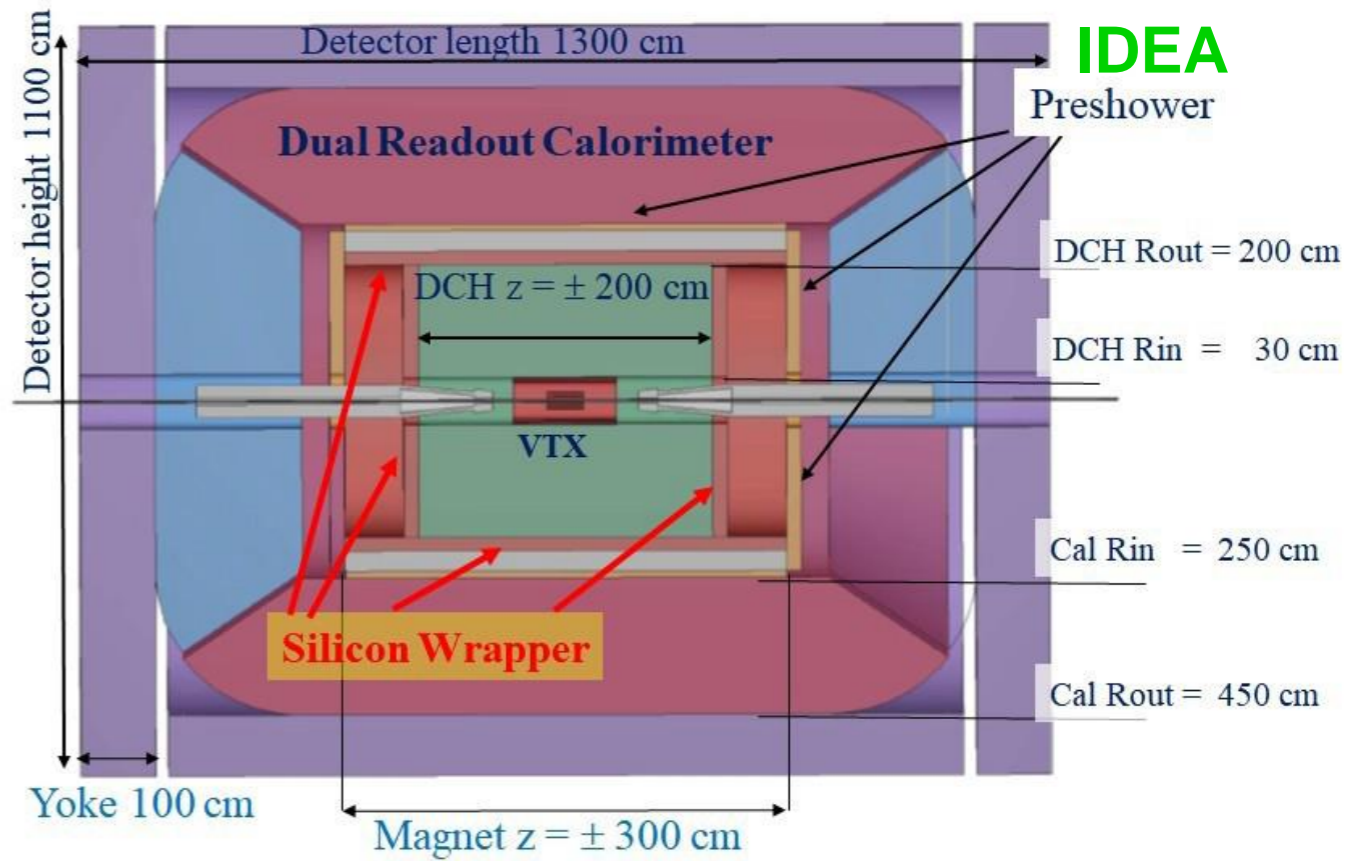
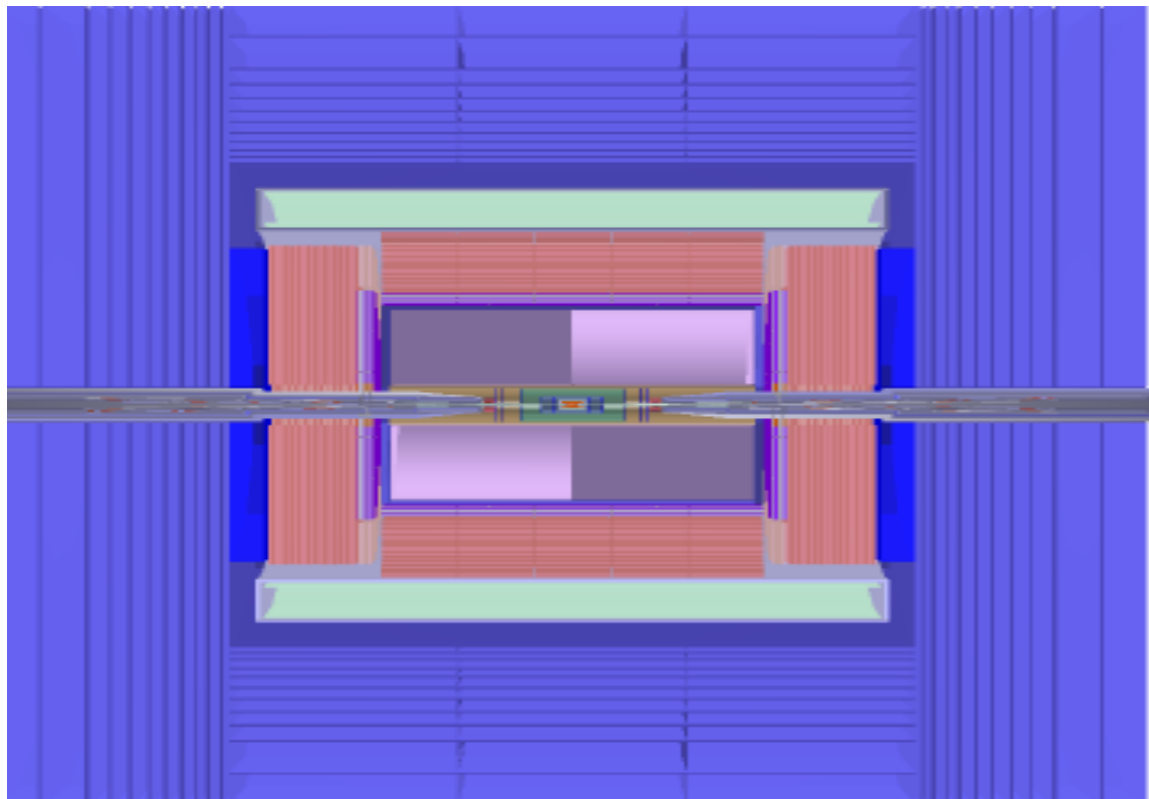
- **Tracking requirements**
- **Tracking detector challenges**
- **Vertex detectors**
- **Central trackers**
 - **All silicon**
 - **TPC**
 - **Wire chamber**
- **MPGDs**
 - **Preshower**
 - **Muon detectors**
- **R&D programmes**
- **Conclusions**

detectors

Baseline: Silicon + TPC

- IDEA: Silicon+Drift chamber(DCH)
- FST: all-silicon tracker
- Tracking performances:
 - VXD share common design
 - Tracker: TPC vs DCH vs Silicon

Baseline



FST

Tracking requirements at H, Z, WW

- $\Delta p_t/p_t^2 \sim 2 \times 10^{-5} \text{ (GeV}^{-1}\text{)}$
- Tracker must be as light as possible
- High efficiency down to low momentum
- Identification of secondary vertices similar and better than modern LHC detectors
- Flavour tagging
 - Decay length
- Excellent b/c separation (much better than LHC detectors)
- PID for π^{+-} separation from other particles

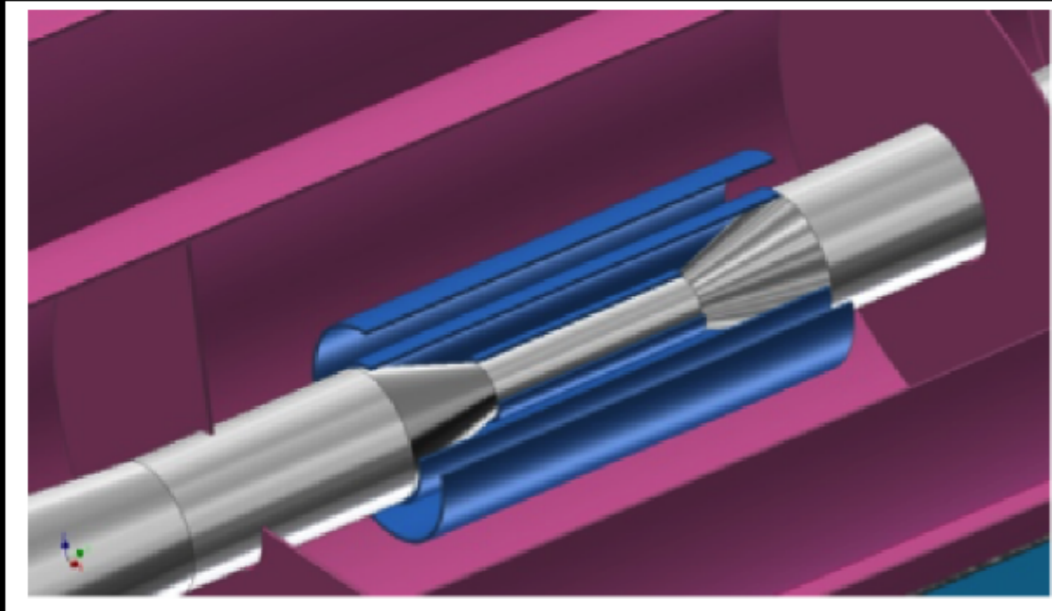
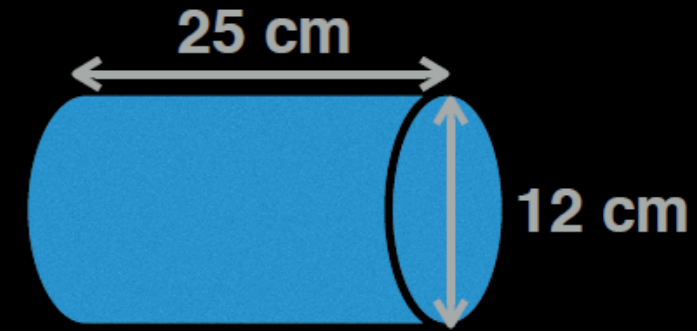
Vertex detectors: challenges

- **Very good spatial resolution,**
 - **$\sim 3-4 \mu\text{m}$**
- **As little material as possible**
 - **Extremely thin detectors,**
 - **$\sim 50-100 \mu\text{m}$ thickness**
 - **1st layer as close as possible to the IP**
- **Very low power consumption**
 - **$< 20 \text{ mW/cm}^2$**
- **Very efficient cooling**
- **Do we need to cool also the beam pipe?**

Vertex detectors: baseline

Baseline Pixel Detector Layout

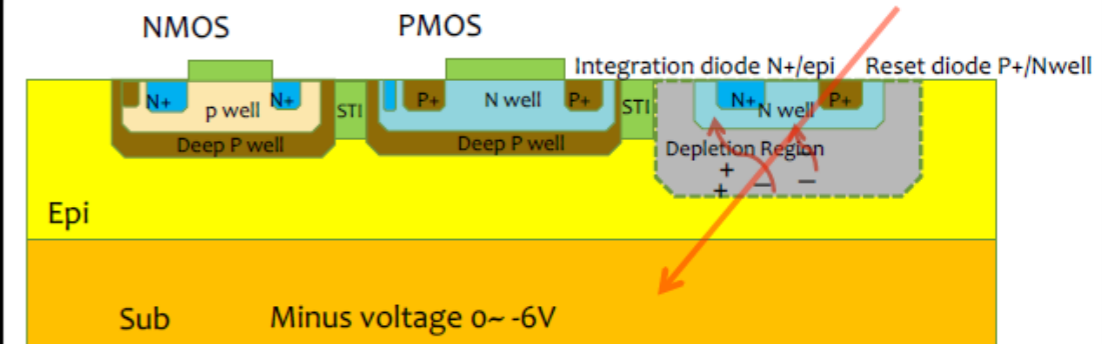
3-layers of double-sided pixel sensors



- ◆ ILD-like layout
- ◆ Innermost layer: $\sigma_{SP} = 2.8 \mu\text{m}$
- ◆ Polar angle $\theta \sim 15$ degrees

Implemented in GEANT4 simulation framework (MOKKA)

CMOS pixel sensor (MAPS)



Integrated sensor and readout electronics on the same silicon bulk with “standard” CMOS process:

- low material budget,
- low power consumption,
- low cost ...

	$R(mm)$	$ z (mm)$	$ \cos\theta $	$\sigma(\mu\text{m})$	Readout time(us)	
Ladder 1	Layer 1	16	62.5	0.97	2.8	20
	Layer 2	18	62.5	0.96	6	1-10
Ladder 2	Layer 3	37	125.0	0.96	4	20
	Layer 4	39	125.0	0.95	4	20
Ladder 3	Layer 5	58	125.0	0.91	4	20
	Layer 6	60	125.0	0.90	4	20

Silicon Vertex Detector **Prototype** – MOST (2018–2023)

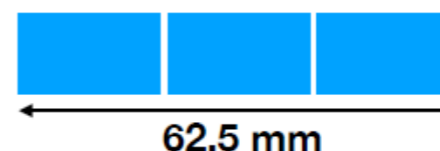
Sensor technology CMOS TowerJazz

- ✦ Design sensor with large area and high resolution
- ✦ Integration of front-end electronic on sensor chip

Benefit from MOST 1 research program



Double sided ladder

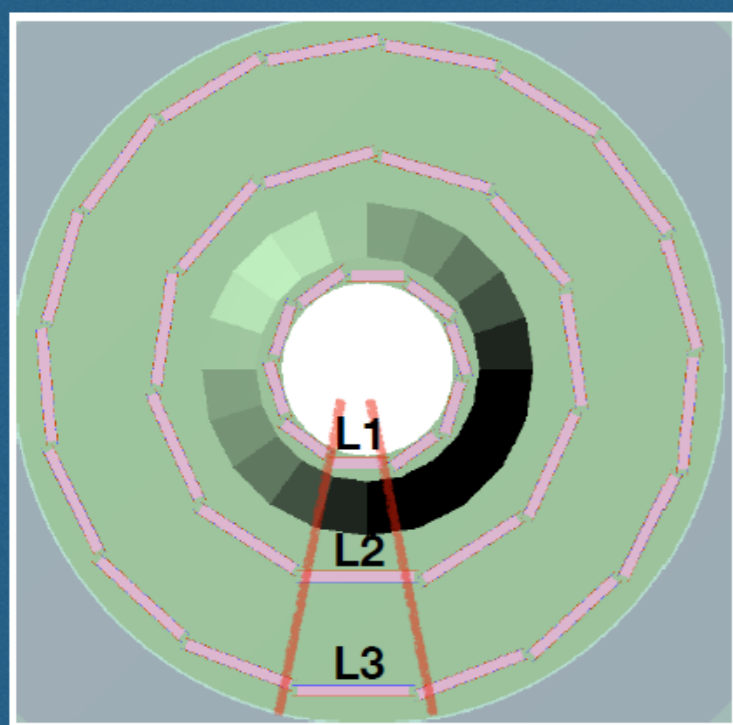


62.5 mm

Layer 1 (11 mm x 62.5 mm)
Chip size: 11 mm X 20.8 mm

3 X 2 layer = 6 chips

3-layer sector



Baseline MOST2 goal:
3-layer prototype

Default layout requires different size ladders

Keep it simple for baseline design

L1

L2

L3

3-layers
same size
same chip

Goals:

1 MRad TID

3-5 μ m SP resolution

Integrate electronics
readout

Design and produce
light and rigid
support structures

8

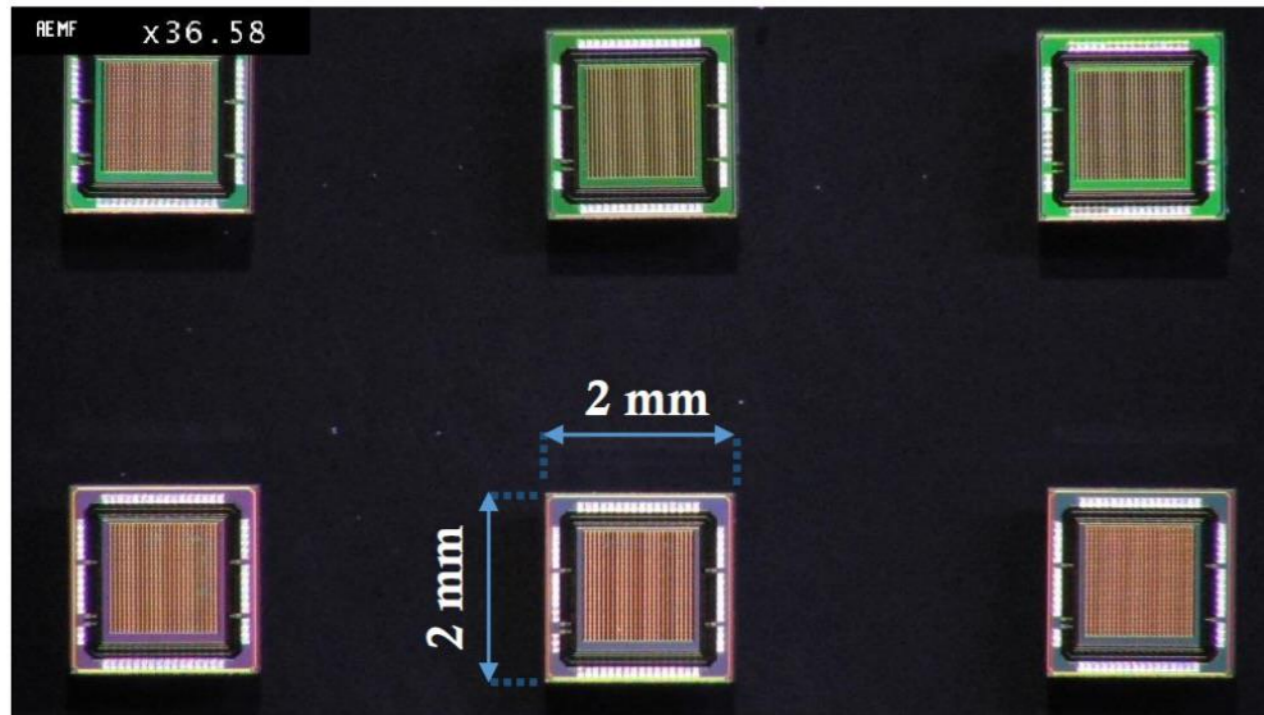
Vertex detectors: challenges

Limitation of the existing CMOS sensors

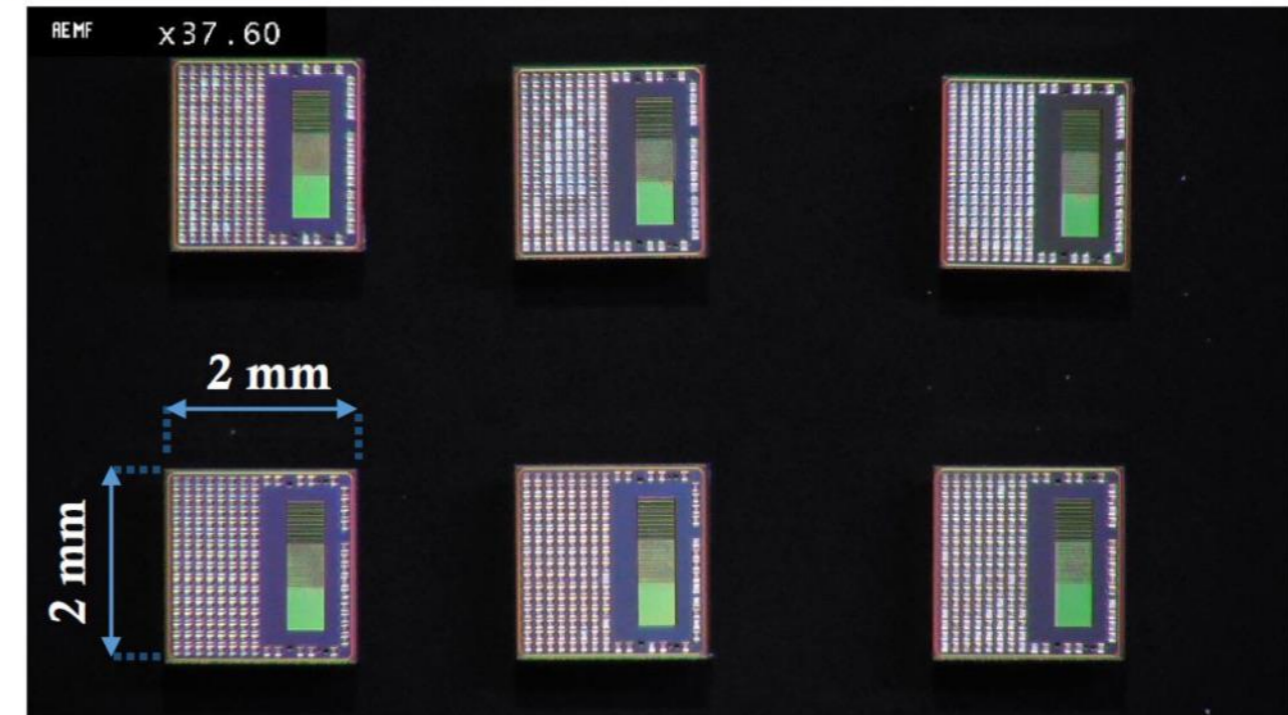
- **None of the existing CMOS sensors can fully satisfy the requirement of high-rate CEPC Vertex Detector**
- **Two major constraints for the CMOS sensor**
 - **Pixel size: should be $< 25\mu\text{m} * 25\mu\text{m}$, aiming for $16\mu\text{m} * 16\mu\text{m}$**
 - **Readout speed: bunch crossing @ 40MHz**
- **TID is also a constraint, but 1Mrad is not so difficult**

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA	JadePix/ MIC4 (MOST1)
Pixel size	✓	X	✓	✓
Readout Speed	X	✓	X	X
TID	X (?)	✓	✓	To be tested

Complete monolithic sensor

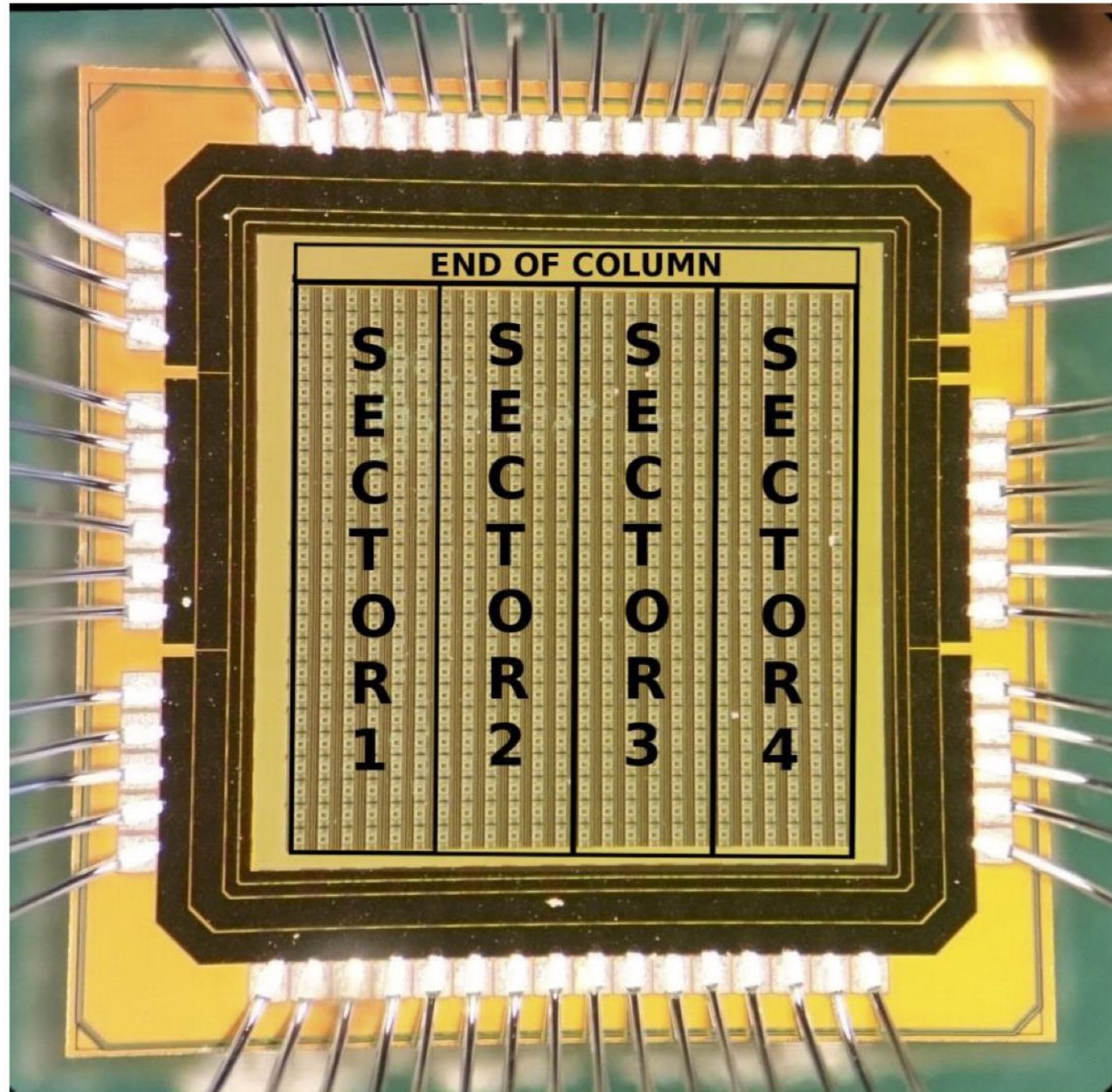


Test chip



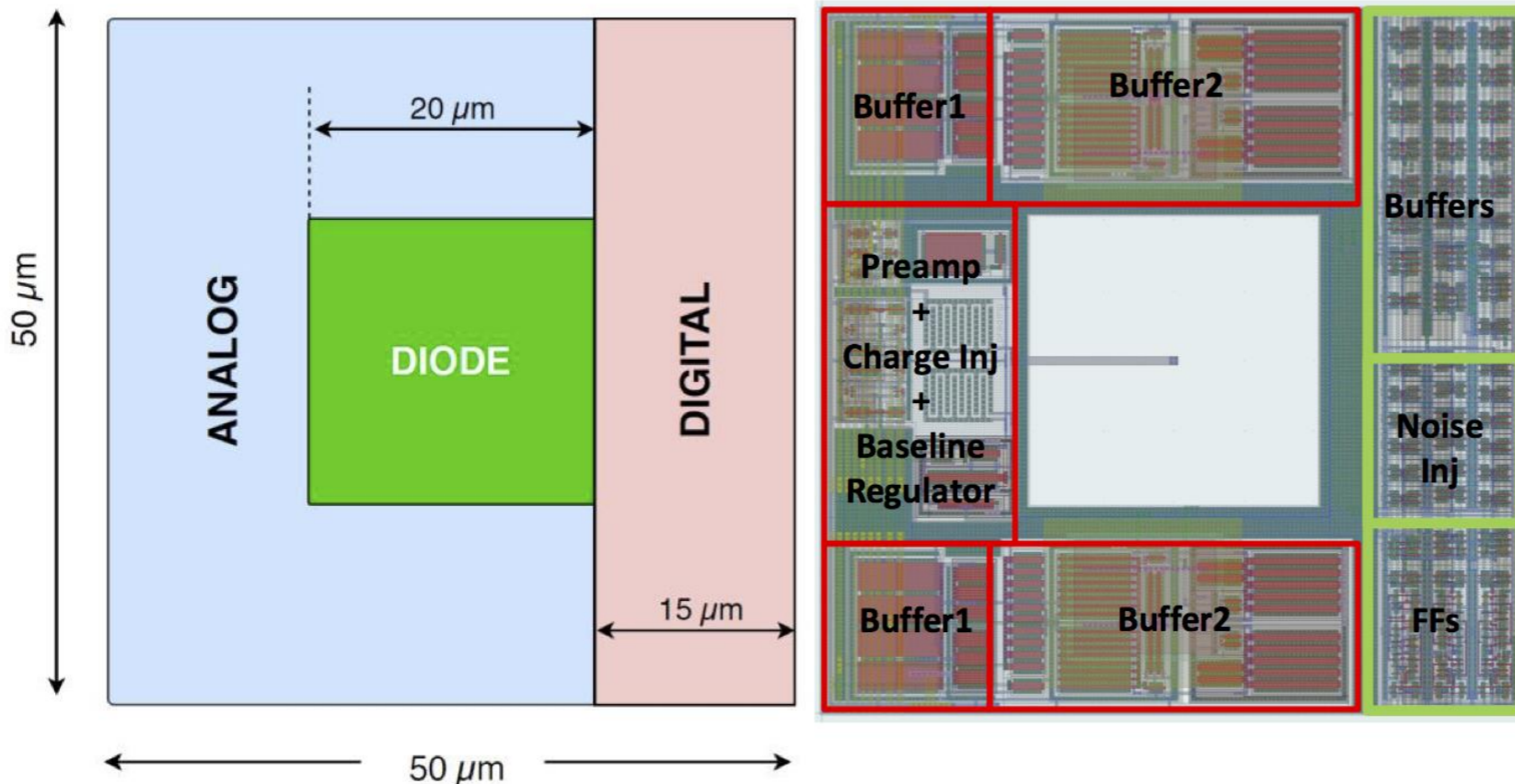
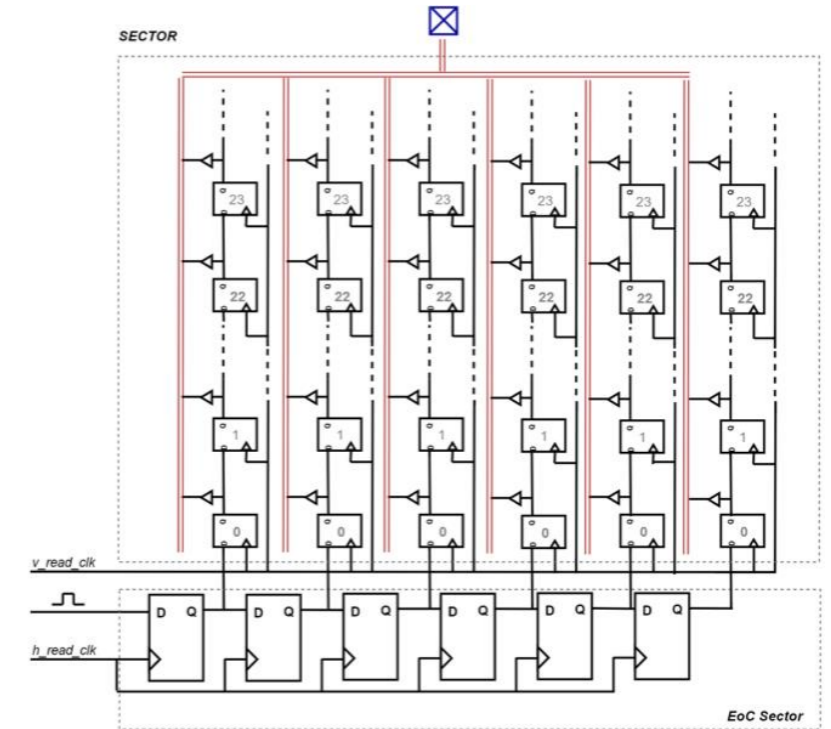
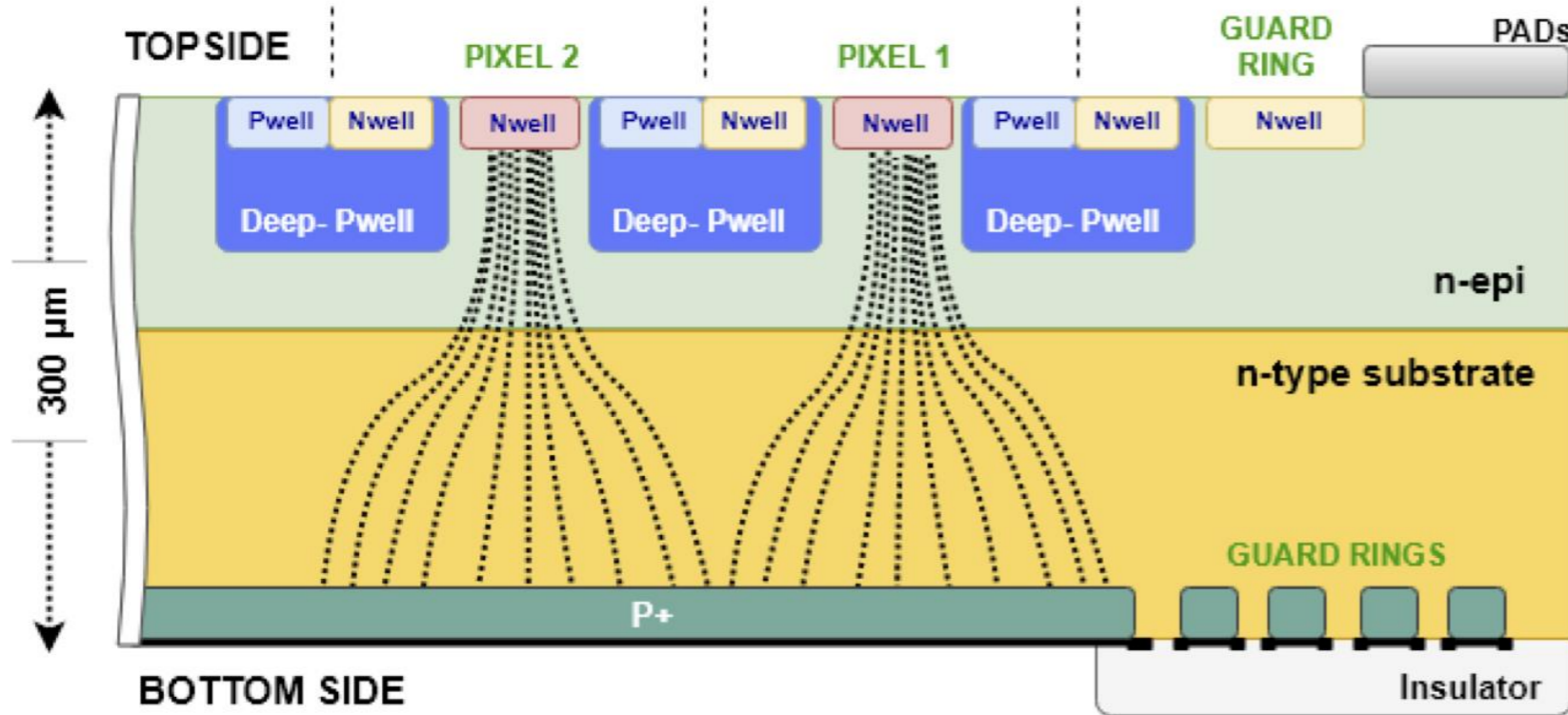
Technology	110 nm double side CMOS technology
Metal layers	6
Size	2 X 2 mm ²

- Wafers with small different epitaxial layer thickness have been used for the production



- ◆ Monolithic sensor with embedded CMOS electronics.
- ◆ Compatible with a standard CMOS process
- ◆ matrix of 24 x 24 pixels organised in 4 sectors
- ◆ Analog readout with CDS
- ◆ 2x2 mm² die, VDD=1.2V

ARCADIA: sensor architecture



Sensors with Embedded Electronics Design (SEED)

Supported by INFN R&D Committee

- R&D effort on DMAPS taking momentum within INFN
- Direct cooperation with a silicon foundry (LFoundry)
- Pixel size between $10\ \mu$ and $100\ \mu$
- Large scale demonstrators planned for mid-2020
- Take as much profit as possible for the existing in the meanwhile

Central trackers: challenges

- **Silicon tracker**

- **Number of layers**

- **As low as possible material budget**

- **Very thin detectors**

- **TPC**

- **Ion backflow**

- **Calibration and alignment**

- **Low power consumption FEE ASIC chip**

- **Mechanical and distortion challenges**

- **Wire chamber**

- **Very long wires, ~4m**

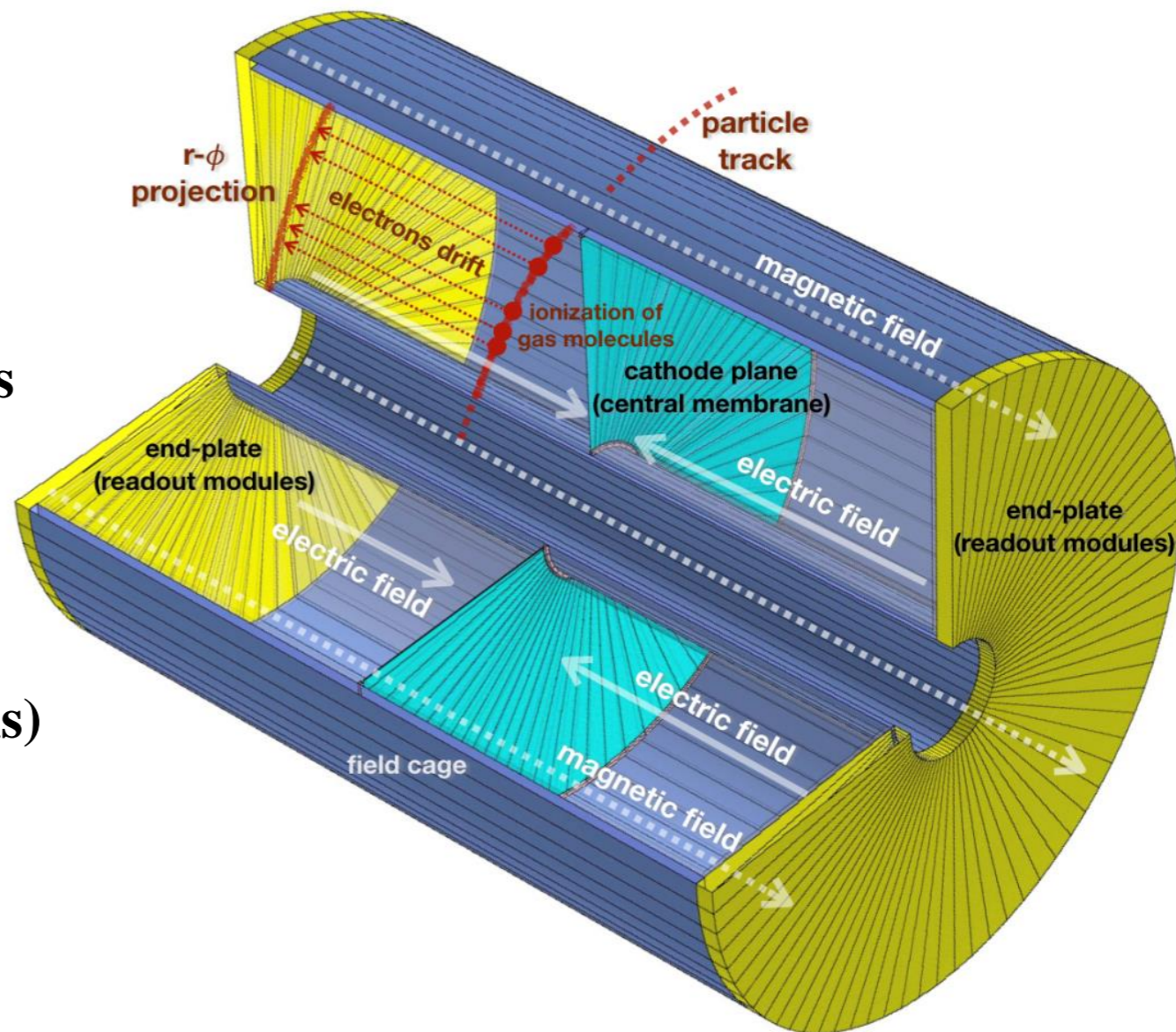
- **New wire materials, with or without metallic coating**

- **Cluster counting**

TPC could directly provides three-dimensional space points; the gaseous detector volume gives a low material budget; and the high density of such space points enables excellent pattern recognition capability.

Why use TPC detector as the tracker detector?

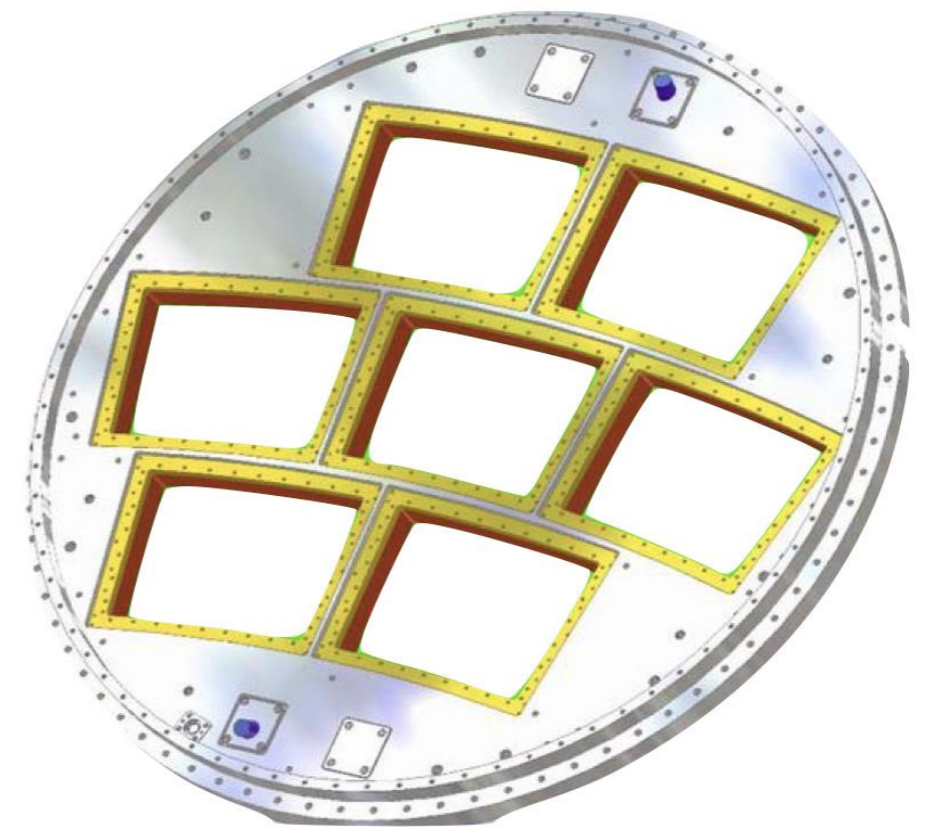
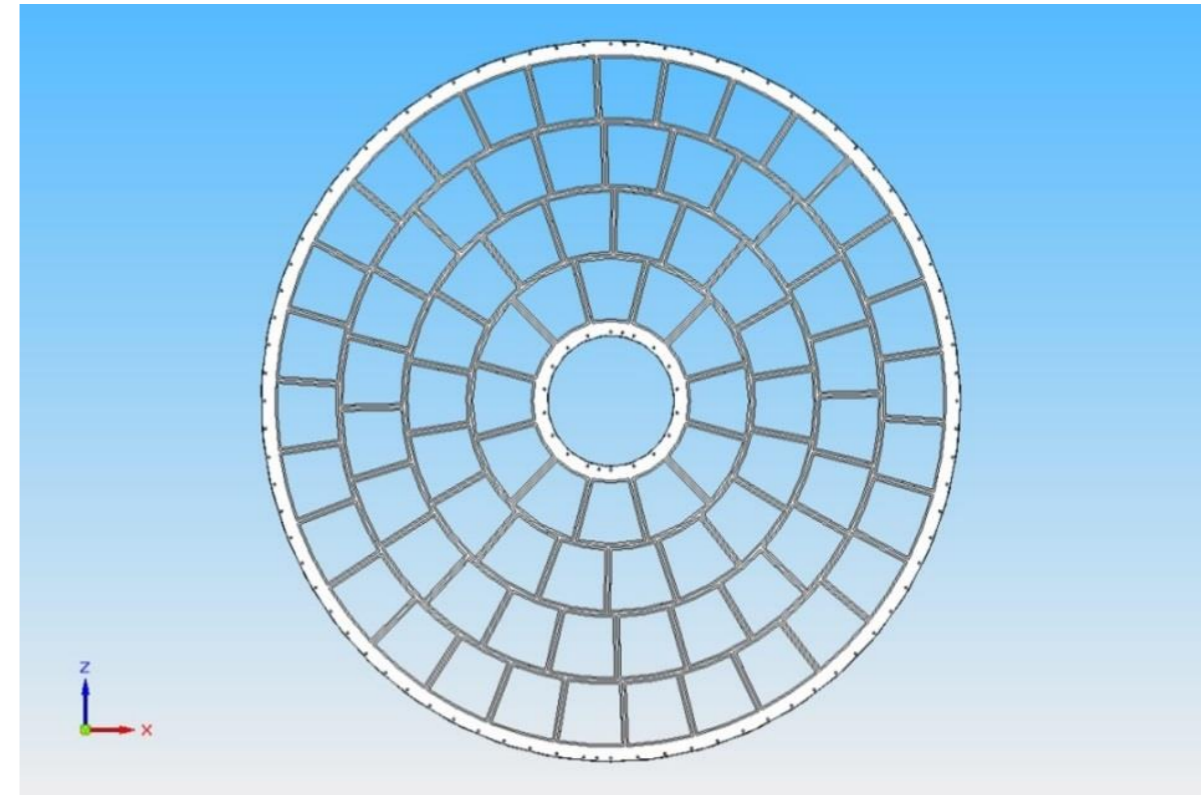
- ❑ Motivated by the H tagging and Z
- ❑ TPC is the perfect detector for HI collisions ... (ALICE TPC...)
- ❑ Almost the whole volume is active
- ❑ **Minimal radiation length (field cage, gas)**
- ❑ Easy pattern recognition (continuous tracks)
- ❑ PID information from ionization measurements (dE/dx)
- ❑ **Operating under high magnetic field**
- ❑ MPGD as the readout



Overview of TPC detector concept

TPC detector concept:

- ❑ Under 3 Tesla magnetic field (**Momentum resolution: $\sim 10^{-4}/\text{GeV}/c$ with TPC standalone**)
- ❑ Large number of 3D space points (**~ 220 along the diameter**)
- ❑ **dE/dx resolution: $< 5\%$**
- ❑ **$\sim 100 \mu\text{m}$ position resolution in $r\phi$**
 - ❑ **$\sim 60 \mu\text{m}$ for zero drift, $< 100 \mu\text{m}$ overall**
 - ❑ **Systematics precision ($< 20 \mu\text{m}$ internal)**
- ❑ **TPC material budget**
 - ❑ **$< 1X_0$ including outer field cage**
- ❑ **Tracker efficiency: $> 97\%$ for $p_T > 1\text{GeV}$**
- ❑ **2-hit resolution in $r\phi$: $\sim 2\text{mm}$**
- ❑ **Module design: $\sim 200\text{mm} \times 170\text{mm}$**
- ❑ **Minimizes dead space between the modules: 1-2mm**



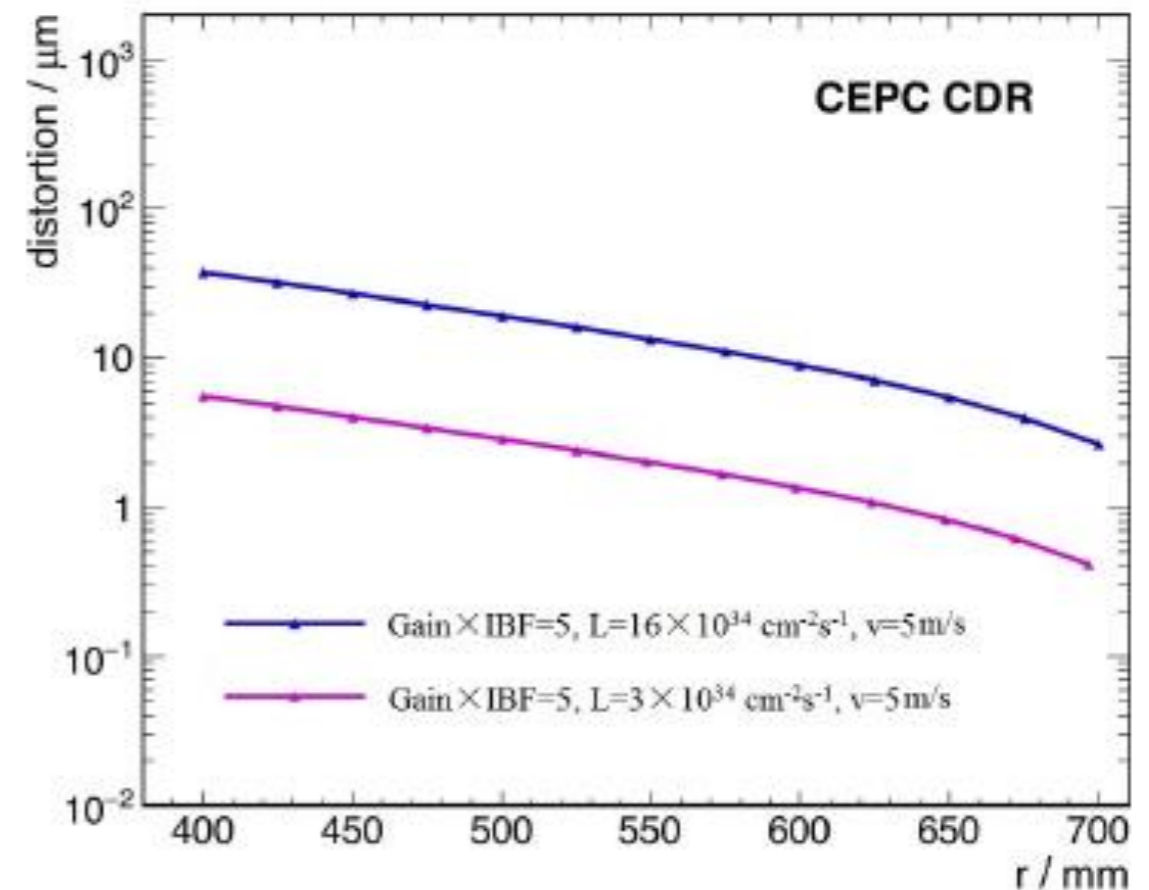
TPC detector endplate concept

- Occupancy simulation
 - **Gain×IBF** refers to the number of ions that will escape the end-plate readout modules per primary ionization, obtained by the multiplication of the readout modules gain and the ion backflow reducing rate (IBF)
 - L : the luminosity in units of $10^{34} \text{cm}^{-2} \text{s}^{-1}$
 - Voxel size: $1\text{mm} \times 6\text{mm} \times 2\text{mm}$
@DAQ/40MHz
 - Maximal occupancy at TPC inner most layer: $\sim 10^{-5}$ (safe)
 - Full simulation: 9 thousand Z to qq events
 - Bhabha events: a few nb
 - Background considered ? (Need careful designed Shielding/detector protection)

Pad size : $1\text{mm} \times 6\text{mm}$

$T_{\text{sample}} : 25\text{ns}$

$V_{\text{drift}} : 80\mu\text{m}/\text{ns}$

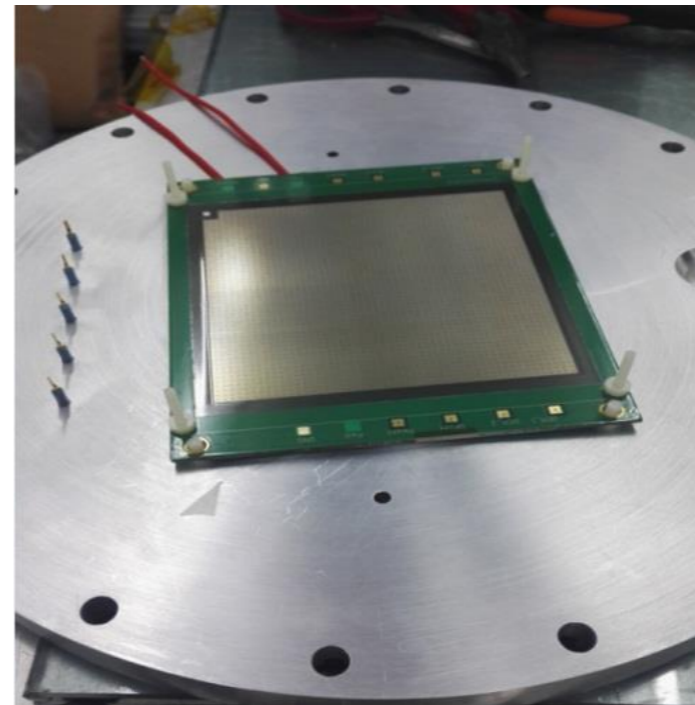


Distortion on the hit position reconstruction

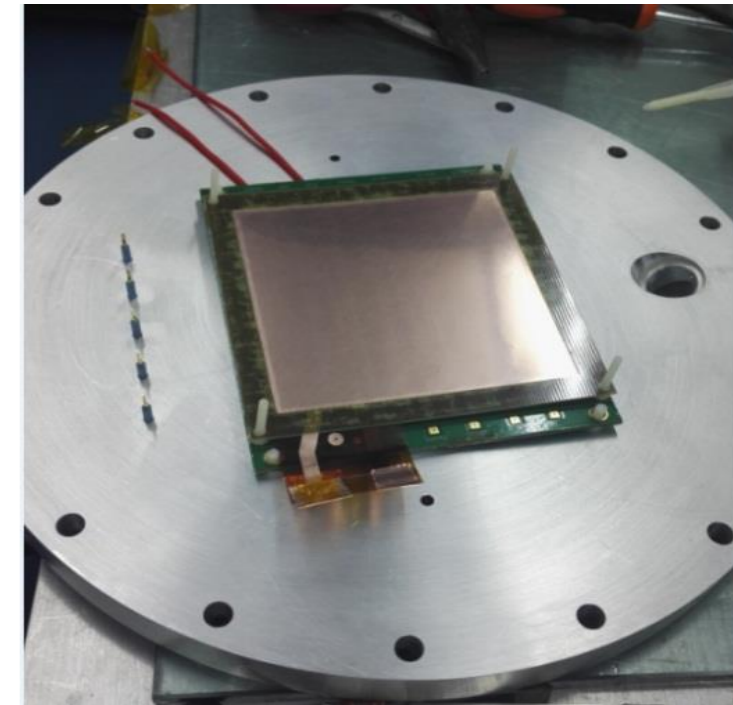
To conclude, the TPC will be able to be used if the **Gain×IBF** can be controlled to a value smaller than 5.

- Some R&D activities
 - TPC detector module -> IBF control
 - TPC detector prototype -> Calibration
 - Low power consumption -> FEE ASIC chip

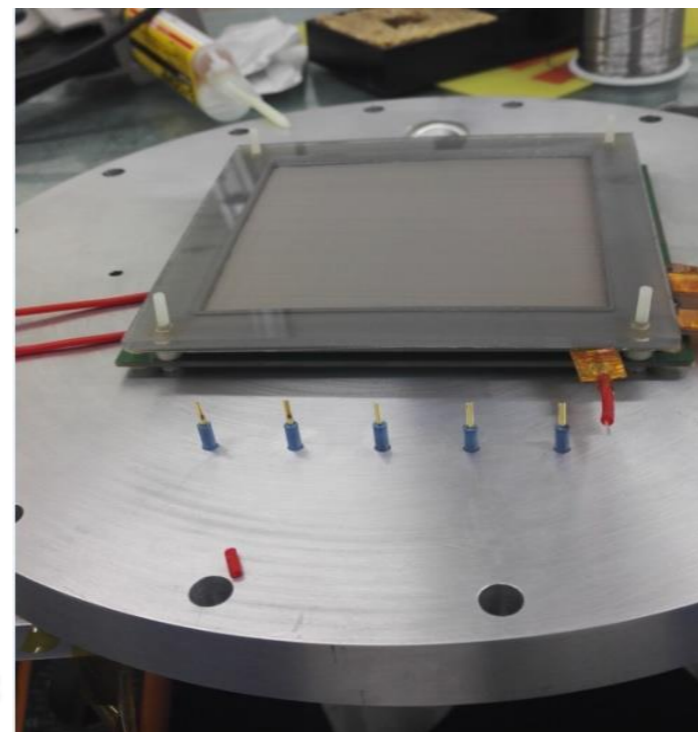
- ❑ Study with GEM-MM module
 - ❑ New assembled module
 - ❑ Active area: 100 mm×100 mm
 - ❑ X-tube ray and ^{55}Fe source
 - ❑ Bulk-Micromegas assembled from Saclay
 - ❑ Standard GEM from CERN
 - ❑ Avalanche gap of MM: 128 μm
 - ❑ Transfer gap: 2 mm
 - ❑ Drift length: 2 mm~200 mm
 - ❑ pA current meter: Keithley 6517B
 - ❑ Current recording: Auto-record interface by LabView
 - ❑ Standard Mesh: 400 LPI
 - ❑ High mesh: 508 LPI



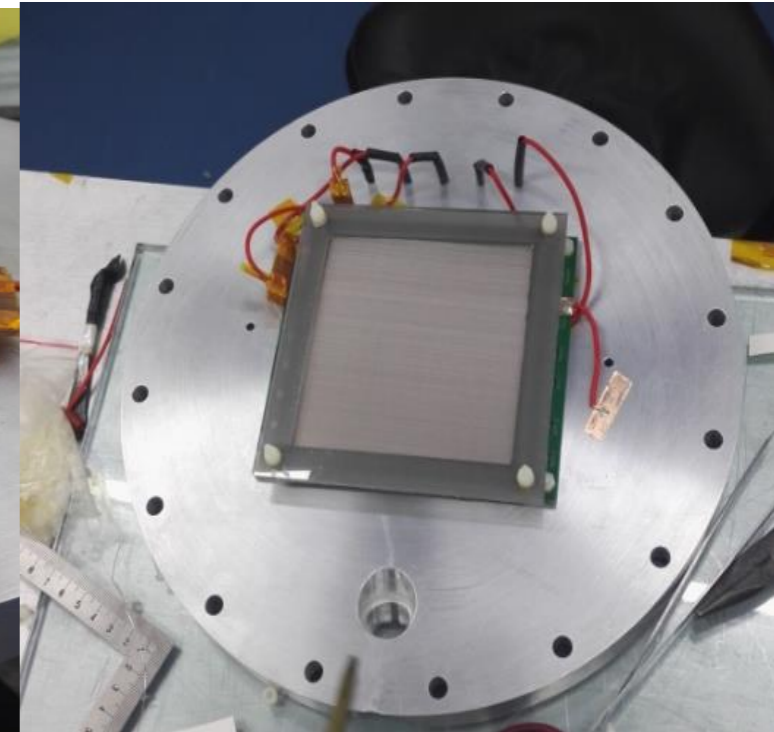
Micromegas(Saclay)



GEM(CERN)



Cathode with mesh



GEM-MM Detector

$50 \times 50 \text{ mm}^2$ $100 \times 100 \text{ mm}^2$ $200 \times 200 \text{ mm}^2$
 2015-2016 \longrightarrow 2017-2018 \longrightarrow 2019-

Central trackers: TPCs

Motivation of the TPC prototype

- Study and estimation of the distortion from the IBF and primary ions with the laser calibration system
- Main parameters
 - Drift length: **~510mm**, Readout active area: **200mm × 200mm**
 - Integrated the laser calibration with 266nm
 - GEMs/Micromegas as the readout
 - Matched to assembled in the 1.0T PCMAG

1. TPC chamber
2. Laser calibration

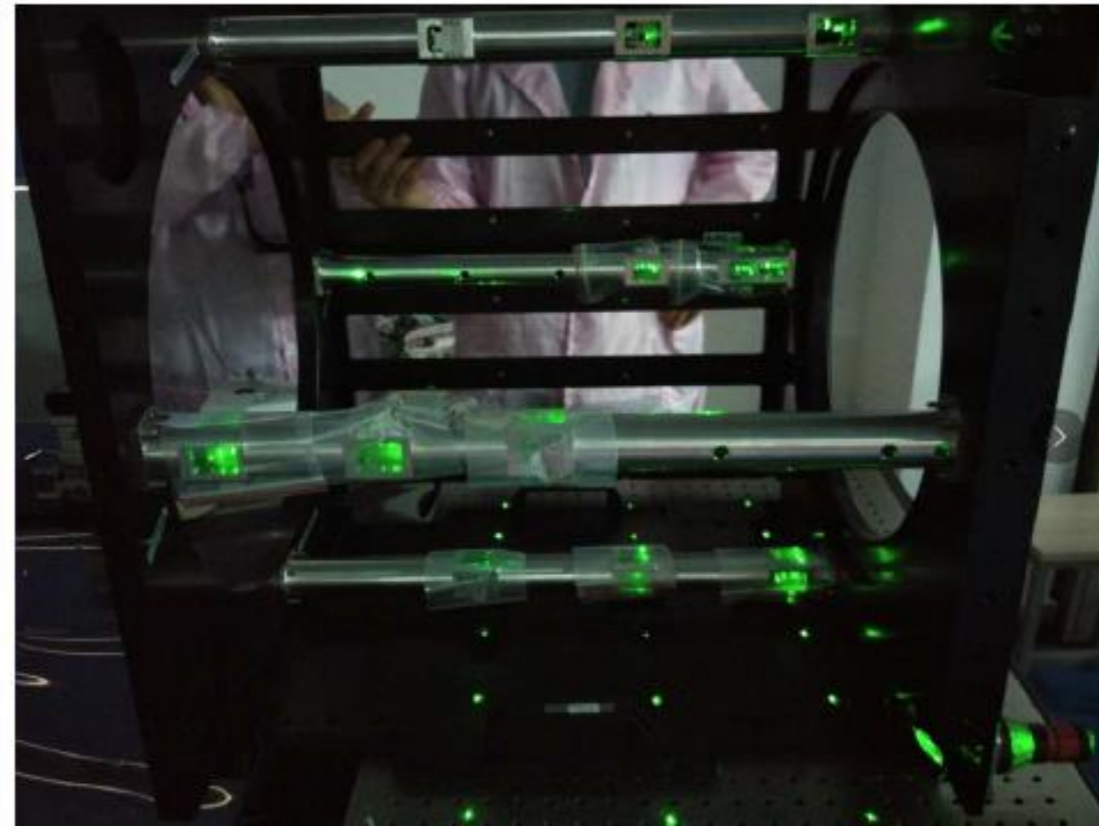
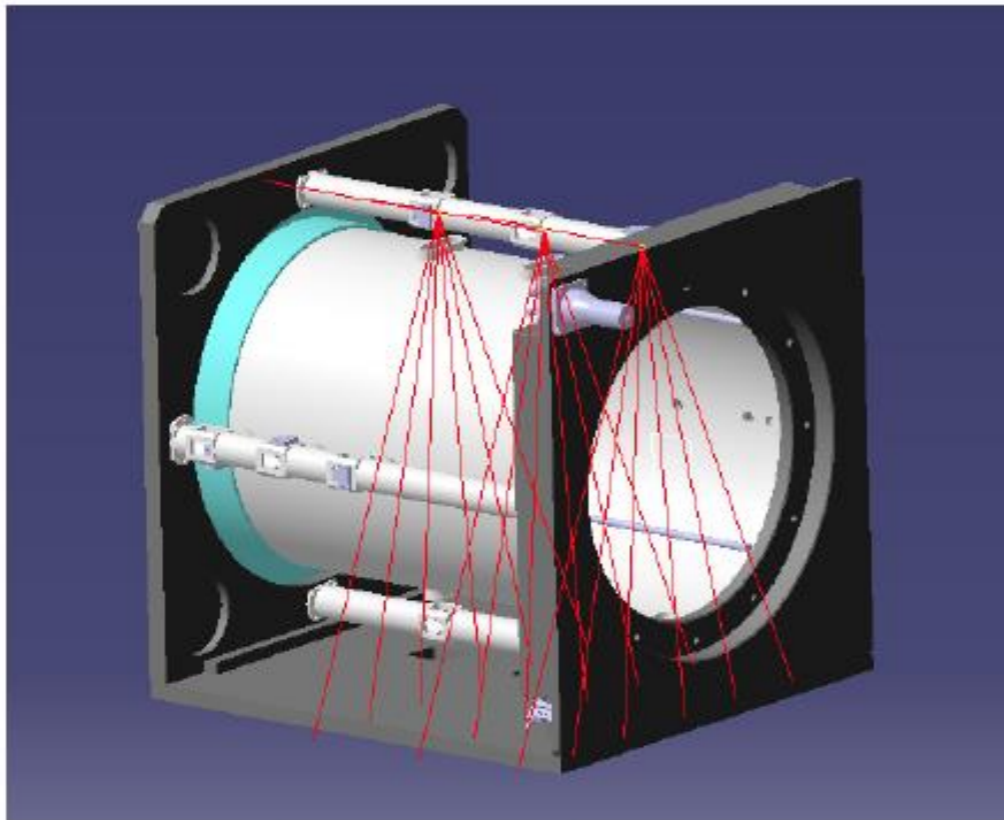
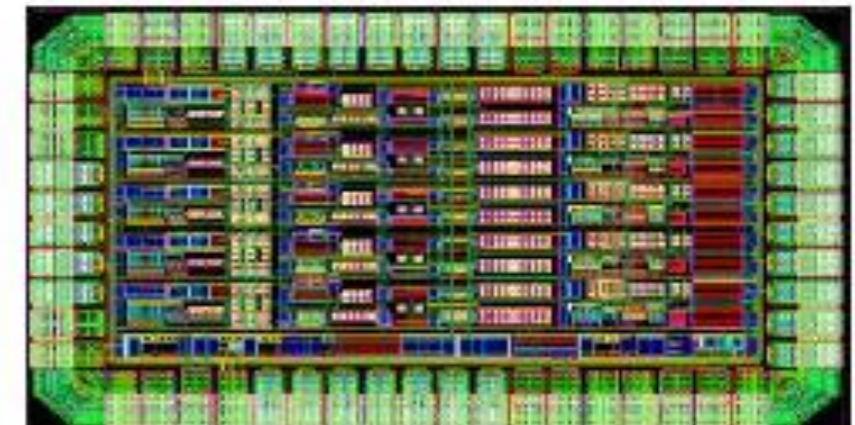
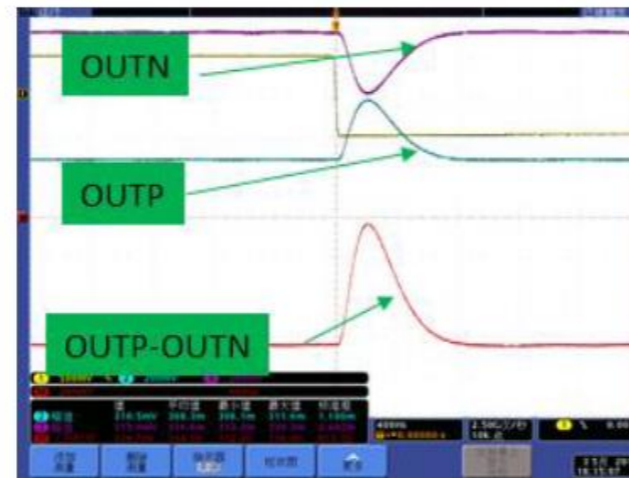
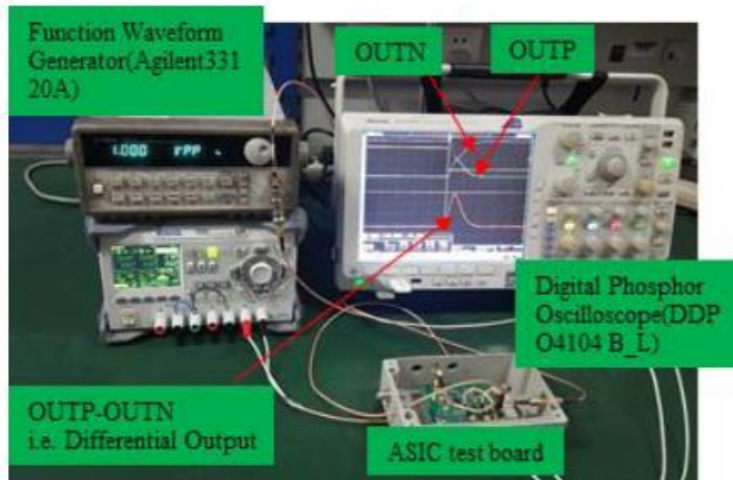
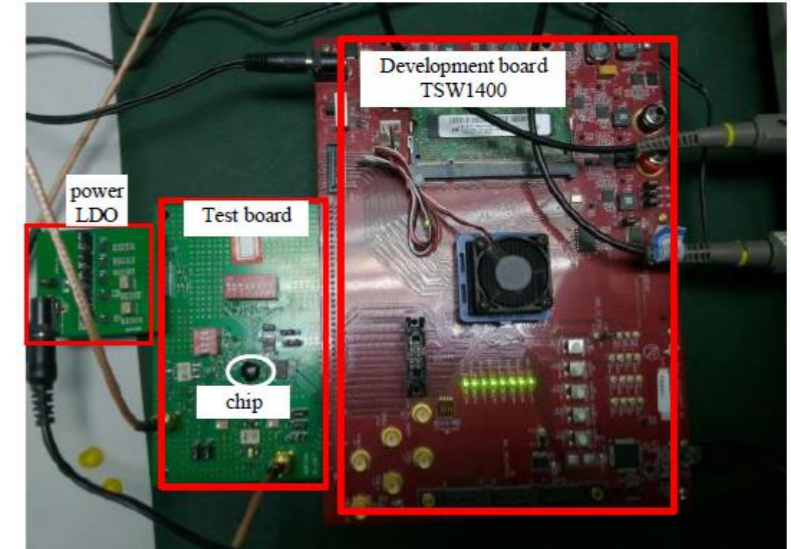


Diagram of the TPC prototype with the laser calibration system

Huirong Qi

TPC FEE chip

- Develop a low power and highly integration front-end ASIC in 65 nm CMOS
- Each channel consists of the analog front-end (AFE) and a SAR ADC in 10b and up to 40 MSPS
- Less than 5 mW per channel



• AFE test summary

	Specifications	Test Results
Gain	10mV/fC	10.5mV/fC
Dynamic Range	120fC	>120fC
INL	<1%	0.41%
Power consumption	2.50mW/ch	2.18mW/ch
ENC	500e @ 10pF	448e @ 10pF
Xtalk	<1%	<0.36%

• SAR ADC test summary

	Specifications	Test Results
Sampling rate	40 MSPS	50 MSPS
Resolution	10 bit	10 bit
INL	<0.65 LBS	<0.5 LSB
DNL	<0.6 LSB	<0.5 LSB
ENOB	>9 bit	9.18 bit
Power consumption	<2.5 mW/ch	1 mW/ch

Wire length problem

Electrostatic stability condition

$$T > \frac{C^2 V_0^2 L^2}{4\pi\epsilon w^2}$$

T = wire tension
 C = capacitance per unit length
 V_0 = anode-cathode voltage
 L = wire length, w = cell width

IDEA Drift Chamber: $C = 10$ pF/m, $V_0 = 1500$ V, $L = 4.0$ m, $w = 1.0$ cm

$$T > 0.32 \text{ N}$$

- 20 μm W sense wire (Y.S. ≈ 1200 MPa): $T_{max} = 0.38$ N (marginal)
 - 40 μm Al field wire (Y.S. ≈ 300 MPa): $T_{max} = 0.38$ N (marginal)
- => **shorten chamber** (loss of acceptance)
=> **widen cell size** (increase occupancy)
=> **increase wire diameter** (increase multiple scattering and endplate

load)

or,

=> replace 40 μm Al with **Titanium** (Y.S. ≈ 550 MPa): $T_{max} = 0.70$ N
but Ti G5 (90%Ti-6%Al-4%V) hard to draw in such sizes ("galling phenomenon")

=> replace 40 μm Al with **35 μm Carbon monofilament**

(Y.S. > 860 MPa): $T_{max} > 0.83$ N

New wires: Carbon monofilaments

SPECIALTY MATERIALS, INC.

Manufacturers of Boron and SCS Silicon Carbide Fibers and Boron Nanopowder

CARBON MONOFILAMENT



TYPICAL PROPERTIES

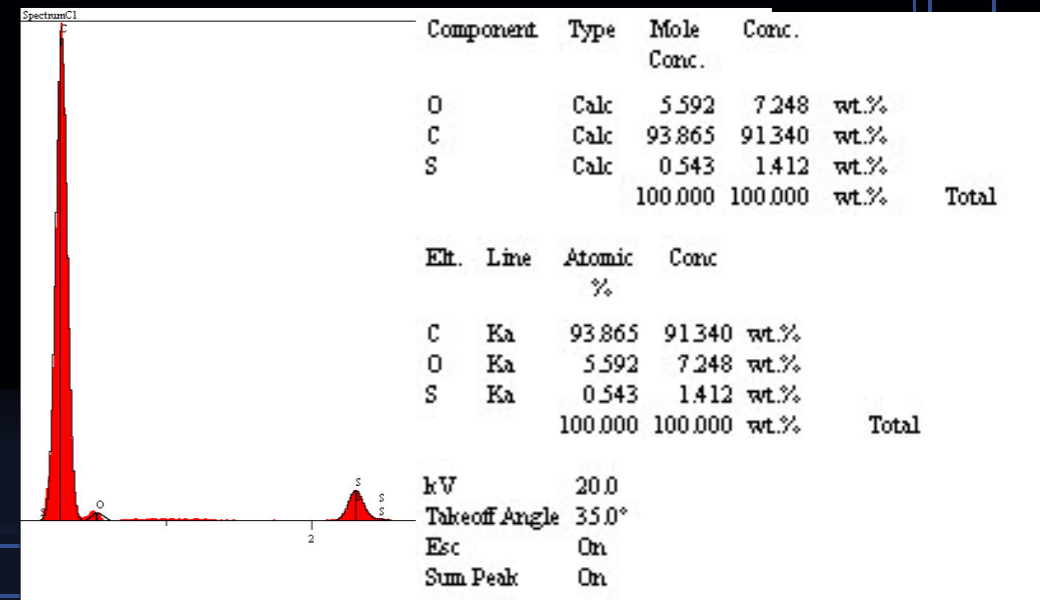
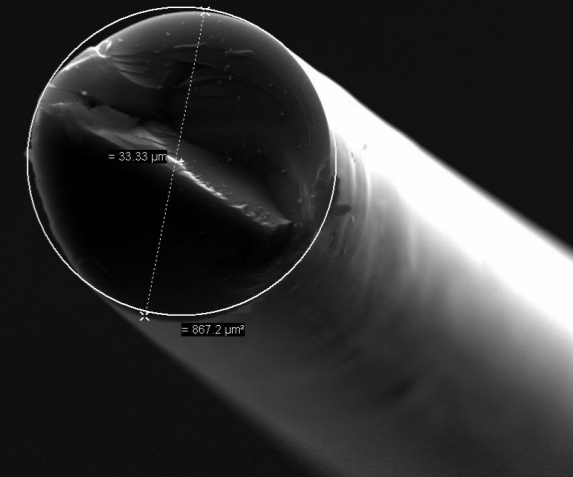
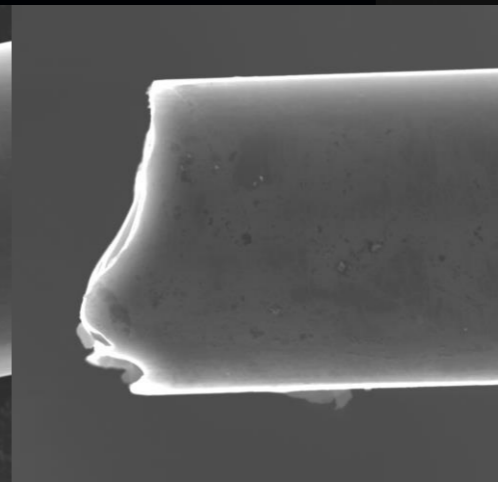
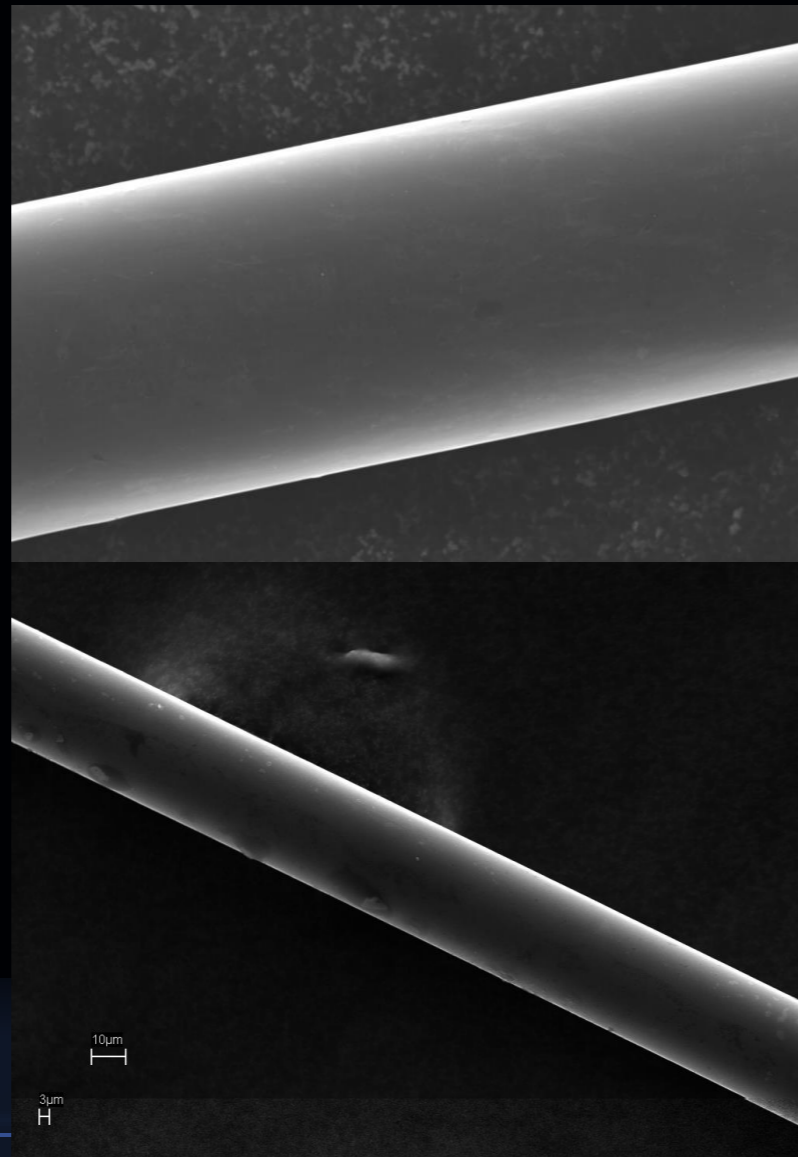
Diameter: 0.00136 +/- 0.0001" (34.5 +/- 2.5 μm)
Tensile Strength: 125 ksi (0.86 GPa)
Tensile Modulus: 6 msi (41.5 GPa)
Electrical Resistivity: 3.6×10^{-3} ohm cm
Density: 1.8 g/cc

Specialty Materials, Inc.
 1449 Middlesex Street
 Lowell, Massachusetts 01851

CARBON MONOFILAMENT PRODUCT PRICE LIST
 Effective October 1, 2017

Product	Quantity	Price LF
CARBON MONOFILAMENT	1 Million LF	\$0.02
	500,000 LF	\$0.03
	1,000 LF	\$0.93

Phone: 978-322-1900
 Fax: 978-322-1970



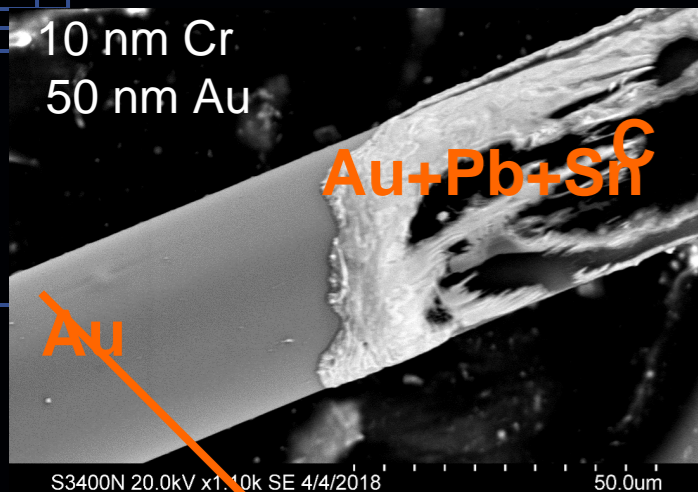
C wire metal coating

BINP

A. Popov
V. Logashenko

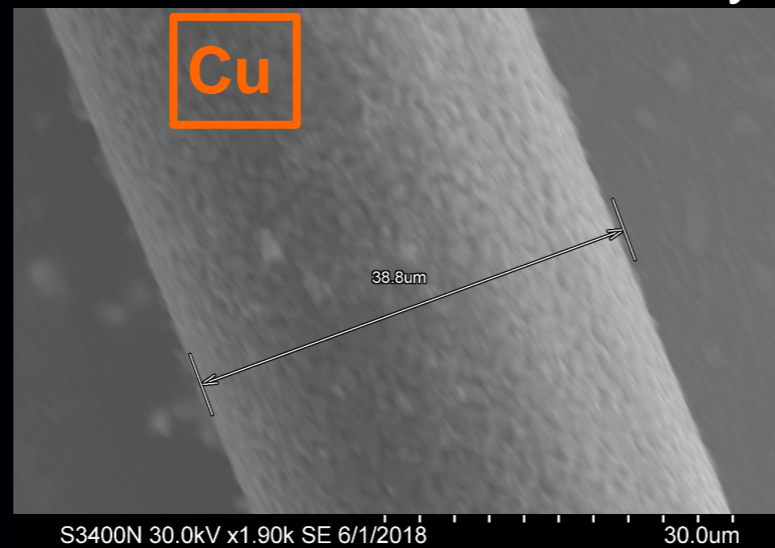
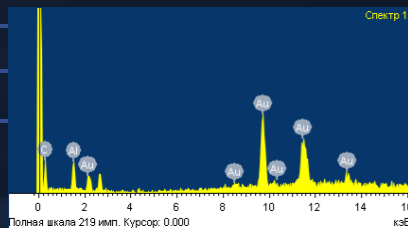
HiPIMS: High-power impulse magnetron sputtering

physical vapor deposition (PVD) of thin films based on magnetron sputter deposition (extremely high power densities of the order of kW/cm^2 in short pulses of tens of microseconds at low duty cycle $<10\%$)

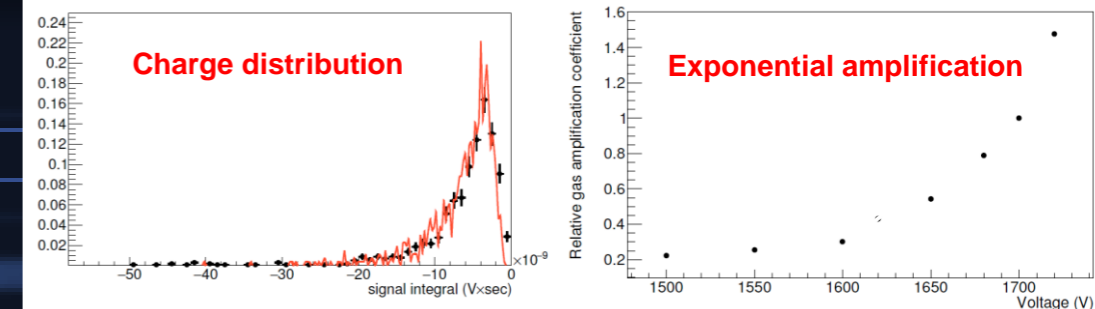
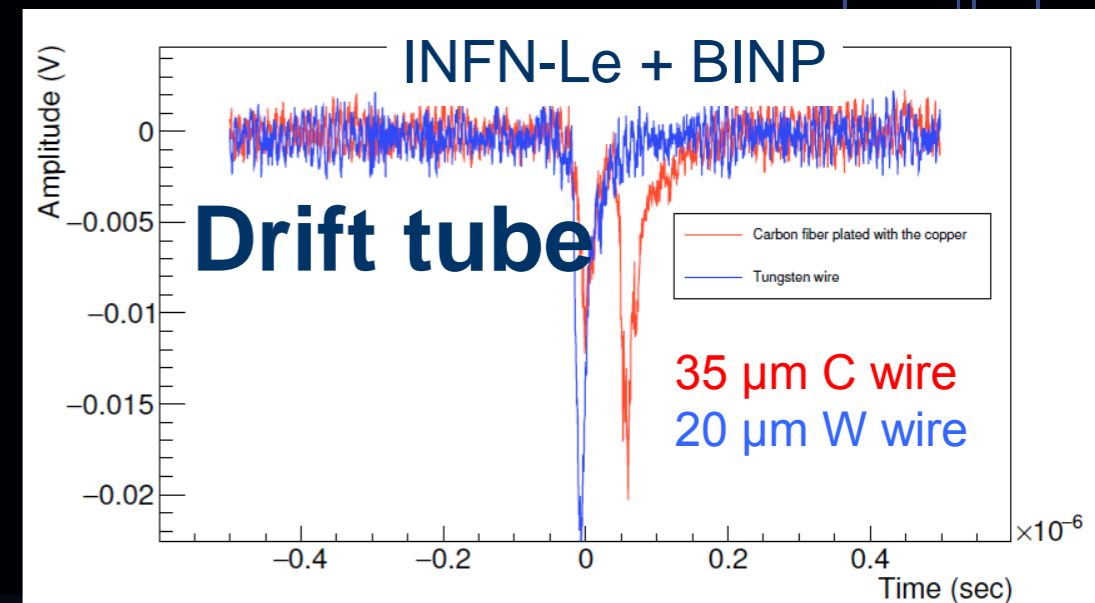
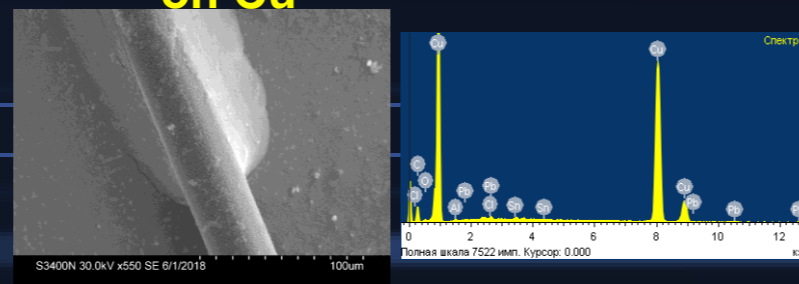


soldering attempt

Lead forms intermetallic compound with gold and completely dissolves the 50 nm Au layer.



good solder wettability on Cu



F. Grancagnolo

C wire soldering without metal coating

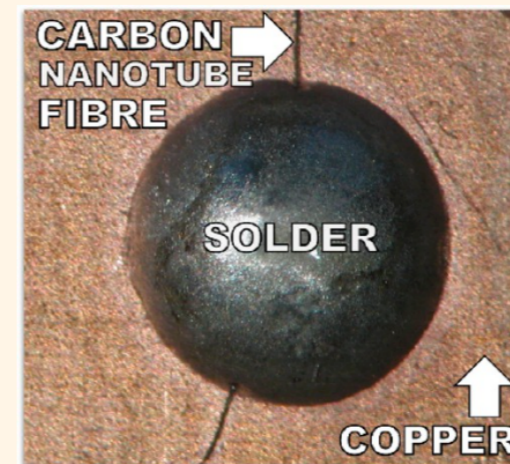
Soldering of Carbon Materials Using Transition Metal Rich Alloys

Marek Burda,^{*,†} Agnieszka Lekawa-Raus,[†] Andrzej Gruszczyk,[‡] and Krzysztof K. K. Koziol^{*,†}

[†]Department of Materials Science and Metallurgy, University of Cambridge, 27 Charles Babbage Road, CB3 0FS, Cambridge, U.K. and [‡]Welding Department, Silesian University of Technology, Konarskiego 18a, 44-100 Gliwice, Poland

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10.1021/acsnano.5b02176

ABSTRACT Joining of carbon materials *via* soldering has not been possible up to now due to lack of wetting of carbons by metals at standard soldering temperatures. This issue has been a severely restricting factor for many potential electrical/electronic and mechanical applications of nanostructured and conventional carbon materials. Here we demonstrate the formation of alloys that enable soldering of these structures. By addition of several percent (2.5–5%) of transition metal such as chromium or nickel to a standard lead-free soldering tin based alloy we obtained a solder that can be applied using a commercial soldering iron at typical soldering temperatures of approximately 350 °C and at ambient conditions. The use of this solder enables the formation of mechanically strong and electrically conductive joints between carbon materials and, when supported by a simple two step technique, can successfully bond carbon structures to any metal terminal. It has been shown using optical and scanning electron microscope images as well as X-ray diffraction patterns and energy dispersive X-ray mapping that the successful formation of carbon–solder bonds is possible, first, thanks to the uniform nonreactive dispersion of transition metals in the tin-based matrix. Further, during the soldering process, these free elements diffuse into the carbon–alloy border with no formation of brazing-like carbides, which would damage the surface of the carbon materials.



- **These gas tracking detectors are proposed for:**
 - **IDEA's preshower**
 - **IDEA's muon detector**
 - **TPC's readout**
- **Large surfaces to be covered**
 - **Industrialization**
- **Cost reduction**
 - **Reduce number of channels**
 - **Cheaper electronics?**

CMS GE2/1 sector μ -RWELL prototype

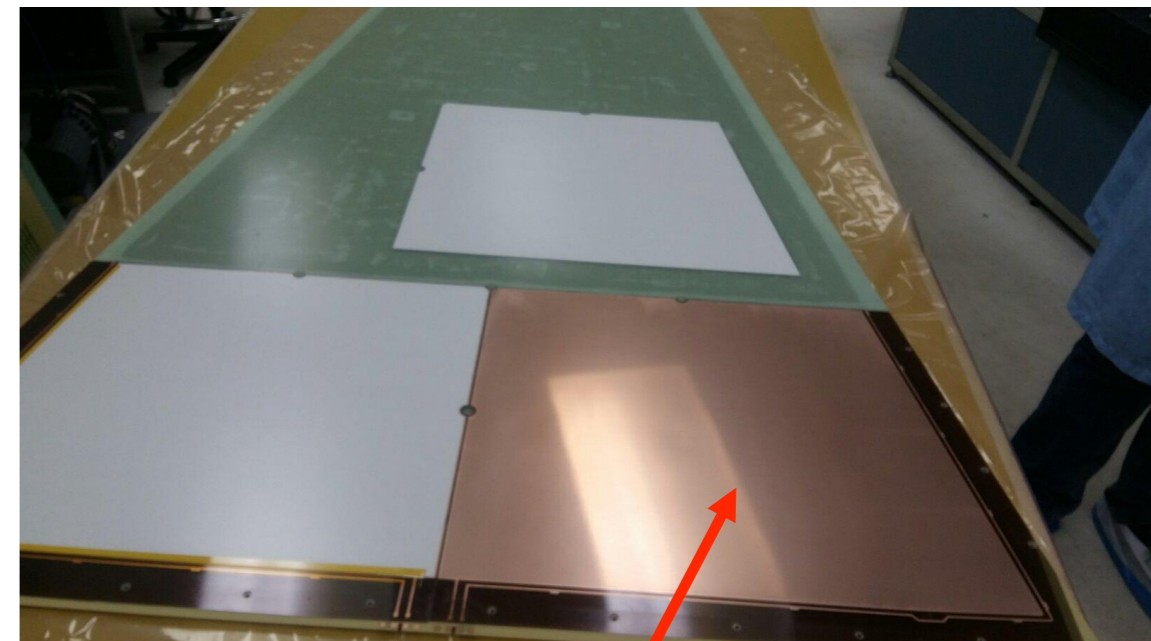


H4 test beam with 150 GeV muons:

- Voltage scan (amplification scan)
- Uniformity scan across the surface of the detector at 530 V (~12000 gain, still to be conditioned)

The **excellent** results obtained demonstrate the great collaboration between INFN-Eltos and Rui de Oliveira's lab

GE2/1 20⁰ sector
with 2 M4 μ RWells
(2 m height, 1.2 m
base)



M4 μ -RWELL

M4 μ -RWELL prototype is a trapezoid of ~55-60x50 cm²

Largest μ -RWELL ever built and operated!

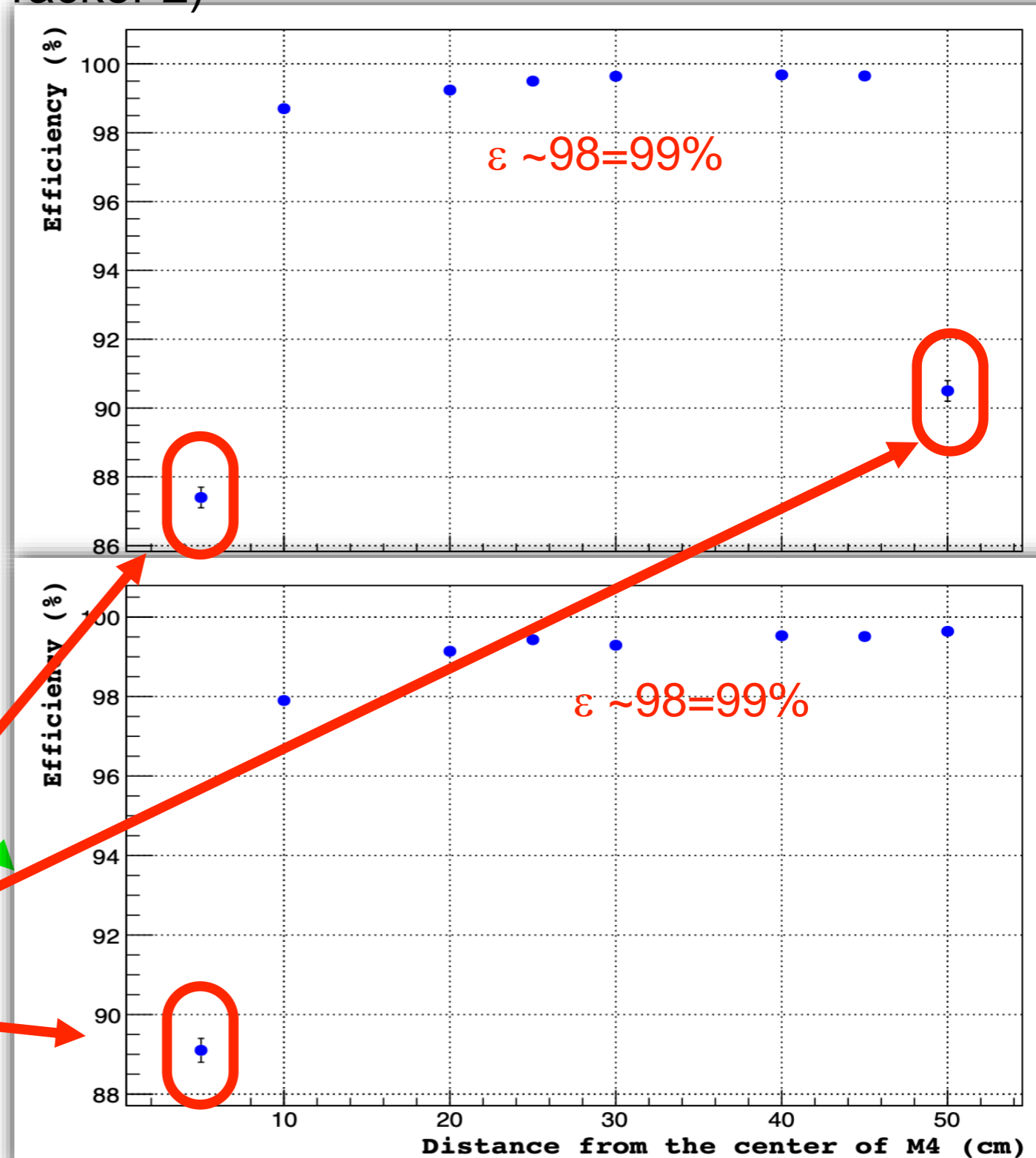
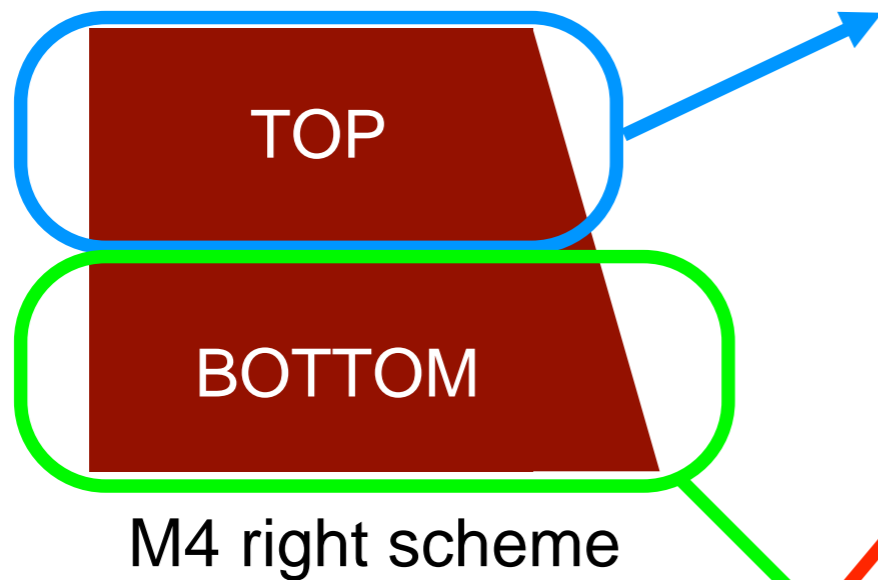
CMS M4 μ -RWELL: homogeneity

Efficiency = $\frac{\# \text{ hits (Tracker 1 \& Tracker 2 \& M4 right)}}{\# \text{ hits (Tracker 1 \& Tracker 2)}}$

M4 right side: $\# \text{ hits (Tracker 1 \& Tracker 2)}$

- ◆ Drift Field = 3.0 kV/cm
- ◆ $V_{\mu\text{-RWELL}} = 530 \text{ V}$

Muon beam



Beam on the edge of the detector
NOT inefficiency!!

R&D programmes

- **There are several R&D programmes that can and should be used for tracking R&D**
- **CERN's EP-RD**
 - **RD51, RD53 and the new R&D lines**
 - **LCTPC, etc.**
 - **Several EU programmes**
 - **The new version of AIDA-2020, AIDA++**
 - **Future experiments at large circular e^+e^- colliders will be one of the top priorities of this programme**
 - **FEST provides travel money to China to collaborate on specific R&D issues**
 - **CREMLIN+ and others**
- **National programmes like ARCADIA, MOST,...**

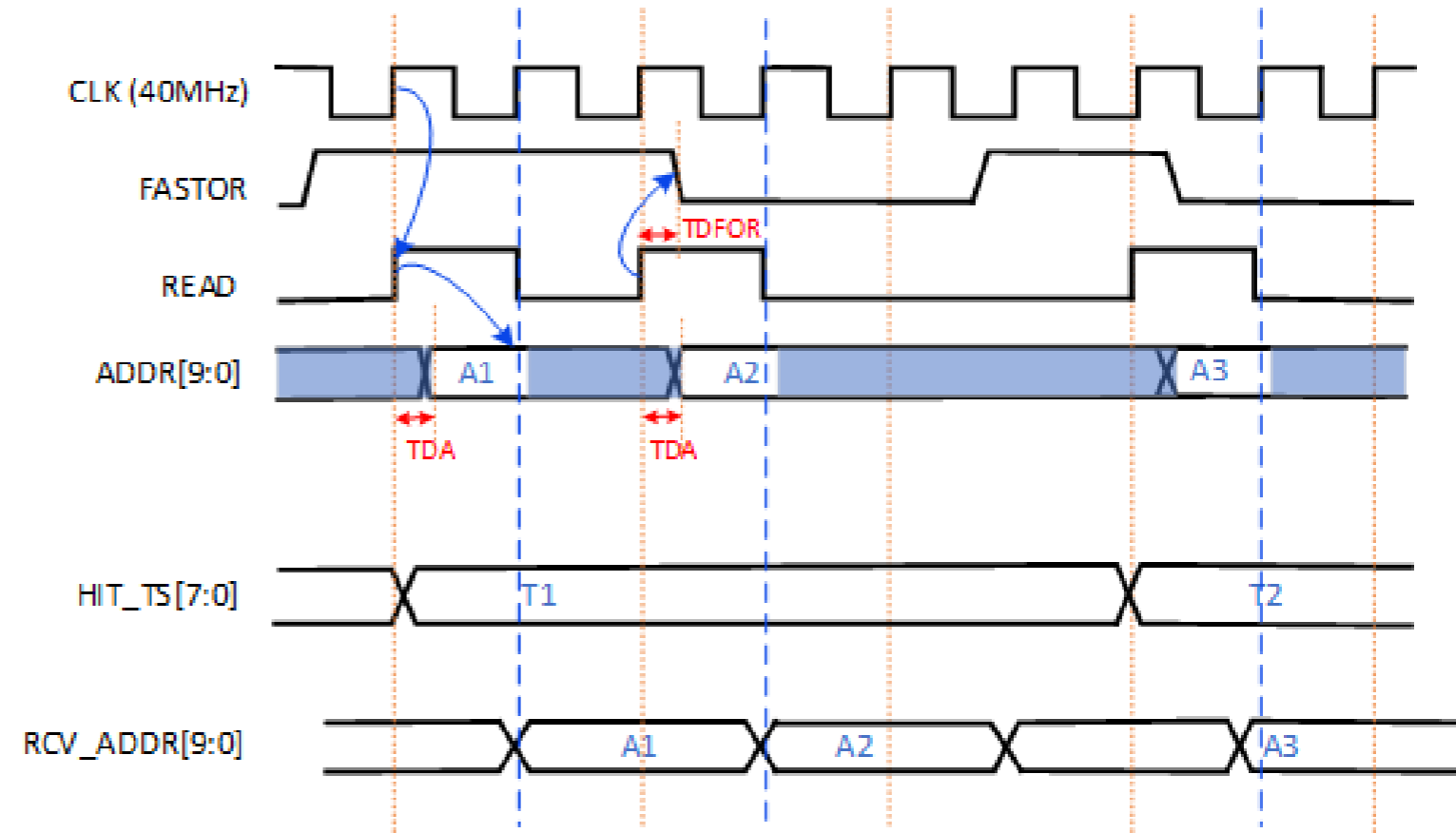
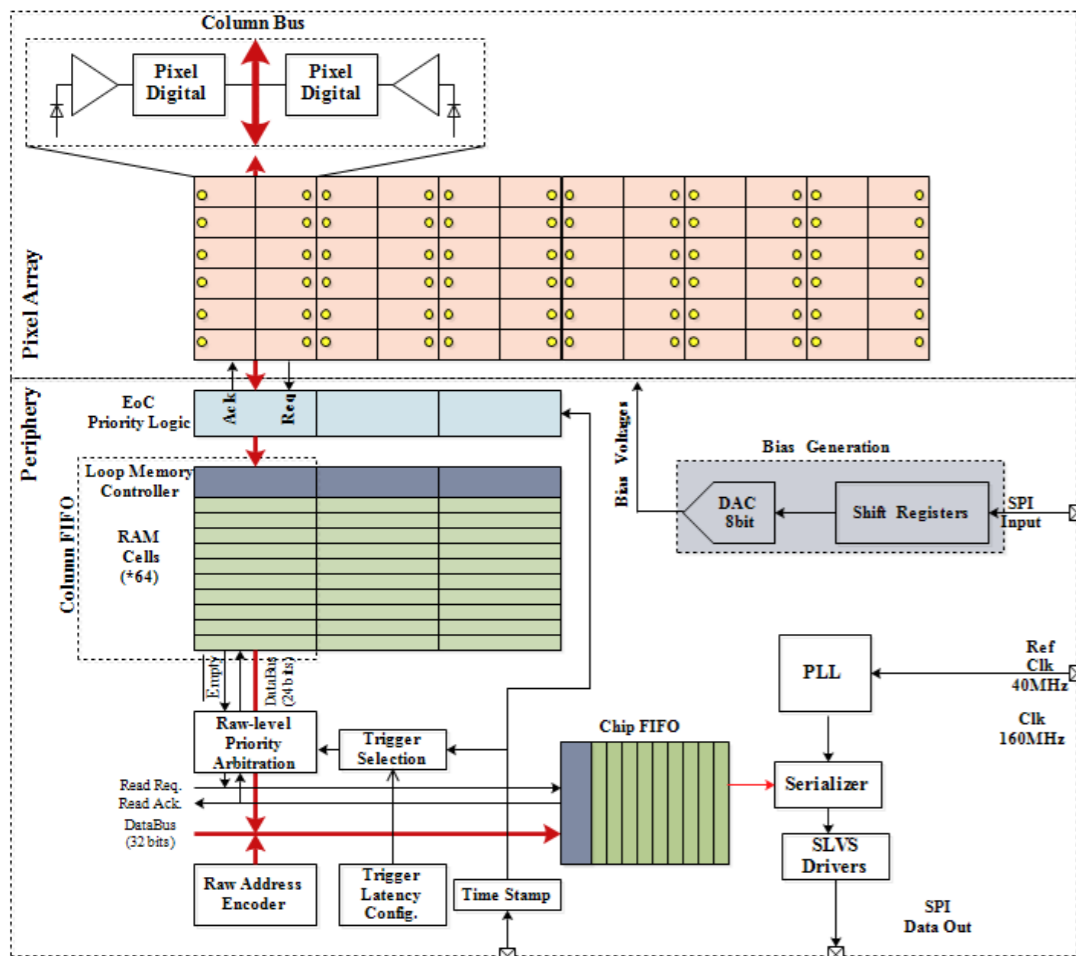
Conclusions

- **Excellent tracking** is one of the most important important detector requirements at CEPC
- Tracking detectors for CEPC could in principle be built with today's technology
- **However**, several issues have to be solved and therefore a strong programme of **R&D is needed**
 - The R&D should lead to construction improvements and cost reductions (industrialization wherever possible)
- Several **R&D programmes** are being put in place right now
 - None of them covers all the needed aspects, so one has to participate and collaborate in several programmes
 - These programmes provide excellent conditions for **synergic collaborations** and are ideal places to form the **new generation of detector experts**

Backup

Vertex detectors: challenges

MOST2 architecture

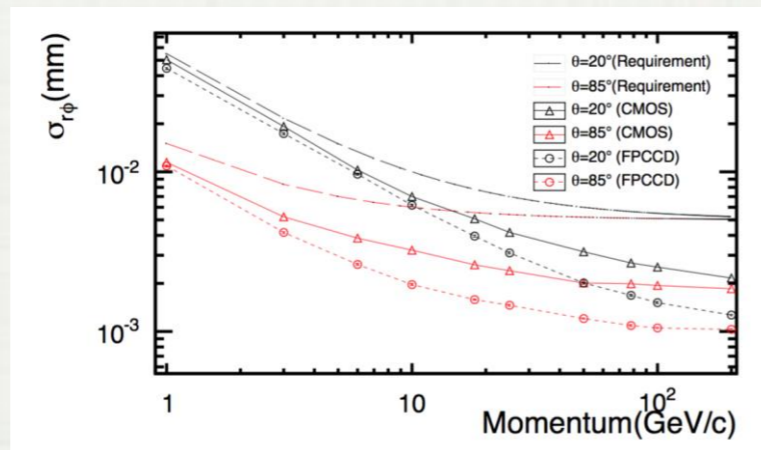


- **Similar to the ATLAS ITK readout architecture: “column-drain” readout**
 - Priority based data driven readout
 - Modification: time stamp is added at EOC whenever a new fast-or busy signal is received
 - Dead time: 2 clk for each pixel (50ns @40MHz clk), negligible compared to the average hit rate
- **2-level FIFO architecture**
 - L1 FIFO: In column level, to de-randomize the injecting charge
 - L2 FIFO: Chip level, to match the in/out data rate between the core and interface
- **Trigger readout**
 - Make the data rate in a reasonable range
 - Data coincidence by time stamp, only the matched event will be readout



The essence of the designing and constructing a **VERTEX DETECTOR**:
fit 1 GigaPixel in a Diet Coke can & keep it cool!

☑ Physics First!



impact parameter resolution

Accelerator	a [μm]	b [$\mu\text{m}\cdot\text{GeV}/c$]
LEP	25	70
SLC	8	33
LHC	12	70
RHIC-II	13	19
ILC	< 5	< 10

ILD DBD 2012

ILD LOI 2009

The ILC figures apply also when you go beyond the linear approximations

- ▶ a depends on the single point resolution and the ratio between the innermost radius and the lever arm:
=> $\sigma_{sp} = 3 \mu\text{m}$ when $R_{in} = 16 \text{ mm}$ and $R_{out} = 60 \text{ mm}$
- ▶ b depends on the multiple scattering at the innermost radius:
=> thickness/layer = 0.15% X_0 [$X_0 = 9.37 \text{ cm}$ for Silicon]

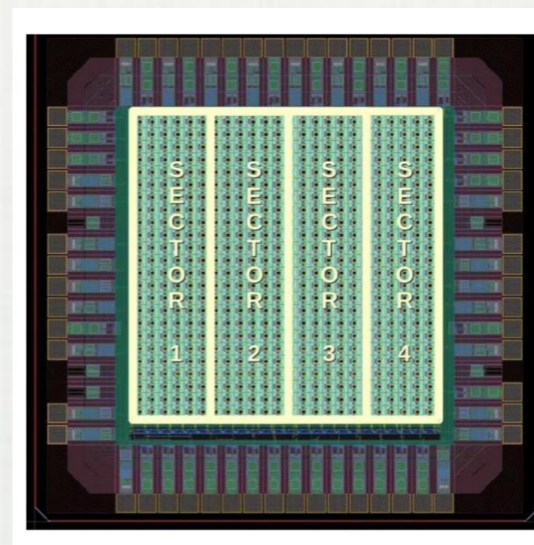
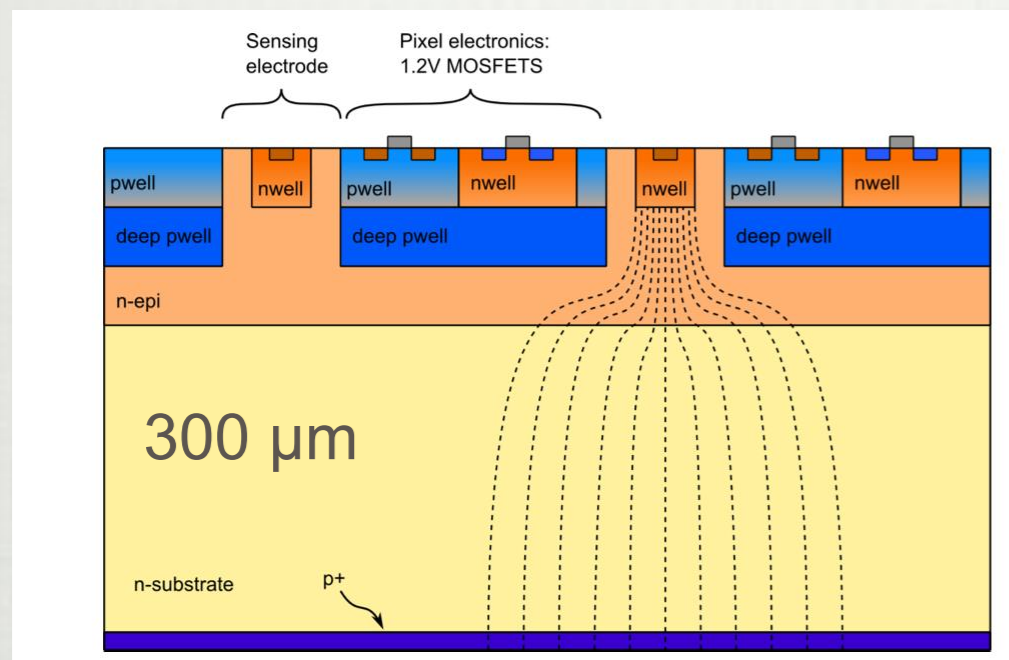
[The ILD and CePC baseline figures]

[140 μm]

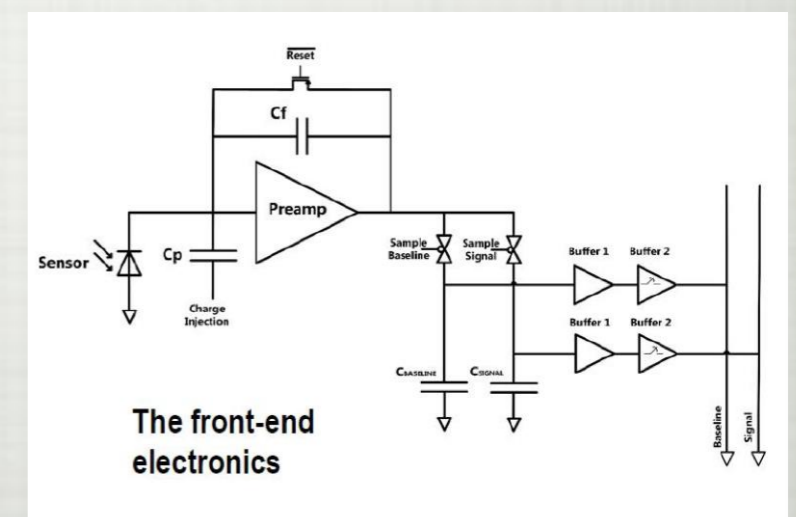
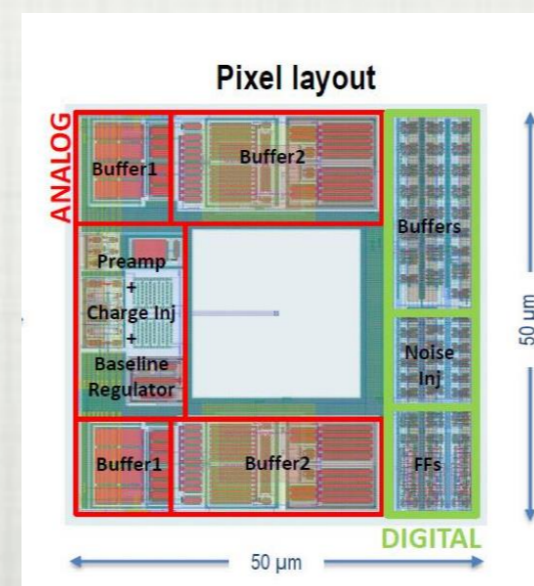
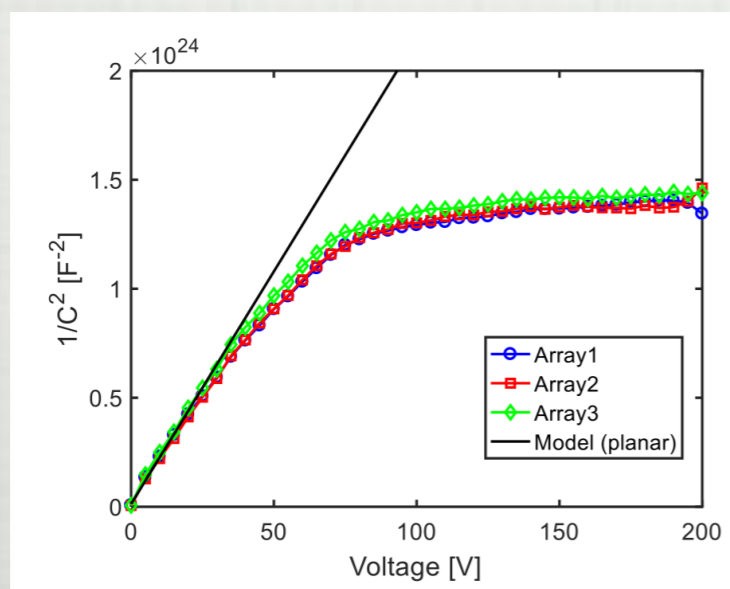
If we look a bit around we know that Monolithic Active Pixel Sensors (MAPS) are a good starting point:

* and new technologies based on high resistivity substrates are very appealing:

The INFN SEED (Silicon with Embedded Electronics Development, partnership with LFour



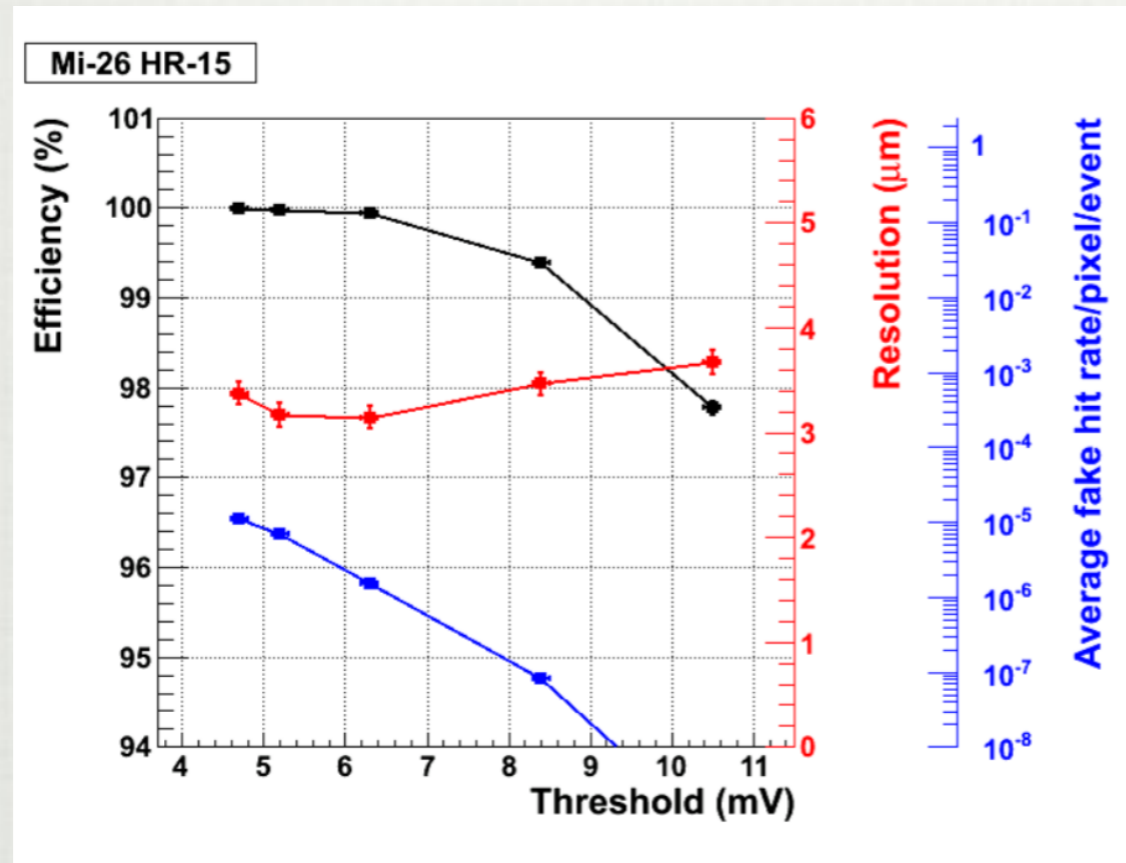
- ▶ die area 2x2 mm²
- ▶ 24x24 pixel array
- ▶ Equivalent Noise Charge: 50 e-rms at room T



S. Panati et al. , IEEE-NSS 2017 Conf. record

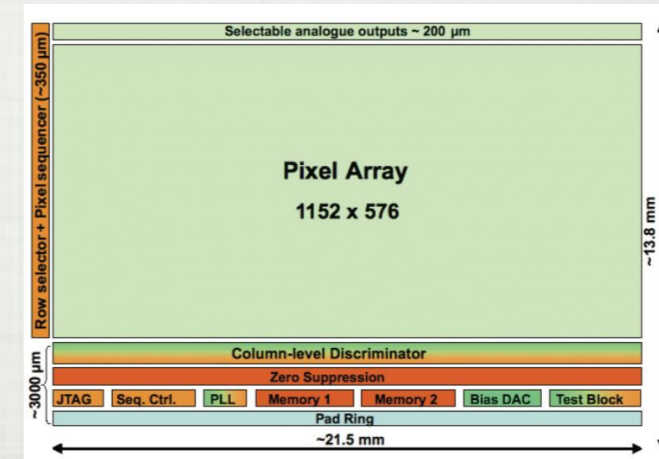
If we look a bit around we know that Monolithic Active Pixel Sensors (MAPS) are a good starting point:

- * MAPS have been shown to be able to provide the required resolution with a binary readout



Test beam results for the MIMOSA-26 sensor:

- * 18.4 μm pitch (5.3 μm binary resolution)
- * rolling shutter & end-of-column zero suppression (200 ns/pixel r.o. time)
- * **250 mW/cm² power consumption**



M. Winter et al., arXiv: 1203.3750v1 (2012)

The pitch/ $\sqrt{12}$ rule has been violated

☑ The machine comes next; and we have to account for

▶ the time structure of the beams:

at the CepC, collisions are equally spaced (in time) with a frequency depending on the number of bunches. In one of the configurations reported in Beijing-201609, we have:

- 50 bunches at the Higgs factory energy
- 5000 bunches at the Z factory energy [where I estimated 4 kHz event rate]

for a beam Xing every 5 μ s (@Higgs) to 50 ns (@Zpole) [3.6 μ s is the “official” number]

▶ the expected Beam-induced background:

there is actually NO solid rock number and estimates have a significant dependence on the machine & final focus parameters (HongBo, 2018, Roma).

A rough figure says ≈ 2.5 hits/cm²/Xing (I believe @Higgs energies)

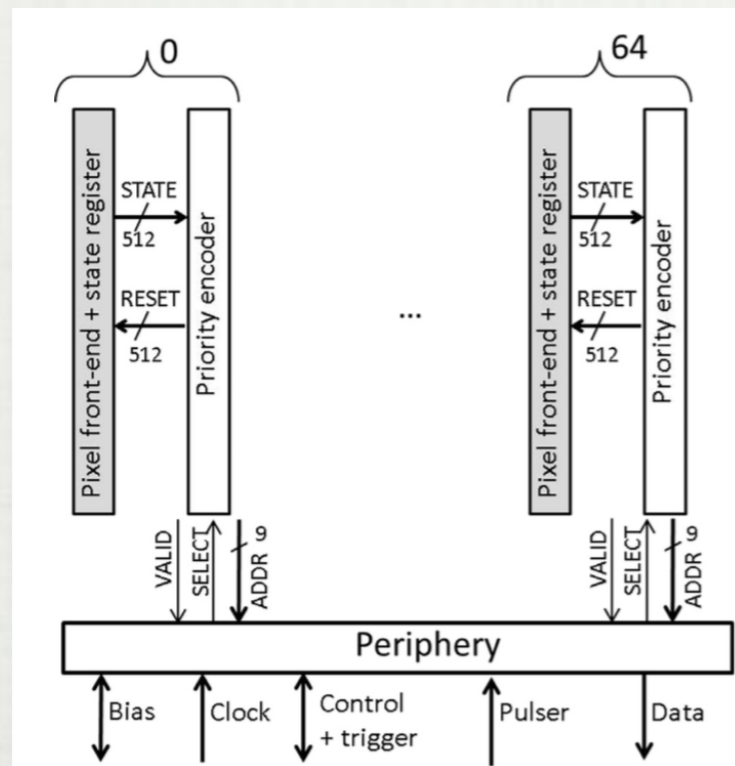
BUT:

- having the spectrum of the bckg particles is important to see if we have “loopers”
- we have to see how it scales with the energy

▶ the expected radiation level: RELAX!

If we look a bit around we know that Monolithic Active Pixel Sensors (MAPS) are a good starting point:

- * sophisticated architectures with ON PIXEL sparsification have been designed and qualified

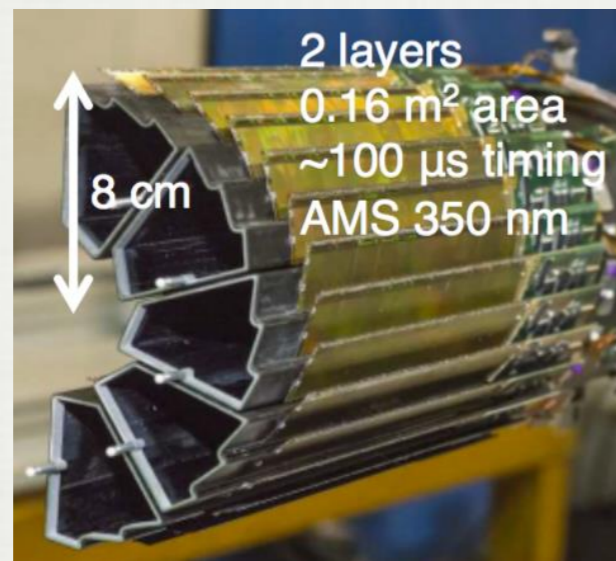


- ▶ 1 discriminator/pixel + 1 bit memory cell
---> analog info locally processed
- ▶ the integration time is independent from read-out (r.o.) time
- ▶ the r.o. time is dependent from the pixel occupancy
- ▶ **current power consumption at the level of 50 mW/cm² (ALPIDE)**

-NIM A 765 (2014) 177 + A 785 (2015) 61
-pixel 2014 proceedings published on JINST
(doi:10.1088/1748-0221/10/03/C03030)

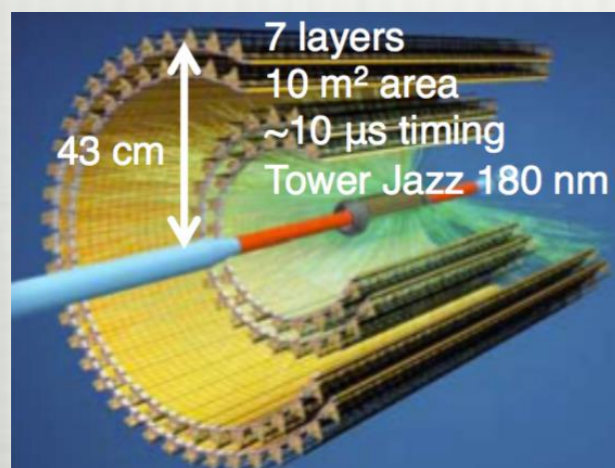
If we look a bit around we know that Monolithic Active Pixel Sensors (MAPS) are a good starting point:

* large systems have been designed and commissioned (or will be, in a short while):



- ▶ 400 sensors
- ▶ 0.9 Pixel each
- ▶ power dissipation 170 mW/cm²

nothing but a toy compared to what is envisaged for the ITS of the **ALICE** experiment:



	σ_{sp}	$t_{r.o.}$	Dose	Fluency	T_{op}	Power	Active area
STAR-PXL	$< 4 \mu m$	$< 200 \mu s$	150 kRad	$3 \cdot 10^{12} n_{eq}/cm^2$	30-35°C	160 mW/cm ²	0.15 m ²
ITS-in	$\lesssim 5 \mu m$	$\lesssim 30 \mu s$	2.7 MRad	$1.7 \cdot 10^{13} n_{eq}/cm^2$	30°C	$< 300 mW/cm^2$	0.17 m ²
ITS-out	$\lesssim 10 \mu m$	$\lesssim 30 \mu s$	100 kRad	$1 \cdot 10^{12} n_{eq}/cm^2$	30°C	$< 100 mW/cm^2$	$\sim 10 m^2$

a development based on:

- ▶ new technologies (Tower-Jazz 180 nm)
- ▶ and new design (on pixel sparsification)

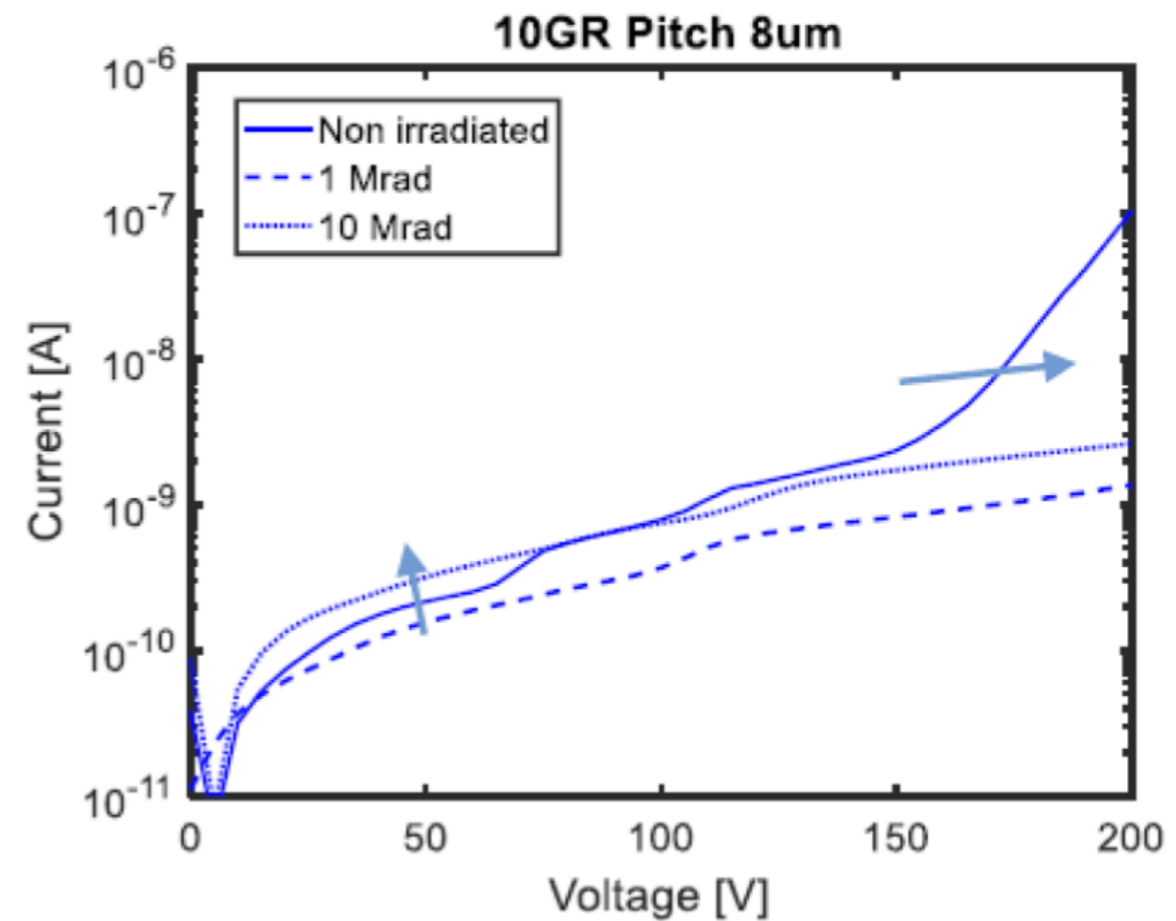
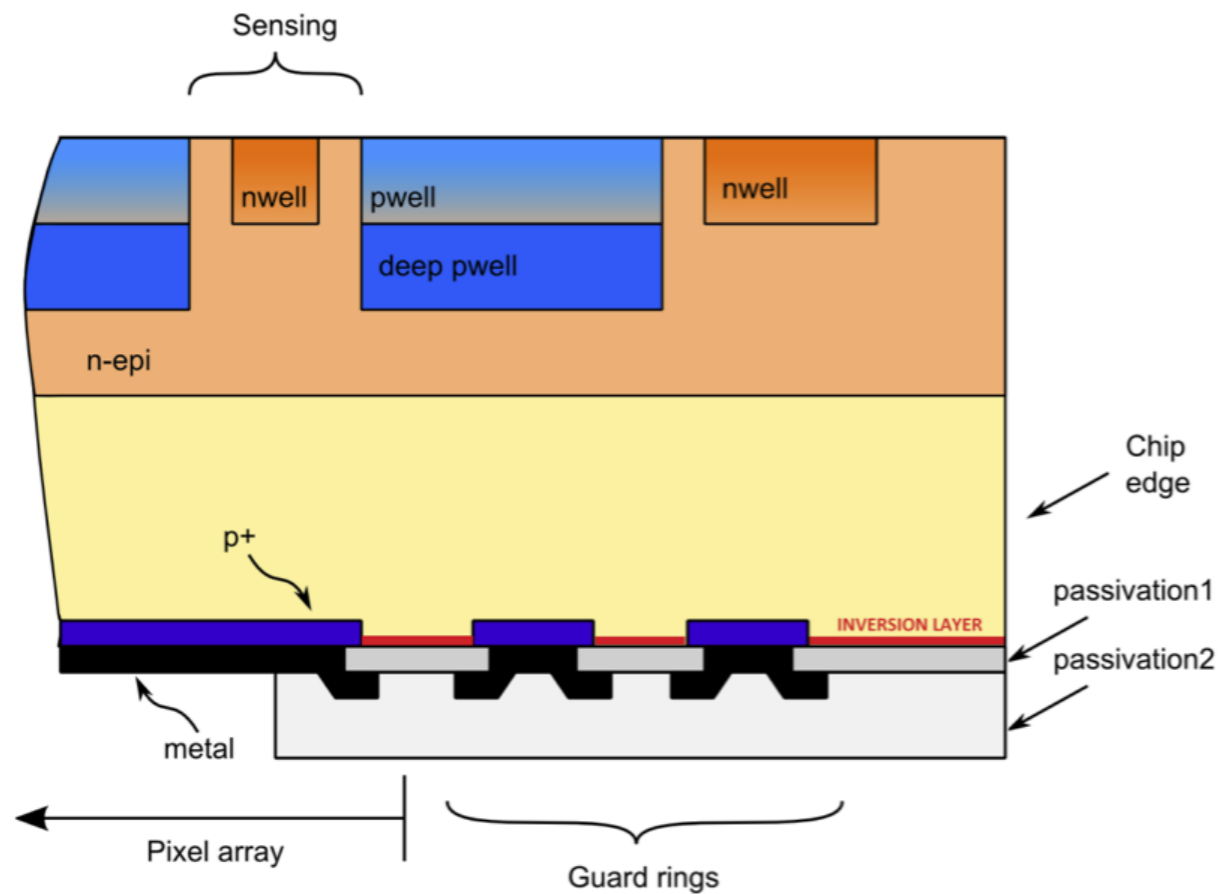
Vertex Detector Conclusions:

- * The new technologies certainly offer unprecedented opportunities
- * Running conditions at the Z shall be carefully considered in designing the detector
- * the real CHALLENGE, to me, will be designing an architecture providing the required data evacuation rate with the MINIMUM power dissipation (<20 mW/cm²), resulting by an optimisation of the ANALOG CELL, the digital architecture, the clock distribution

But I'm confident that fun and excitement will exceed pain & fear!

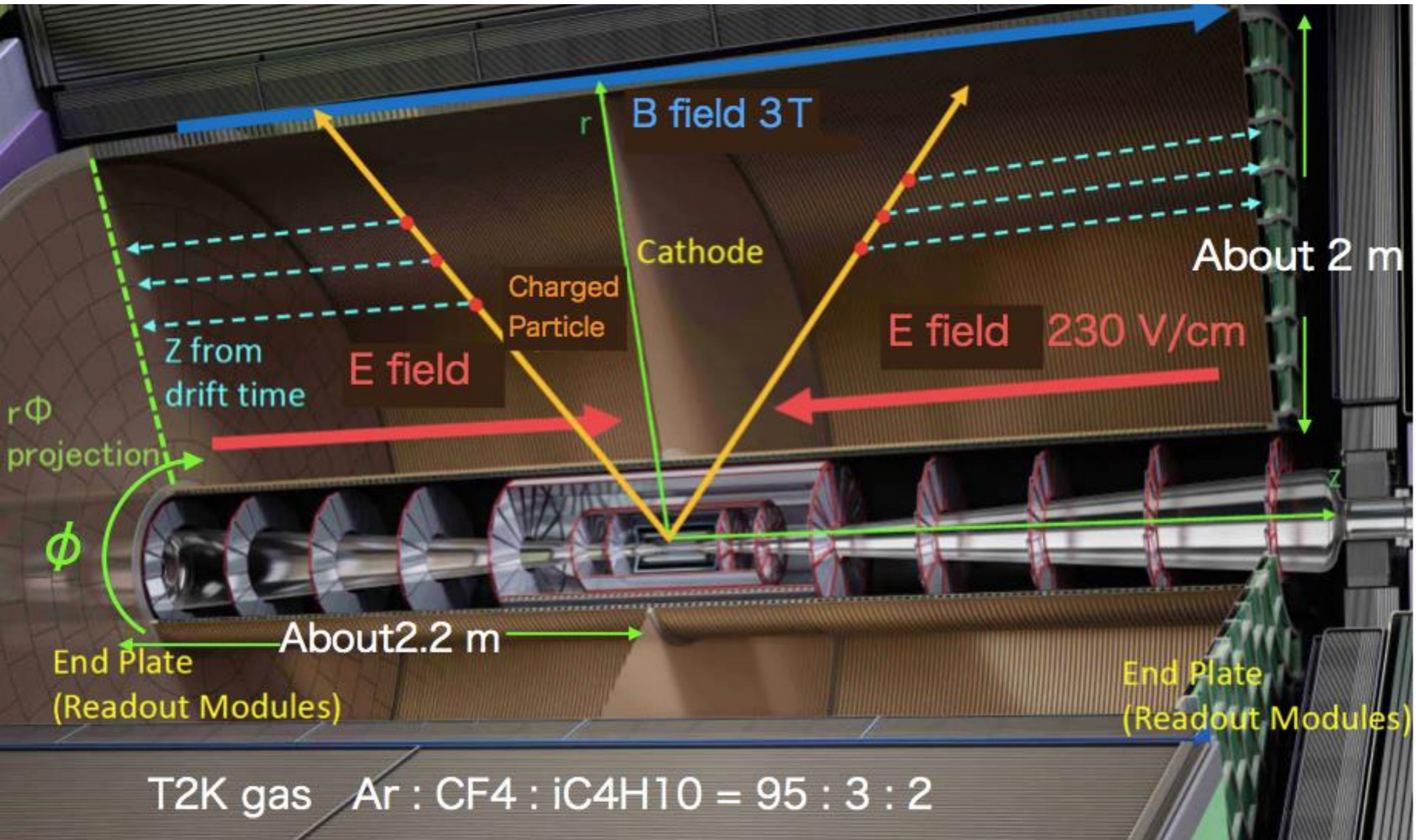
Engineering run by summer 2020

- Pixel size between **10 μ** and **100 μ** ;
- embedded electronics with sparsed readout;
- binary readout modality for **maximum rate** capability, or
- analogue sampling on-pixel, digitisation on periphery;
- **data-driven readout** and low-power digital architecture for data and control signal transmission;
- modular architecture for a straightforward **scaling of the design to a reticle-size** sensor



- Several **test structures** with different **guard-ring** design
- **Inversion layer** may compromise **guard-rings**
- Can be partially **cured** with **irradiation**
- Cause **understood** and **fixed** in the next release just delivered by the foundry

TPC concept



Central trackers: TPCs

e^+e^- machine

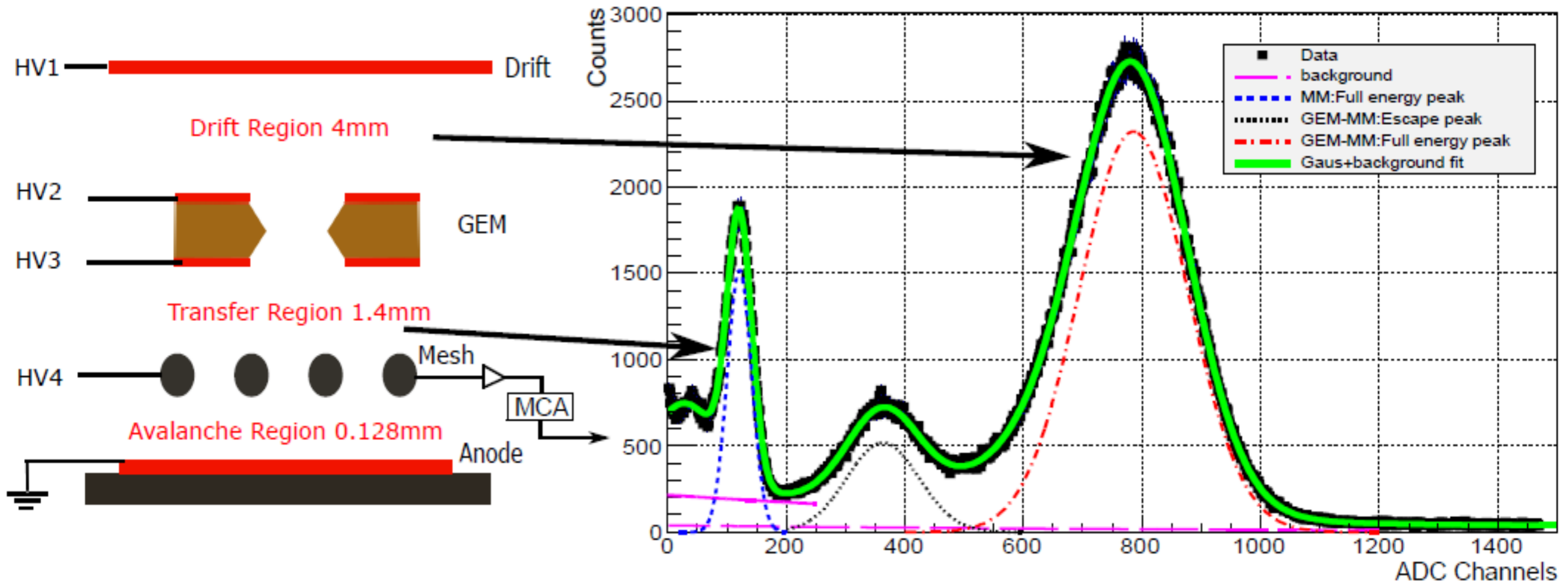
Primary N_{eff} is small: ~ 30

Pad size: $1 \text{ mm} \times 6 \text{ mm}$

Photo peak and escape peak are clear!

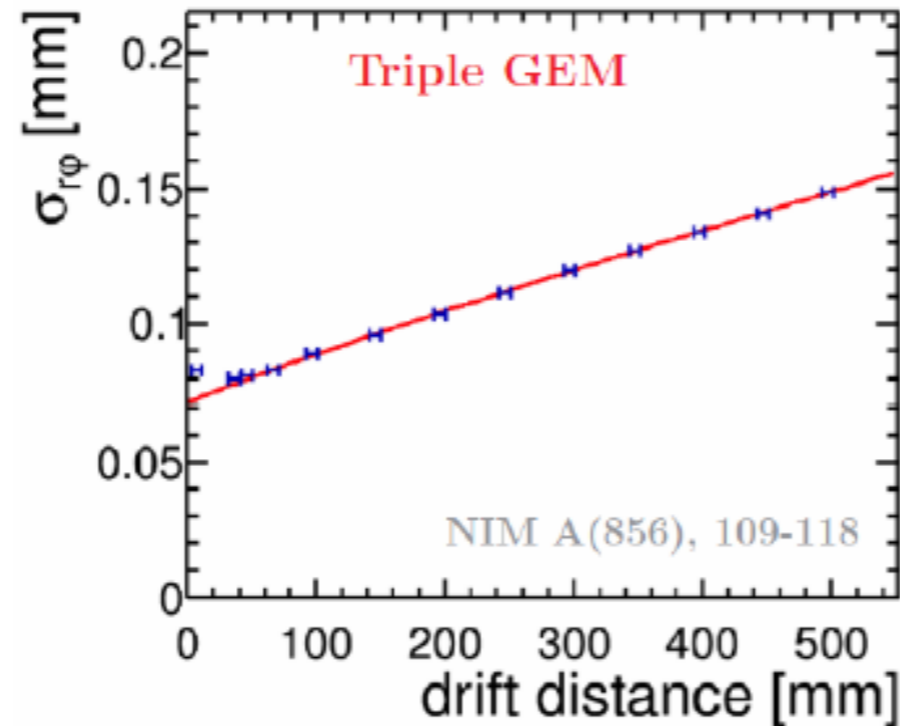
Good electron transmission.

Good energy resolution.

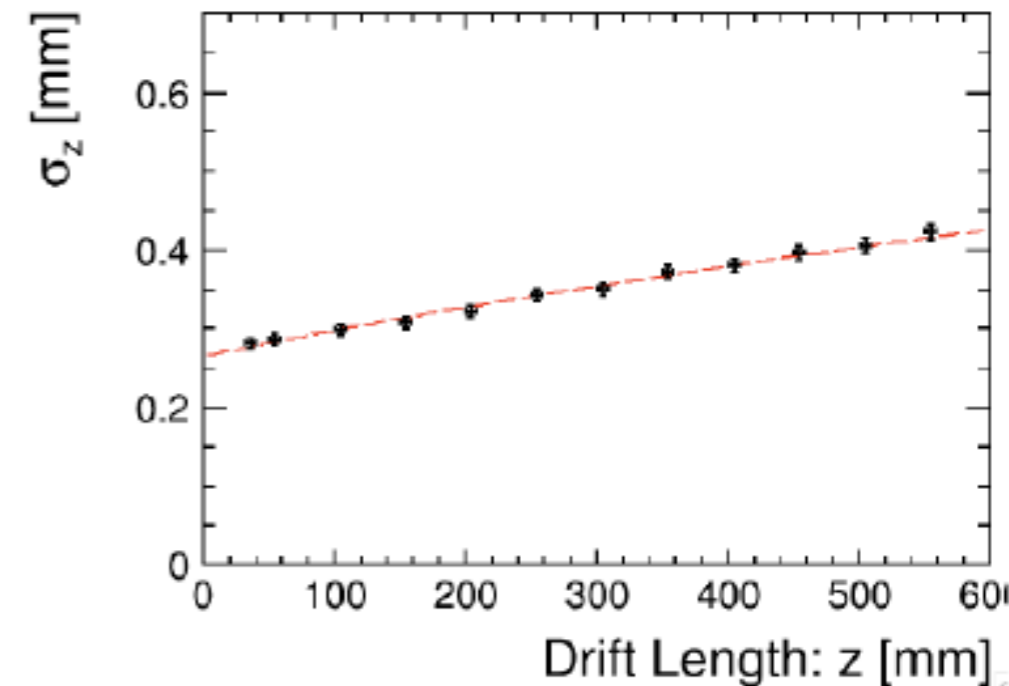
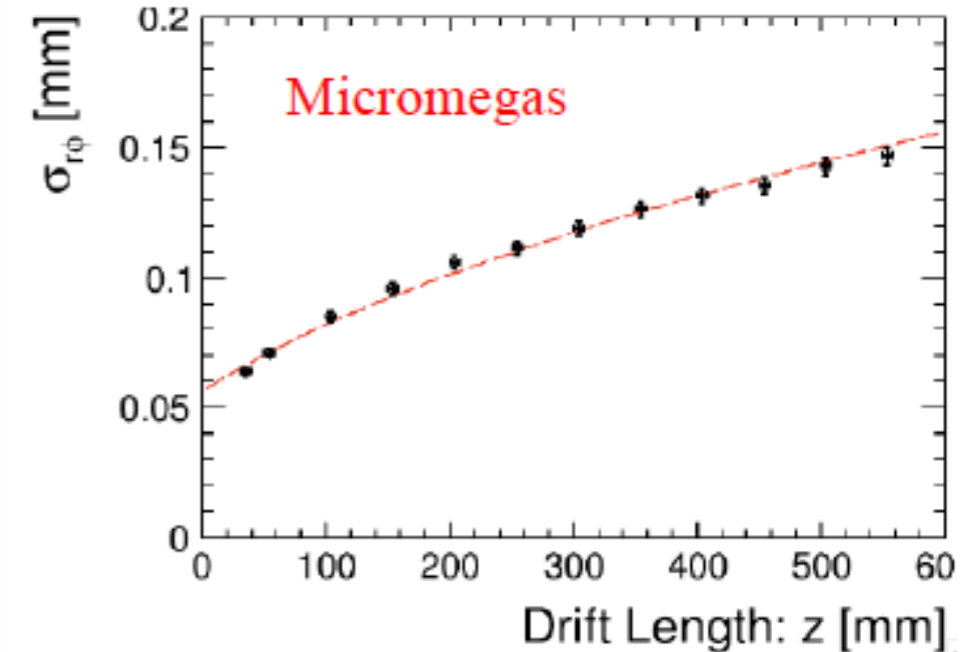


Resolution challenge

T. Ogawa, F. Müller



average of 24 Rows



The resolution goal is now proven with all technologies (GEM, Micromegas and Pixels)

For GEMs, it requires ~ 1 mm pads with enough diffusion in the amplification device.

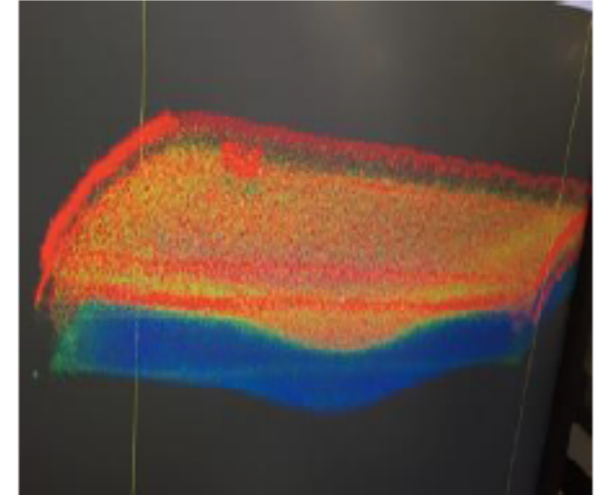
For Micromegas, it requires charge spreading by a resistive-capacitive anode.

For pixels, it requires $< 300\mu\text{m}$ pitch digital readout.

Paul Colas

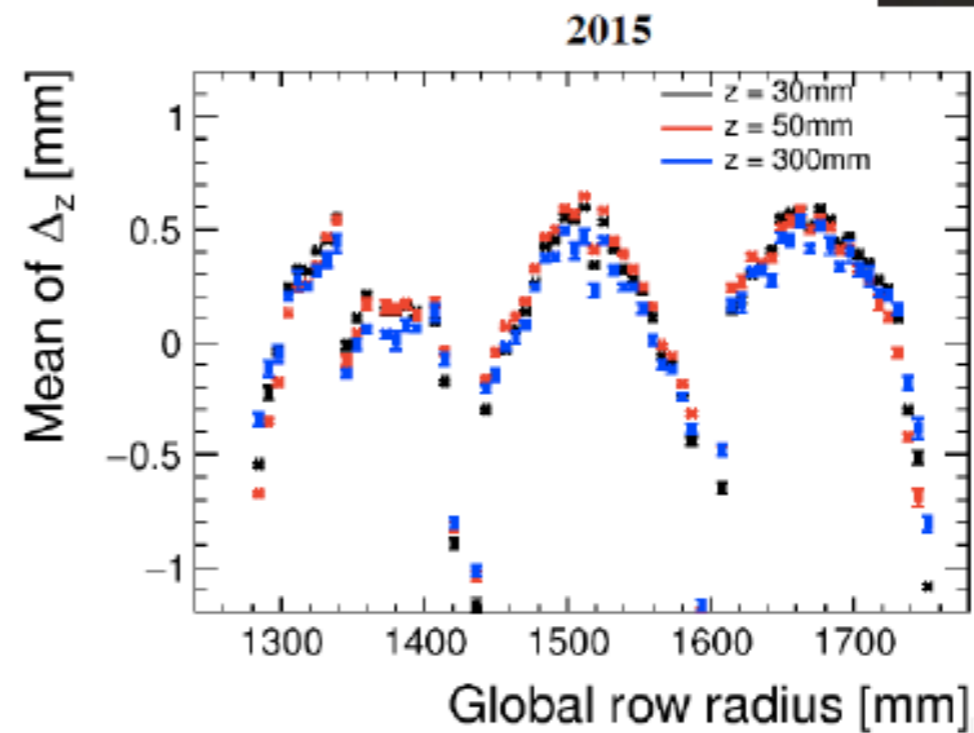
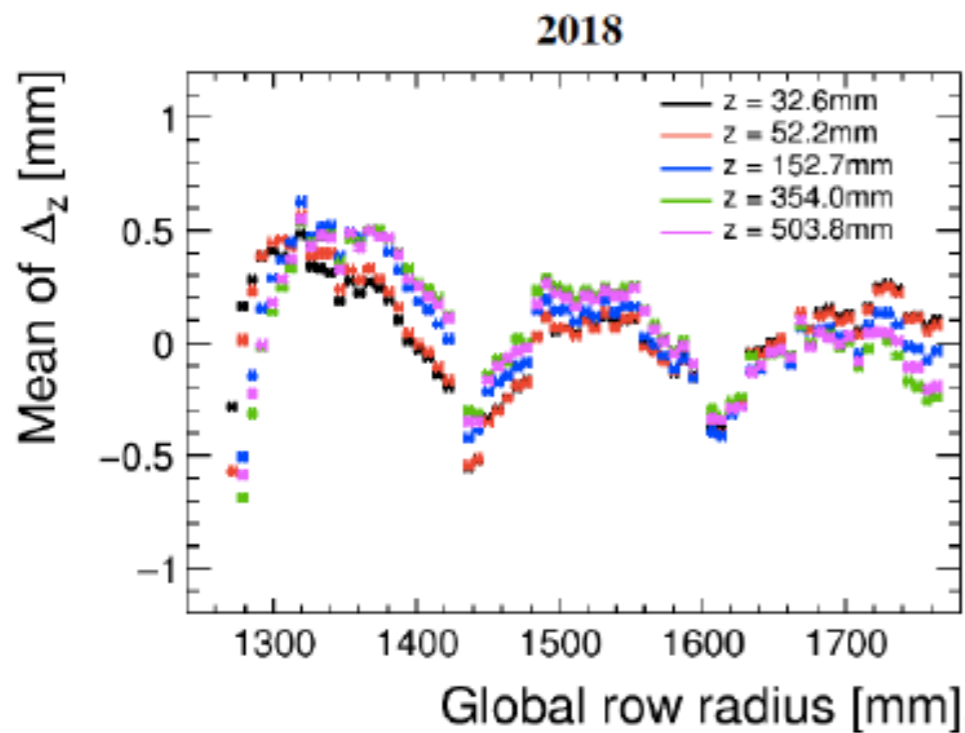
The distortion challenges : 1) Module flatness

The modules have to be extremely flat. they can be deformed by the pressure if they are not rigid enough. This gives rise to ExB effects.



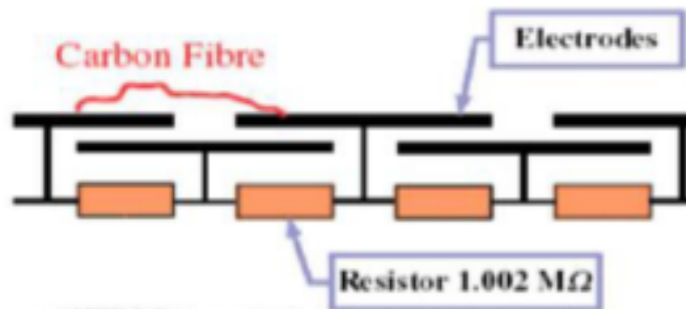
Residual in Z (2018 and 2015 MM)

Data : $E_d=230\text{V/cm}$, $B=0\text{ T}$

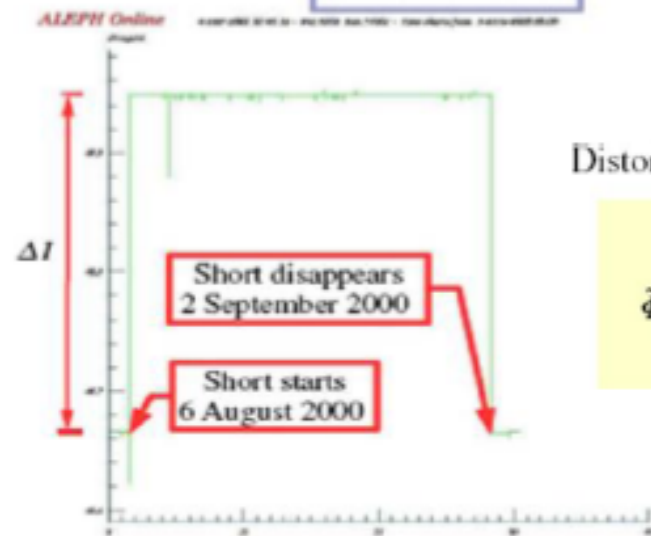


The distortion challenges : 2) field cage quality

- A simple short between two field shaping rings (as happened in ALEPH due to a tiny carbon fiber) can make a sizeable distortion



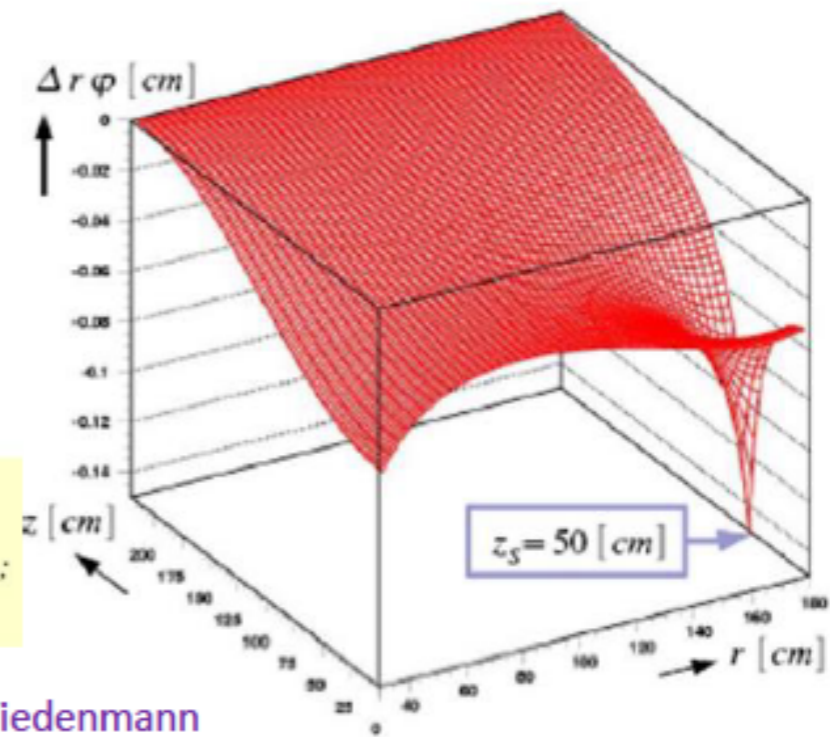
- Correct for distortion
- Remove the fiber



Distortionpotential

$$\tilde{\Phi}(r, \varphi, z) \simeq \text{sign}(z_s) \left(\frac{\Delta U_0}{U_0} \right) \sum_n \frac{\cos\left(\frac{n\pi}{z_M} z_s\right)}{n\pi} \sin\left(\frac{n\pi}{z_M} z\right) P_{\text{FCin}}^{\text{FCin}}\left(\frac{n\pi}{z_M} r\right);$$

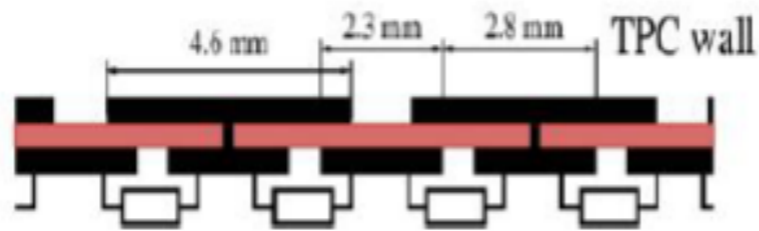
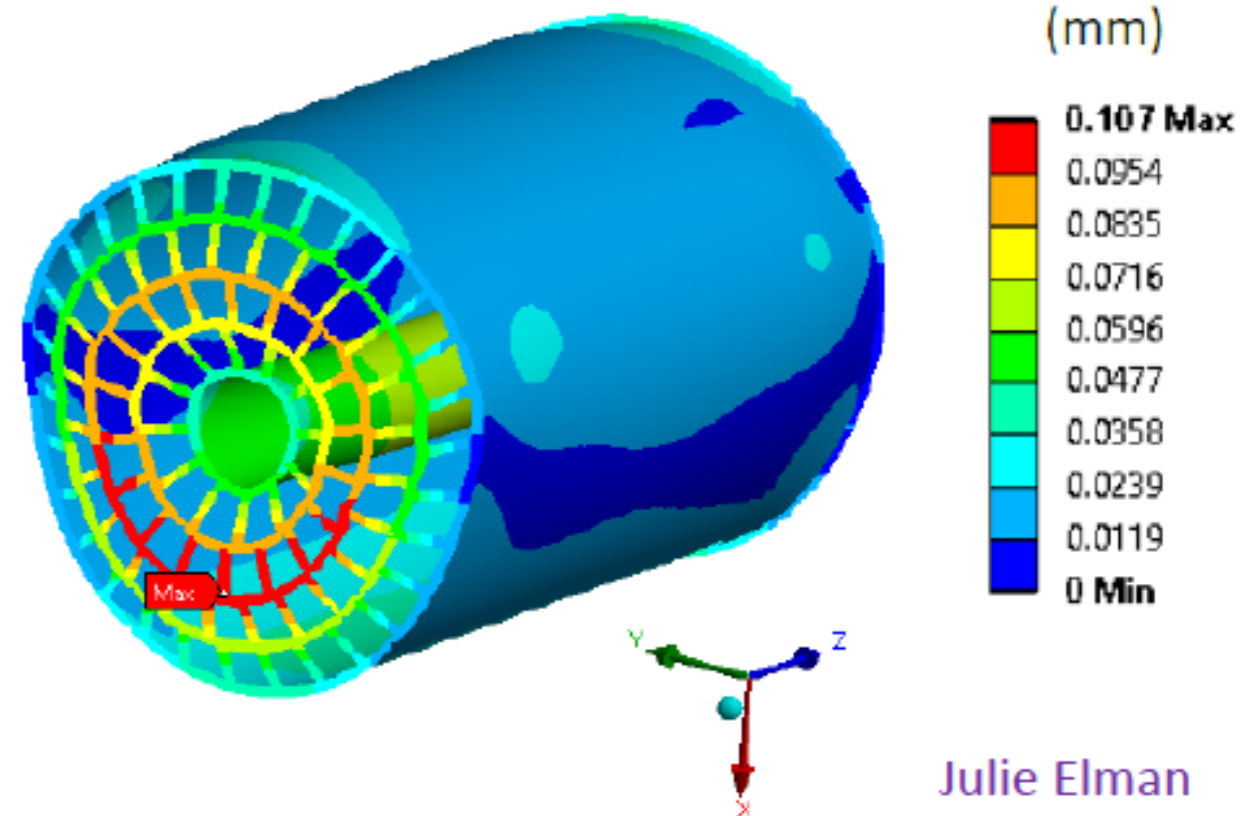
Ron Settles, Werner Wiedenmann



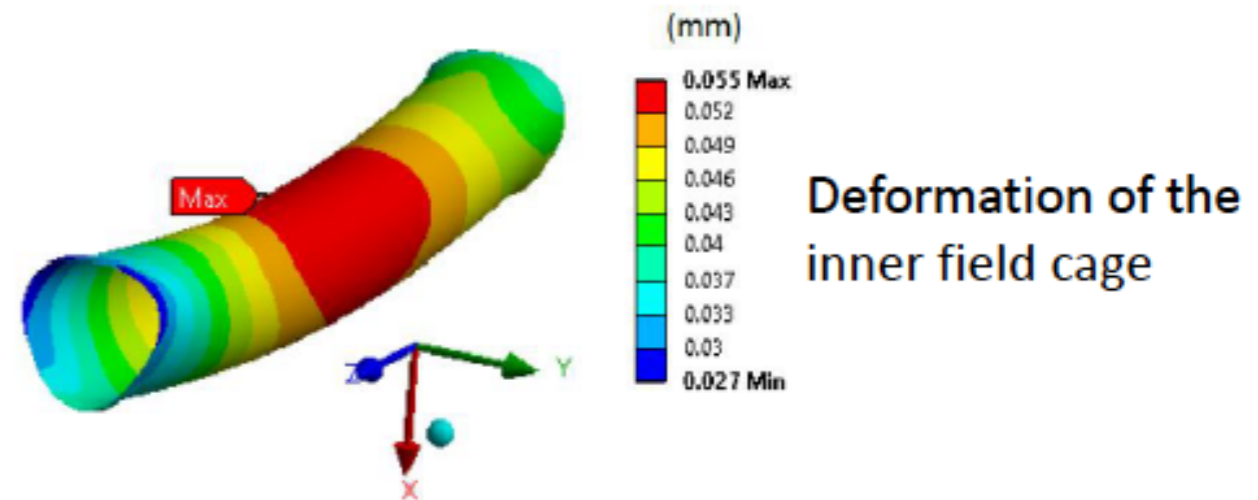
Mechanical challenges

The mechanical design must ensure small enough deformations under weight and pressure, and electric field homogeneity at the 10^{-4} level.

This imposes tough constraints on the field cage rigidity, on the design (mirror strips), and on the suspension



Peter Schade



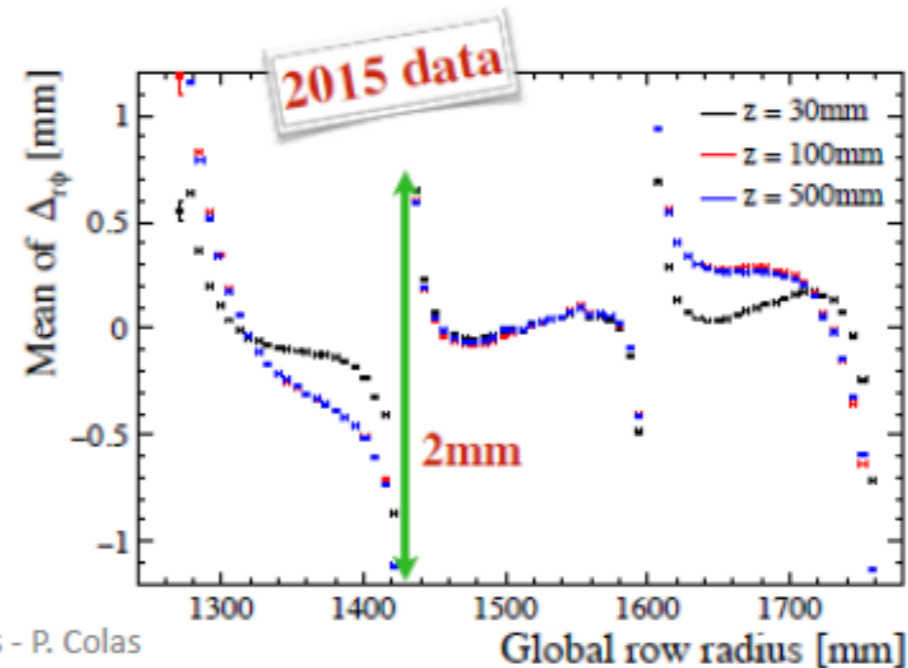
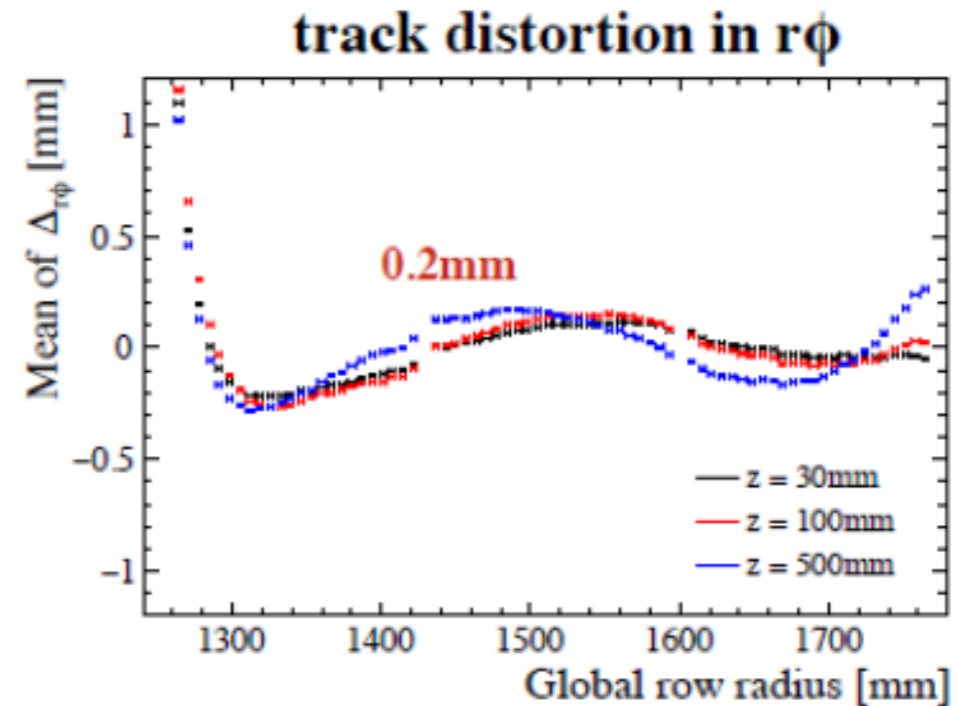
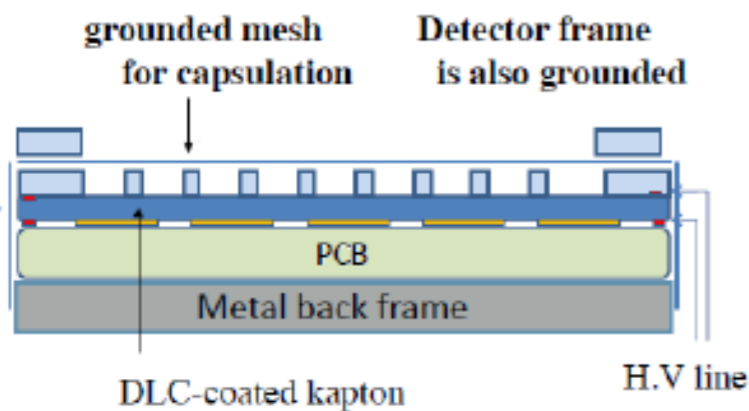
Paul Colas

The distortion mitigation challenge : 3) module edges

T. Ogawa, S. Ganjour

By grounding the mesh and encapsulating the anode at a positive potential, the amplification plane is an almost perfect equipotential, which allows the E-field to be very uniform, even close to the module boundary.

A reduction by an order of magnitude of the ExB distortions is observed.



16/04/2019

TPC technological Challenges - P. Colas

10

Paul Colas

The dE/dx challenge

dE/dx is an essential tool for particle identification, necessary in b physics and in Higgs physics.

It has been proven to be possible with the 3 technologies (Micromegas, GEM and pixels)

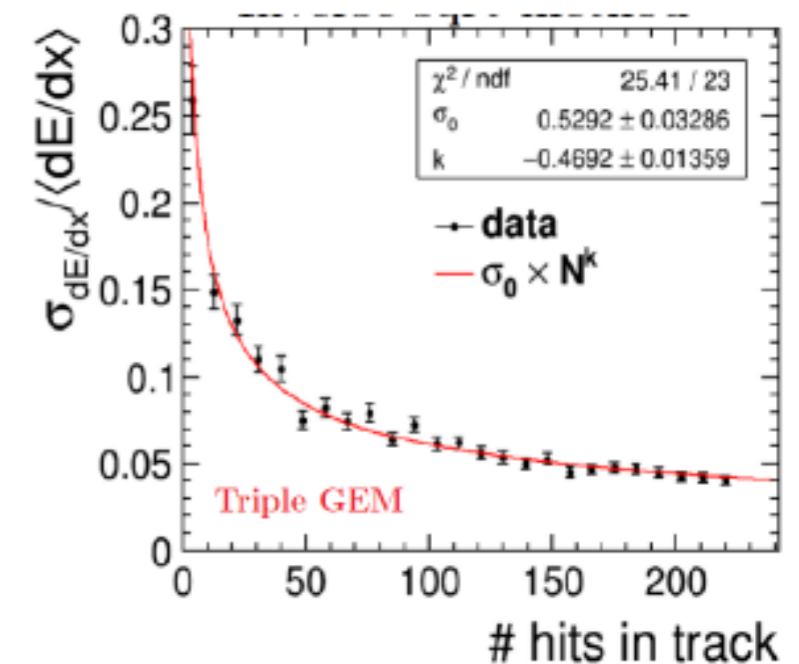
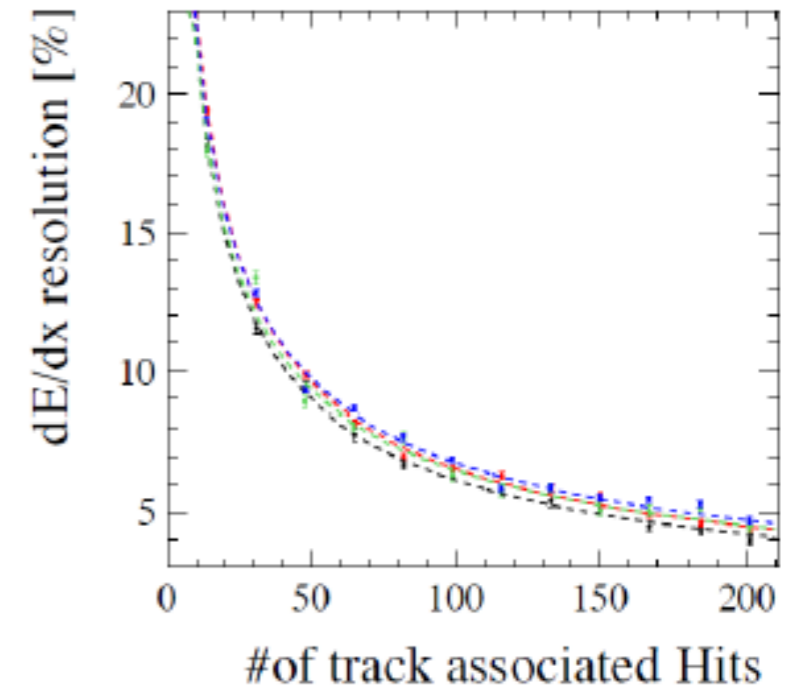
Pixel allow cluster counting, which improves the achievable resolution.

For 1.35 m electron tracks, we obtain:

4.6 % for Micromegas

4.5 % for GEMs

3.5 % for pixels



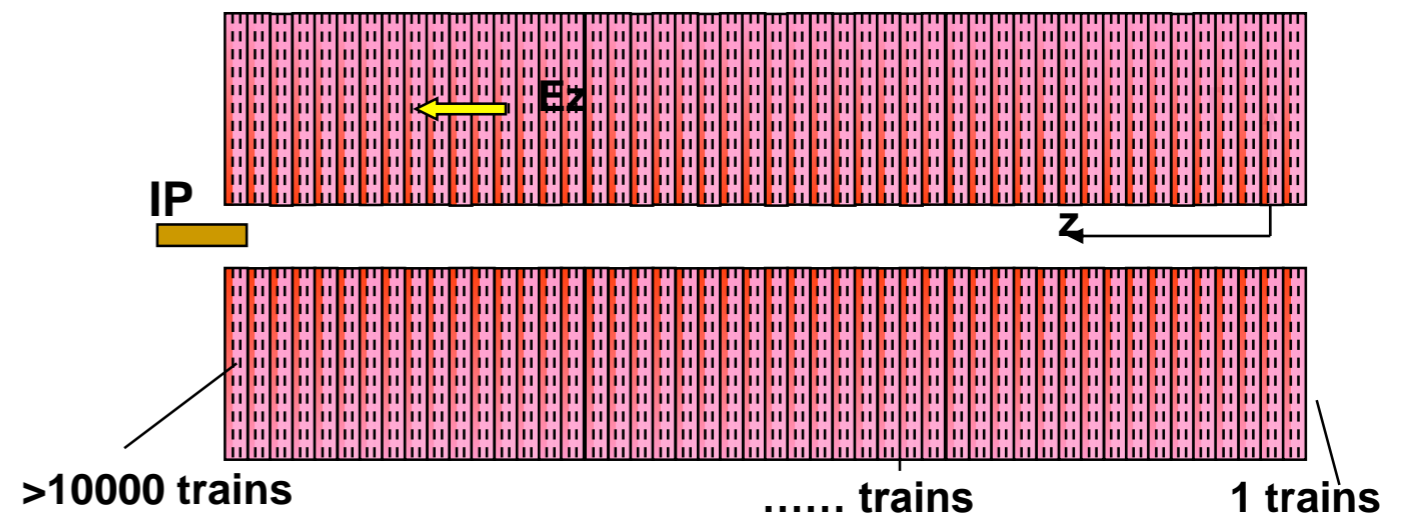
Paul Colas

The ion backflow challenge

- The possibility of gating exists only at ILC. For other colliders (continuous beam or high rate bunch crossings) gating is not possible.
- There is a natural ion backflow suppression in Micromegas, but not sufficient at the Z.
- Other possibilities are Double meshes (??), or a new anode microstructure with hole by hole defocusing amplification field : NEEDS R&D!
- More with ALICE upgrade and TPC at RHIC. More at MPGD19 at La Rochelle.

Ion Back Flow and Distortion

- **Goal:**
 - **Operate TPC at high luminosity at Z pole run**
 - **No Gating options**
- **IBF control similar with ALICE TPC upgrade**
- **~100 μm position resolution in $r\phi$**
- **Distortions by the primary ions at CEPC are negligible**
- **Manu ions discs co-exist and distorted the path of the seed electrons**
- **The ions cleaned during the ~us period continuously**
- **Continuous device for the ions**
- **Long working time**



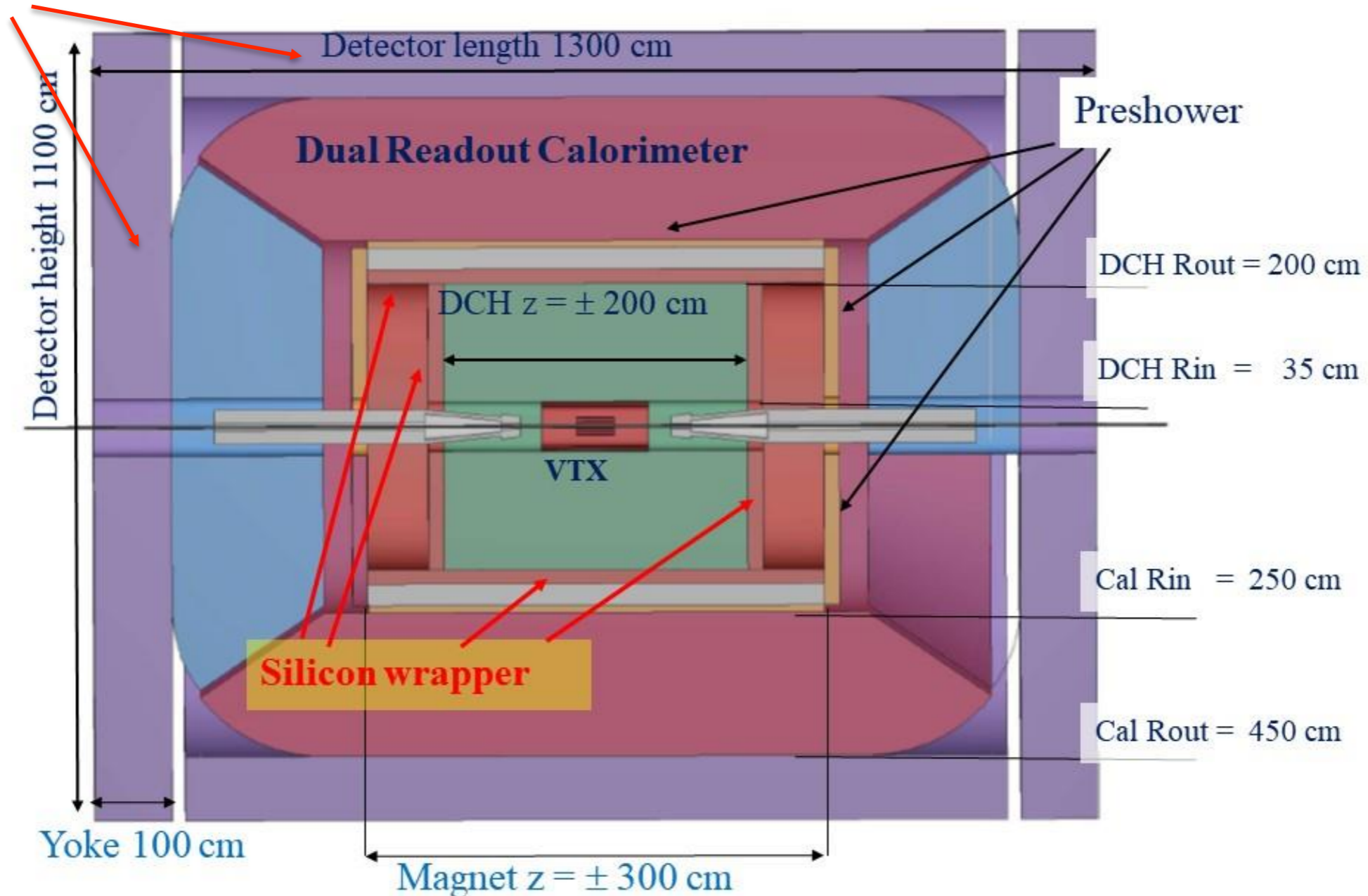
Amplification ions from the endplate @CEPC

	ALICE TPC	CEPC TPC
Maximum readout rate	>50kHz@pp	w.o BG?
Gating to reduce ions	No Gating	No Gating
Continuous readout	No trigger	Trigger?
IBF control	Build-in	Build-in
IBF*Gain	<10	<5
Calibration system	Laser	NEED

Comparison of ALICE TPC and CEPC TPC

The IDEA detector

Muon detector



In the IDEA concept, μ RWell detectors are foreseen for the preshower and the muon detector.

Similar in size, 50×50 cm², but with different strip pitch, 400 μ m in the preshower and 1500 μ m in the muon detector.