SOI detector testbeam analysis

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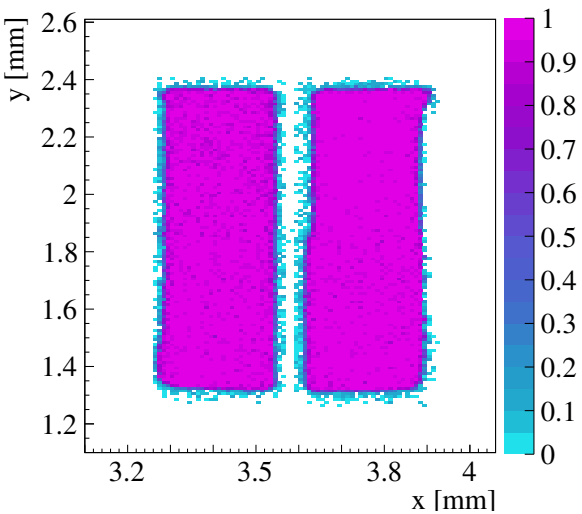
How efficiency has been calculated?

$$\text{efficiency} = \frac{\text{number of DUT correlated hits}}{\text{all tracks}} \quad (1)$$

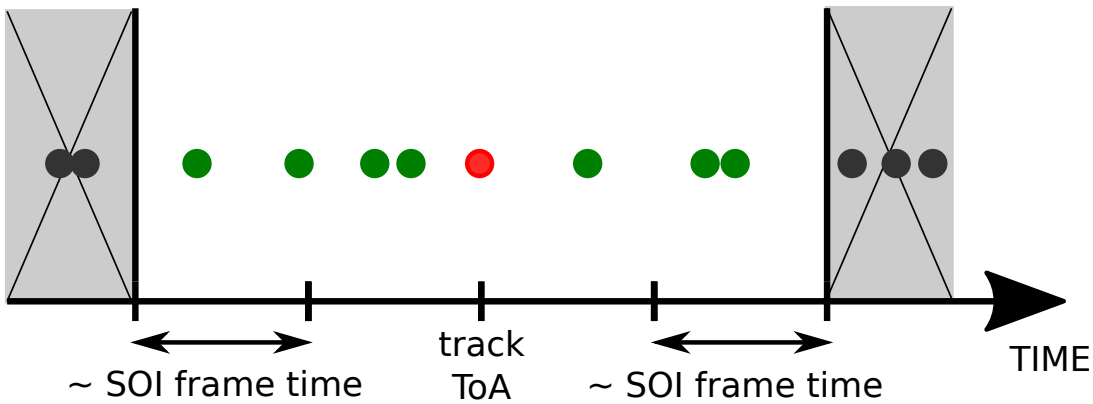
- efficiency is calculated using Four-Pixel Method clusterization in order not to generate large clusters
- clusters on borders taken into account - in principle only the information about hit presence is important, not the true charge amount
- cluster position cannot be more than two pixel pitches away (60 um) from corresponding track *or* its seed position cannot be more than 60 um from track positions (delta electrons problem partially solved)
- reset clusters are not rejected from the analysis



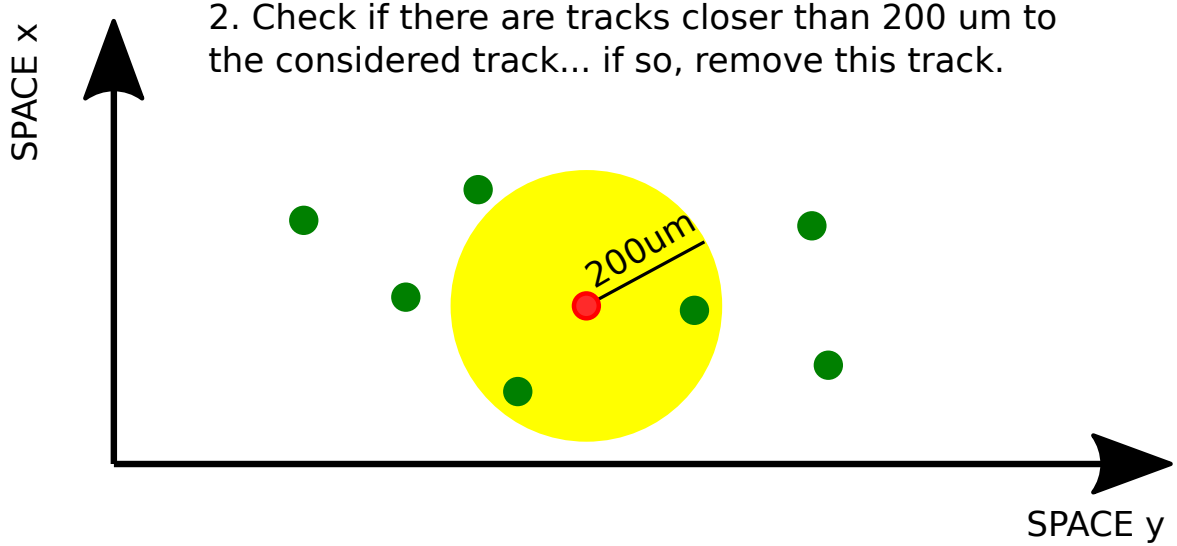
- Calculated in the "inner" region of efficiency map, shown above, to be free from border effects.
- Final efficiency is taken as a mean value from the inner region of efficiency map.
- Pile-up might occur. We have assessed it to be around 1-3%, depending on readout clock frequency.

Track selection procedure - pile-up rejection

1. Find all tracks that are in the range of about
~2 SOI frame times from consiedred track ToA

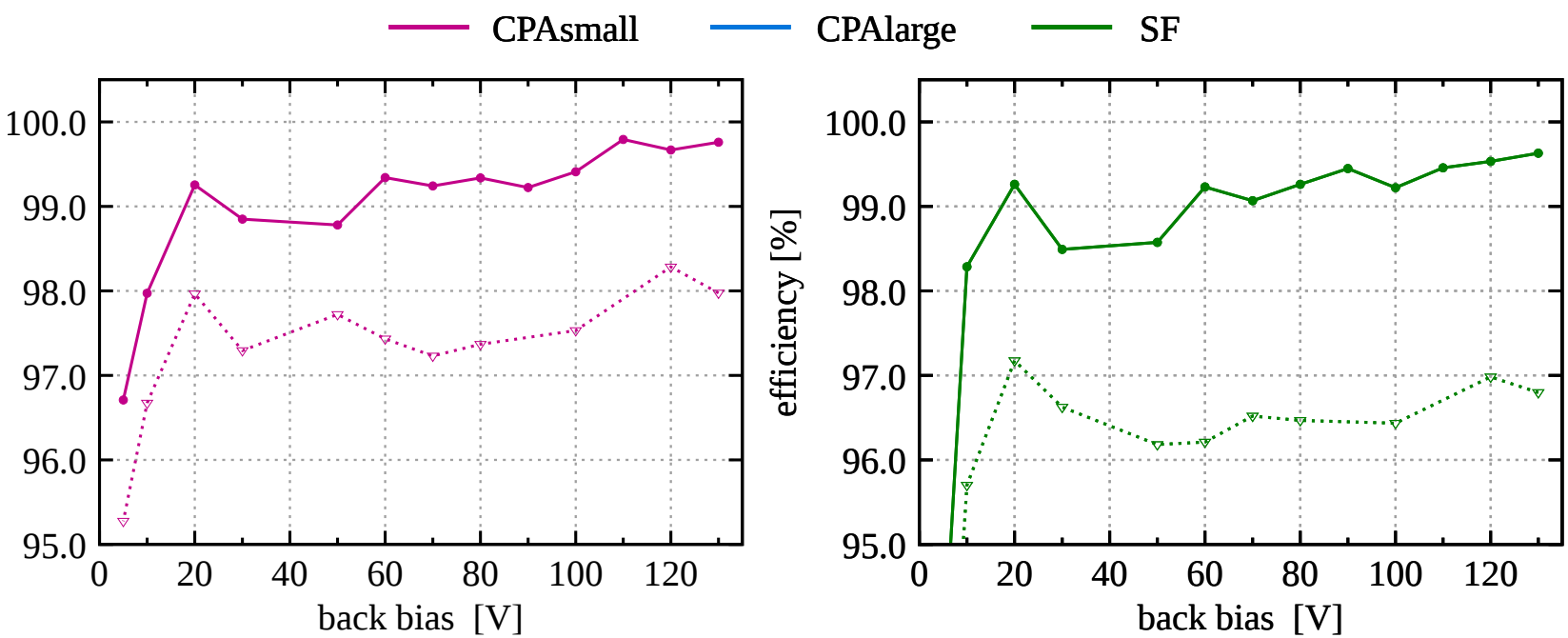


2. Check if there are tracks closer than 200 um to
the considered track... if so, remove this track.



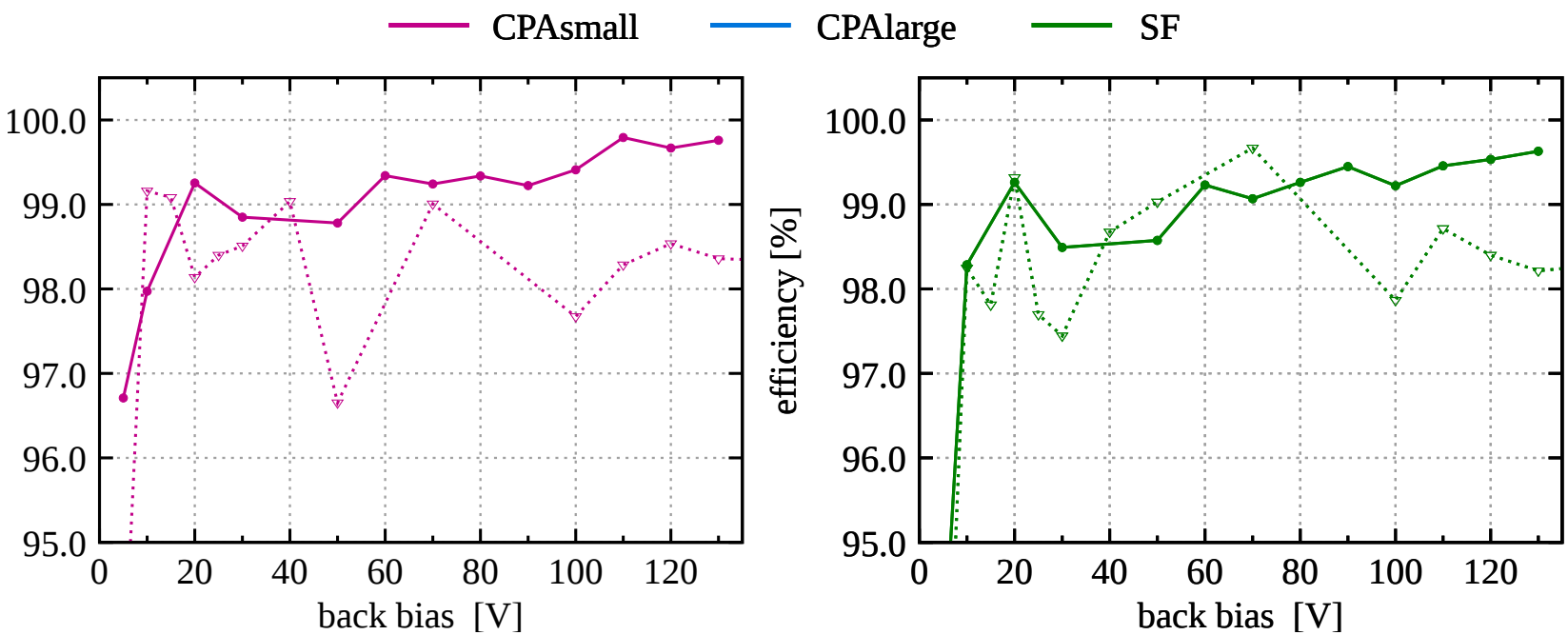
"Old" and "new" approach comparison

- FZN-1, 5MHz
- **dashed** = with pile-up "old"
- **solid** = without pile-up "new"



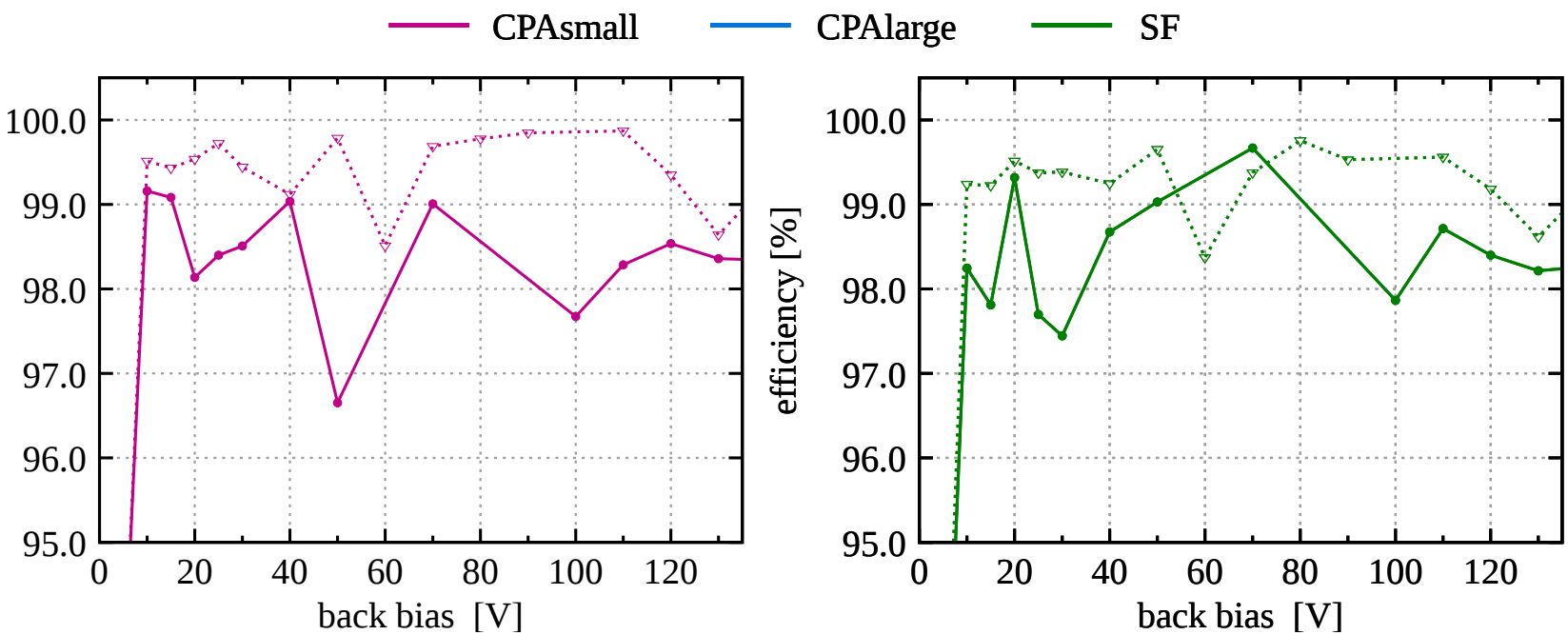
"new" approach - different wafers, the same readout clock

- 5MHz
- **dashed** = FZN-3,
- **soild** = FZN-1,



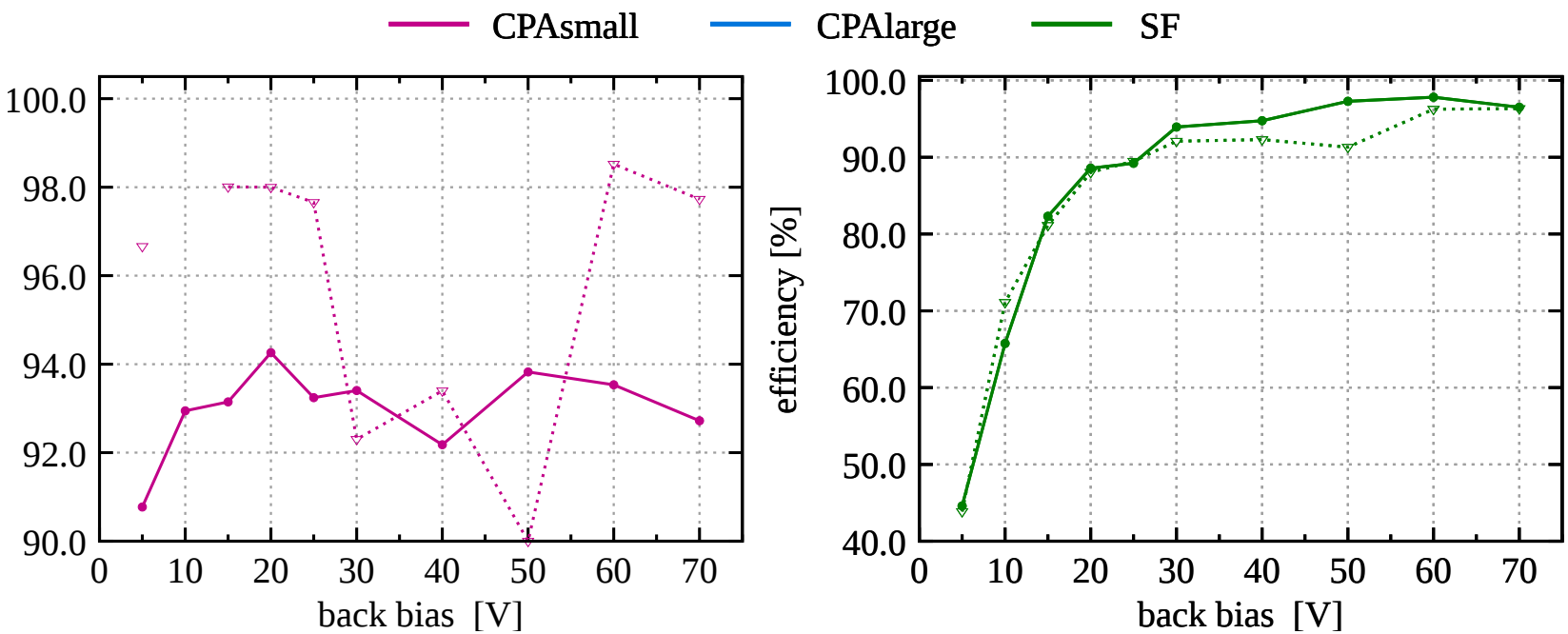
"new" approach - the same wafer, different readout clocks

- FZN-3
- **dashed** = 12.5 MHz,
- **soild** = 5 MHz,



DSOI - old and new comparision

- DSOI1
- 12.5 MHz
- **dashed** = old (pile-up might occur)
- **solid** = new (should be no pile-up)



Not understood, why CPAsmall shows worse performance after pile-up rejection on the DSOI... 5 MHz on the same wafer gave the same results as 12.5 MHz. Need to check other wafer.