Development of the Mu3e Pixel Sensor

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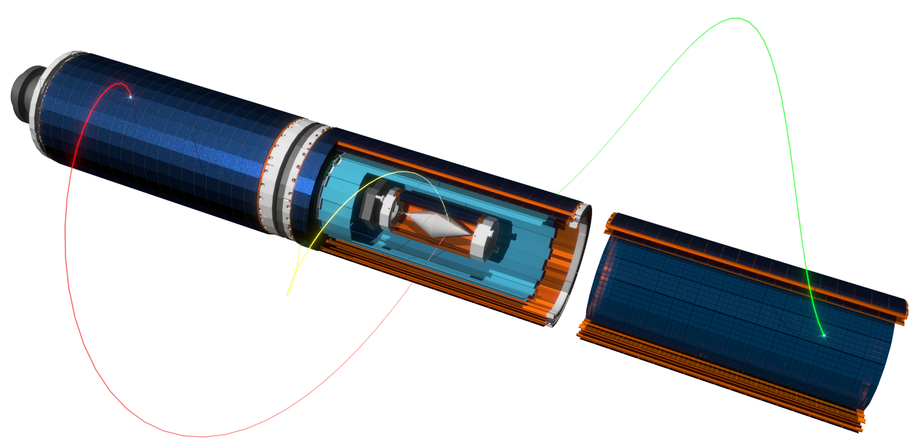
Mu3e

Search for the LFV decay $\mu \to eee$
in an environment of 10^8 - 10^9 μ-decays s^{-1}
($BR_{SM} < 10^{-54}$)



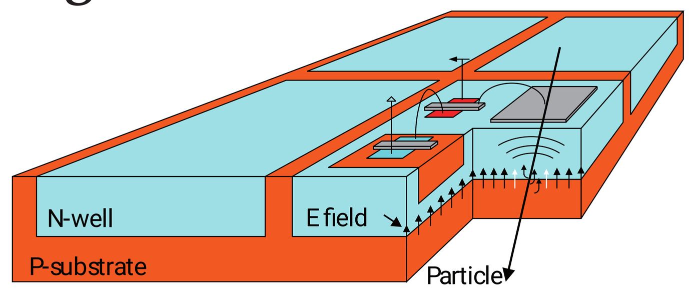
Pixel Sensor Requirements

- Pixel size $< 100 \times 100\,\mu m^2$
- Time **resolution** $\sigma < 20\,ns$
- Material budget $< 0.1\%\ X_0$/layer
- **High rate** capability: $4\,MHits/s$
- $2 \times 2\,cm^2$ active pixel matrix
- Efficiency $> 99\%$ @ low noise
- Power $< 250\,mW\,cm^{-2}$

No standard pixel detector technology can fulfill all of these requirements simultaneously
→ **a new technology is needed!**

HV-MAPS

High Voltage Monolithic Active Pixel Sensor

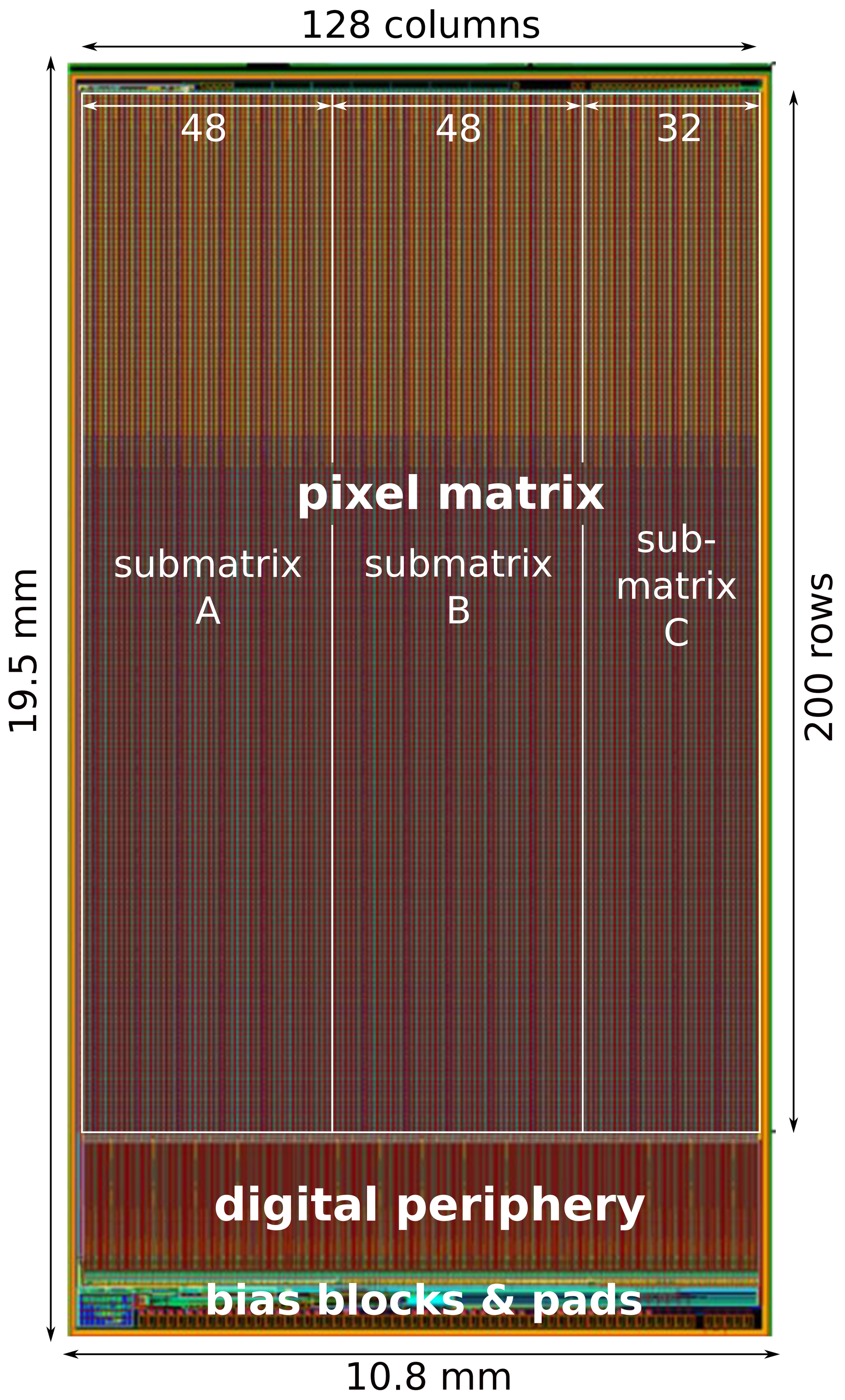


- N-well diode: charge collection via drift
- In-pixel electronics: high integration level
- Detection and readout in one chip

→ Monolithic

- Commercial HV-CMOS process

The MuPix8



- The first large scale prototype
- 180 nm HV-CMOS process
- Pixel size: $81 \times 80\,\mu m^2$
- Thinned down: $50\,\mu m$ to $100\,\mu m$
- Different substrate resistivities: $20\,\Omega\,cm$ to $1000\,\Omega\,cm$
- Timewalk correction possible:
  - Two-Threshold sampling
  - 6 bit Hit-ToT information
- Streaming readout @ $1.25\,Gbit\,s^{-1}$
- Hit rate of more than $10\,MHits/s$ possible

MuPix10

- Submission currently in preparation
- $2 \times 2\,cm^2$ active matrix
- On-chip voltage regulators and slow control infrastructure will be added

→ Ready for module production

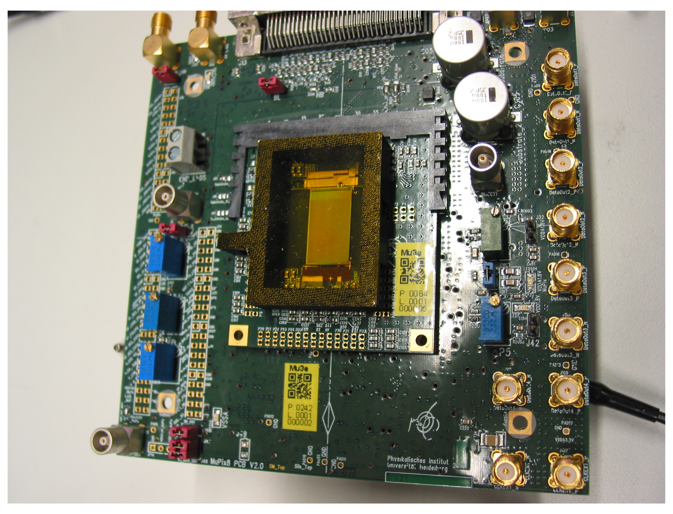
References

[1] I. Perić, *"A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology"*, Nucl.Instrum.Meth., **A582** 876, 2007.

[2] L. Huth, *A High Rate Testbeam Data Acquisition System and Characterization of High Voltage Monolithic Active Pixel Sensors*, PhD thesis, Heidelberg University, 2018.

[3] J. Hammerich, *Analog Characterization and Time Resolution of a large scale HV-MAPS Prototype*, Master thesis, Heidelberg University, 2018.

Setup



- Versatile setup and DAQ system
- Four Chip generations supported: MuPix7, MuPix8, MuPix9, ATLASPix1
- Single chip commissioning and characterisation
- Multiple stacked layers can be combined

→ Beam telescope

Efficiency and Resistivity

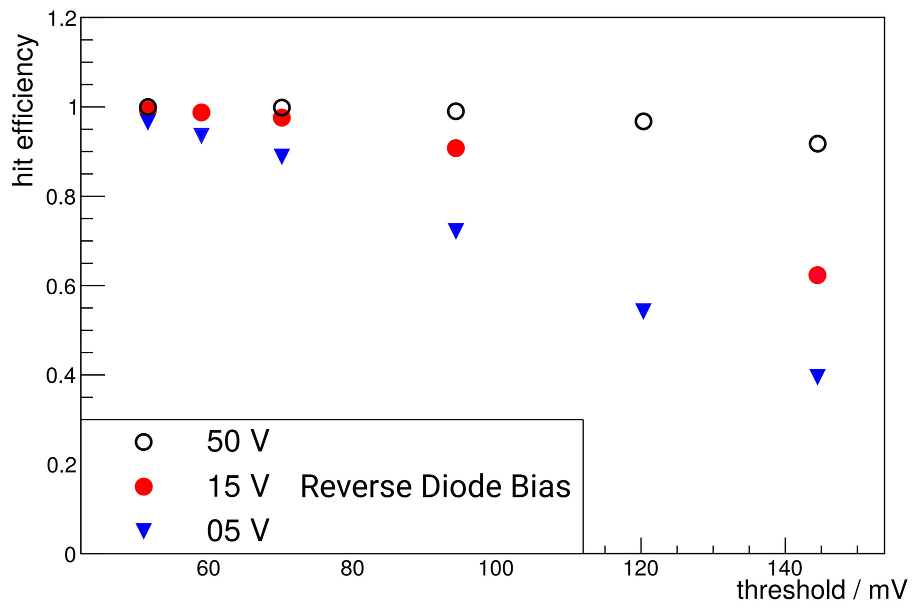


Figure 1: Efficiency of a $200\,\Omega\,cm$ chip for varying reverse bias [2].

Depletion thickness: $w \propto \sqrt{\rho \cdot U}$
ρ = resistivity, U = reverse bias voltage

The collectable charge scales linearly with the depletion thickness:
$w(200\,\Omega\,cm)@\,50\,V \simeq w(80\,\Omega\,cm)@\,100\,V$
$w(200\,\Omega\,cm)@\,\ \ 5\,V \simeq w(20\,\Omega\,cm)@\,\ \ 50\,V$

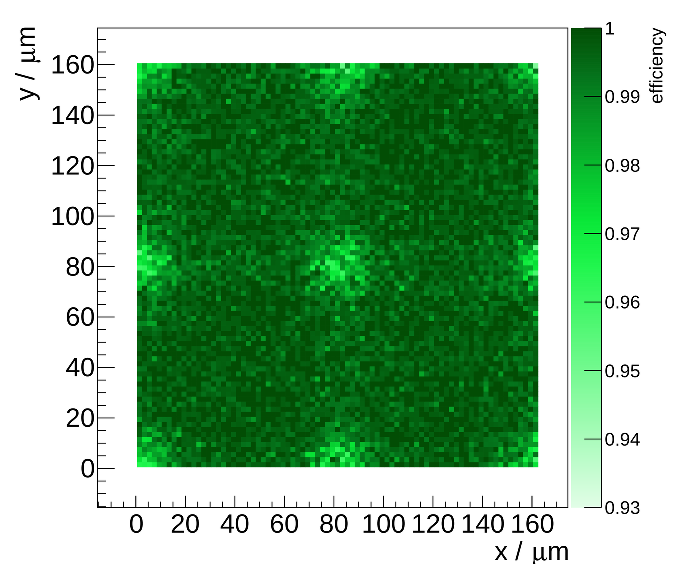


Figure 2: Sub-pixel study (2×2 pixel): $U = -15\,V$ and threshold $= 50\,mV (\approx 900\,e)$.

At these extreme settings, the pixel is not fully depleted.

Time Resolution

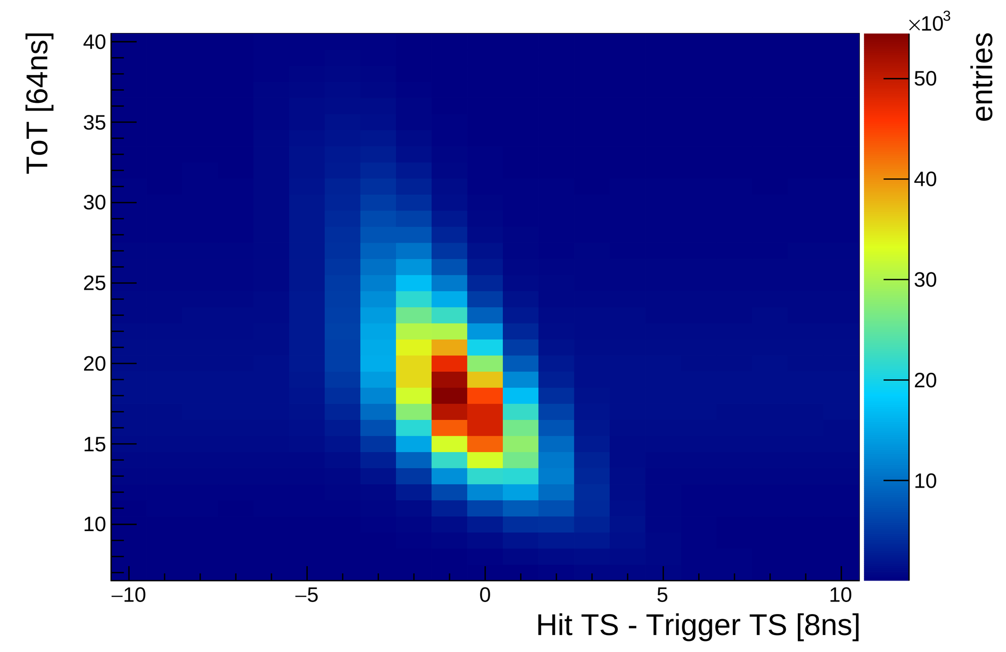


Figure 3: Timewalk: the hit delay depends on the amount of deposited energy.

Observed timewalk and on-chip delays are measured and are mathematically corrected afterwards.

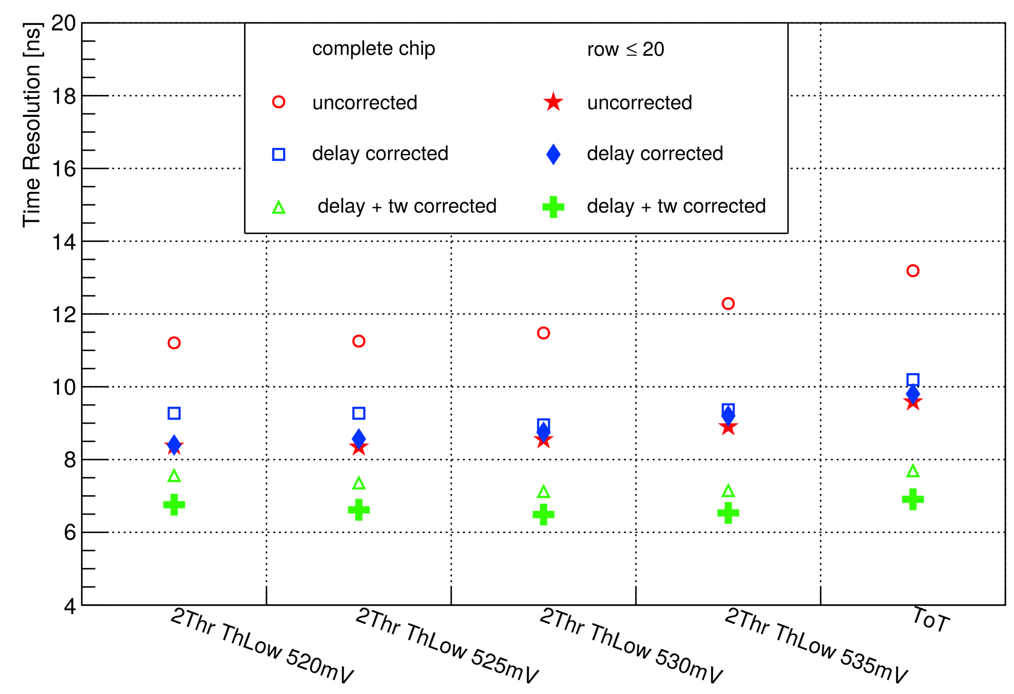


Figure 4: Time resolution corrected for signal line delay and timewalk [3].

By using the timewalk and delay correction the hit times can be corrected offline.
A time resolution $< 6.5\,ns$ is achieved.

Summary & Conclusion

- Scaling of the technology successful
- Very good time resolution $< 6.5\,ns$
- Large working range with high efficiency
- Change of the substrate resistivity from standard ($20\,\Omega\,cm$) to $80\,\Omega\,cm$ successful

→ Large working range with high efficiency