Silicon Pixel Detector R&D for CLIC

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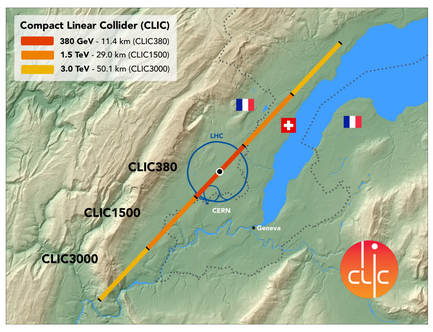
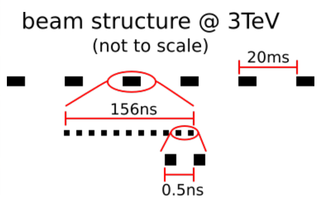
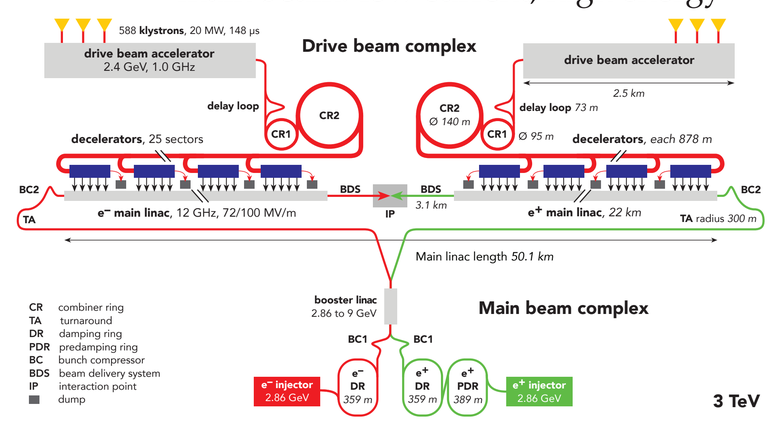
The Compact Linear Collider

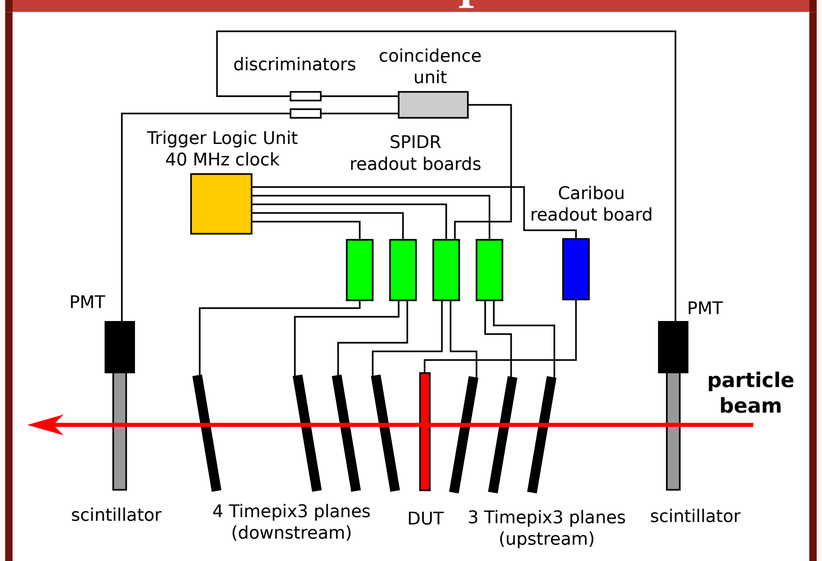




- Compact Linear Collider (CLIC): possible future e^+e^- collider after LHC
- accelerating structures + magnets at room temperature
- two-beam acceleration scheme:
  - drive beam: high current, low energy
  - main beam: low current, high energy



The Beam Telescope

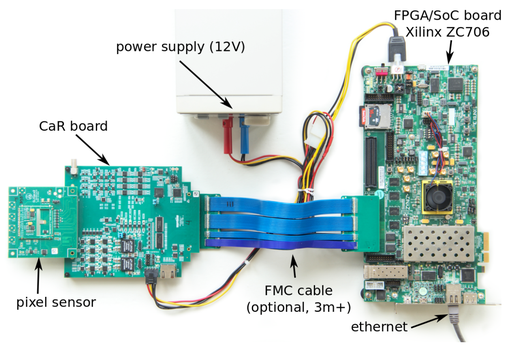


- located at CERN SPS (North Area)
- telescope performance:

track pointing resolution	$\sim 1.8\,\mu\text{m}$
track timing resolution	$\sim 1\,\text{ns}$

The Caribou Readout System

- versatile, open-source, linux-based
- fast and simple implementation of new detectors
- used for DUT readout in beam telescope



References

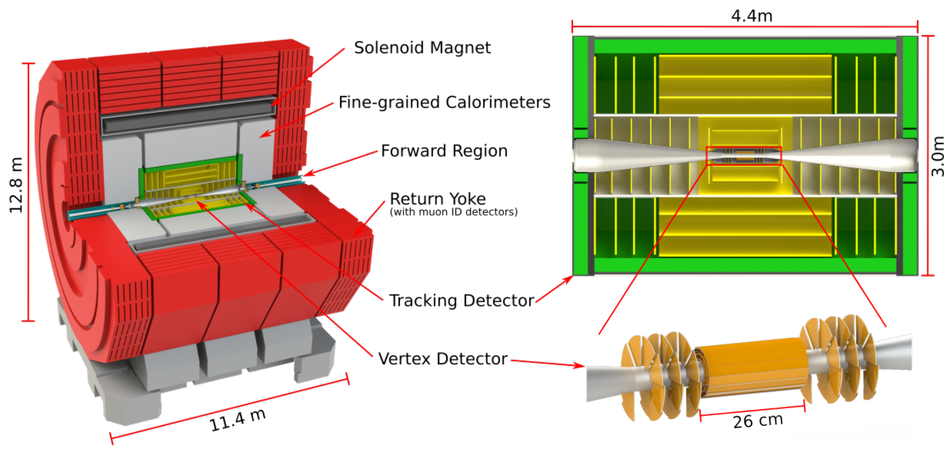
[1] CLIC collaboration. *The Compact Linear Collider (CLIC) 2018 Summary Report*, CERN-2018-005-M

[2] M. Benoit. *Pixel detector R&D for the Compact Linear Collider*, arXiv:1902.08752v4

[3] F. Pitters et al. *Time Resolution Studies with Timepix3 Assemblies with Thin Silicon Pixel Sensors*, arXiv:1901.07007v2

CLIC Detector Requirements

- due to bunch structure: low duty-cycle of $156\,\text{ns}/20\,\text{ms} \approx 0.000\,78\,\%$
- allows triggerless readout + power-cycling between bunches



Vertex Detector

silicon surface	$\sim 0.84\,\text{m}^2$
single-point resolution	$\sim 3\,\mu\text{m}$
timing resolution	$< 5\,\text{ns}$
material budget	$< 0.2\,\%\ X_0$/layer

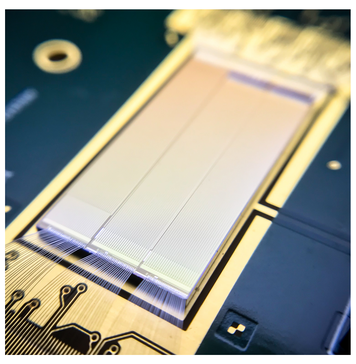
Tracking Detector

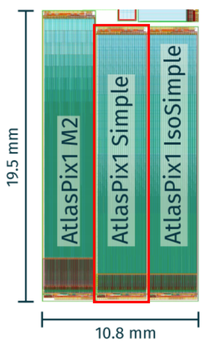
silicon surface	$137\,\text{m}^2$
spatial resolution (trans.)	$7\,\mu\text{m}$
timing resolution	$\sim 5\,\text{ns}$
material budget	$< 2\,\%\ X_0$/layer
hit detection efficiency	$> 99.7{-}99.9\,\%$

The ATLASpix Test Chip

- designed for ATLAS ITk Upgrade, tested in view of CLIC tracker requirements
- High-Voltage Monolithic Active Pixel Sensor (HV-MAPS):
  - fully integrated readout
  - fast charge collection
  - low material budget
- commercial $180\,\text{nm}$ HV-CMOS process: reduced cost/manufacturing complexity
- here only submatrix *ATLASpix_simple*:

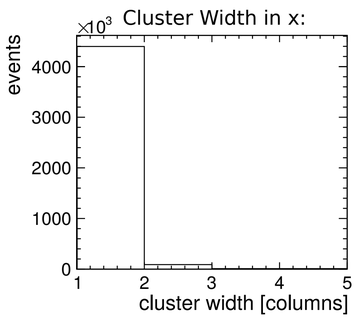
readout scheme	triggerless column drain
pixels	25 columns $\times$ 400 rows
pitch	$130\,\mu\text{m} \times 40\,\mu\text{m}$
time-of-arrival	10 bit
time-over-threshold	6 bit

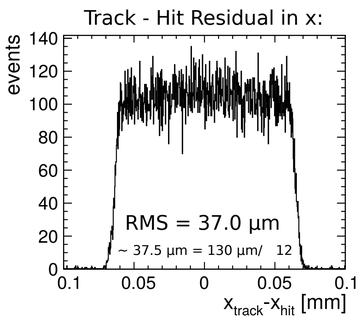


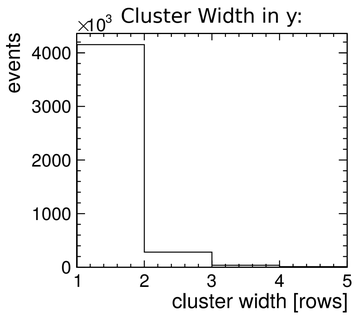


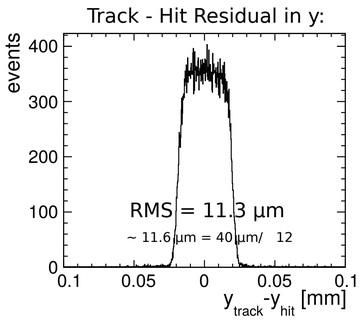
Spatial Resolution

- spatial resolution as expected without much charge sharing: $RMS \sim \text{pitch}/\sqrt{12}$
- slightly more charge sharing between rows (smaller pitch)

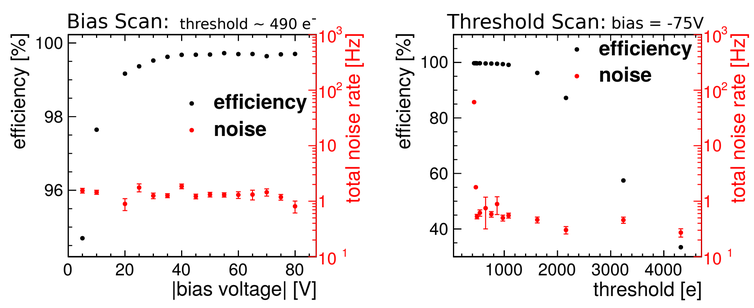








Efficiency Measurements

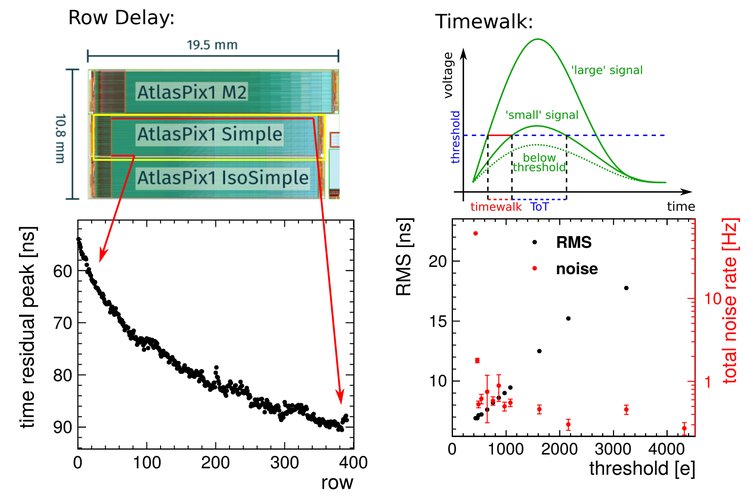


- fully efficient ($> 99.7\,\%$) at moderate bias
- can be operated at thresholds down to $\sim 500\ e^-$ while maintaining low noise

Timing Performance

- determined as RMS of time residual (track-hit on DUT), at 490 e^- threshold:

uncorrected	$8.7\,\text{ns}$
after row correction	$7.1\,\text{ns}$
after timewalk correction	$6.9\,\text{ns}$



Summary

- promising results: most requirements for CLIC Tracking Detector met
- HV-CMOS $\rightarrow$ suitable technology for Tracking Detector

Outlook

- more detailed performance studies for
  - different bulk resistivities
  - large track incident angles
- new test chip with adapted pixel geometry to meet spatial resolution