TCAD Simulation of High Voltage-Monolithic Active Pixel Sensors

Annie Meneses G., Physikalisches Institut, Heidelberg University

UNIVERSITÄT
HEIDELBERG
ZUKUNFT
SEIT 1386

HV-MAPS Technology

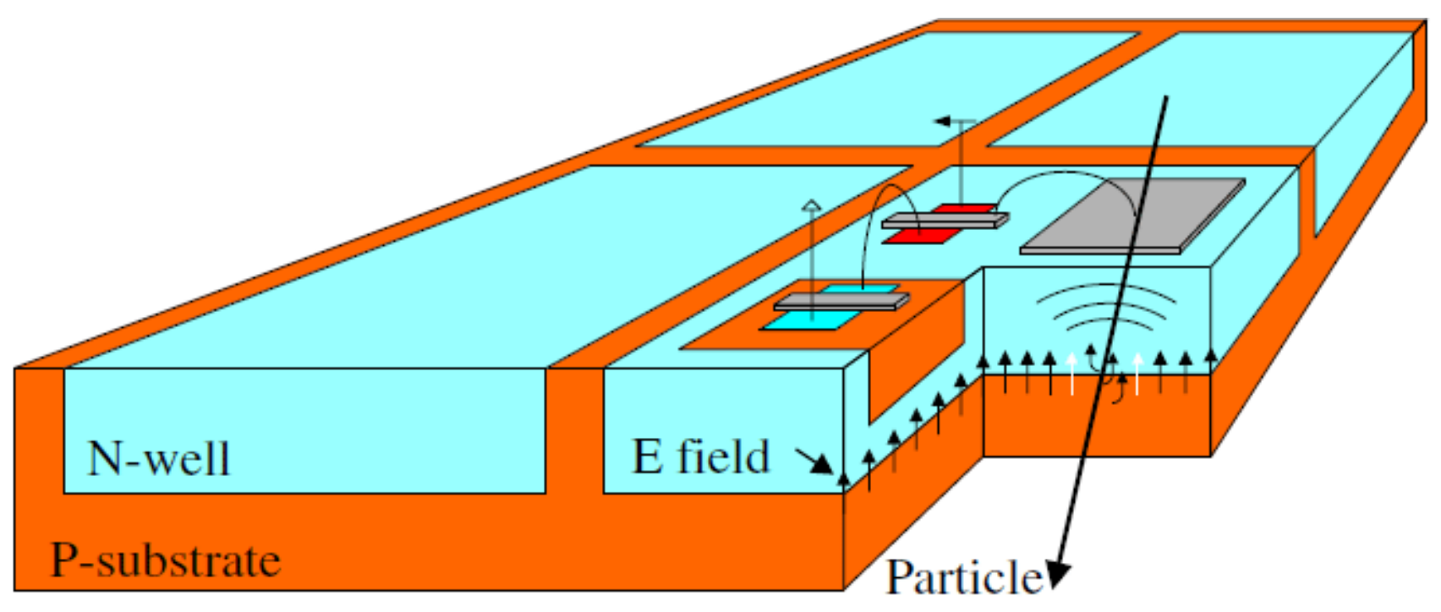

Figure 1: HV-MAPS Schematic (NIM A582 (2007) 876-885)

- Integrated readout electronics and sensor (low material budget)
- Use commercial CMOS process (cheaper than hybrid sensors)
- Fast charge collection via drift
- Technology for the Mu3e Pixel Tracker and a candidate for other future detector applications like LHCb, CLIC and PANDA (ATLAS)

Substrate Resistivity

- **Electric Field and Depletion zone**

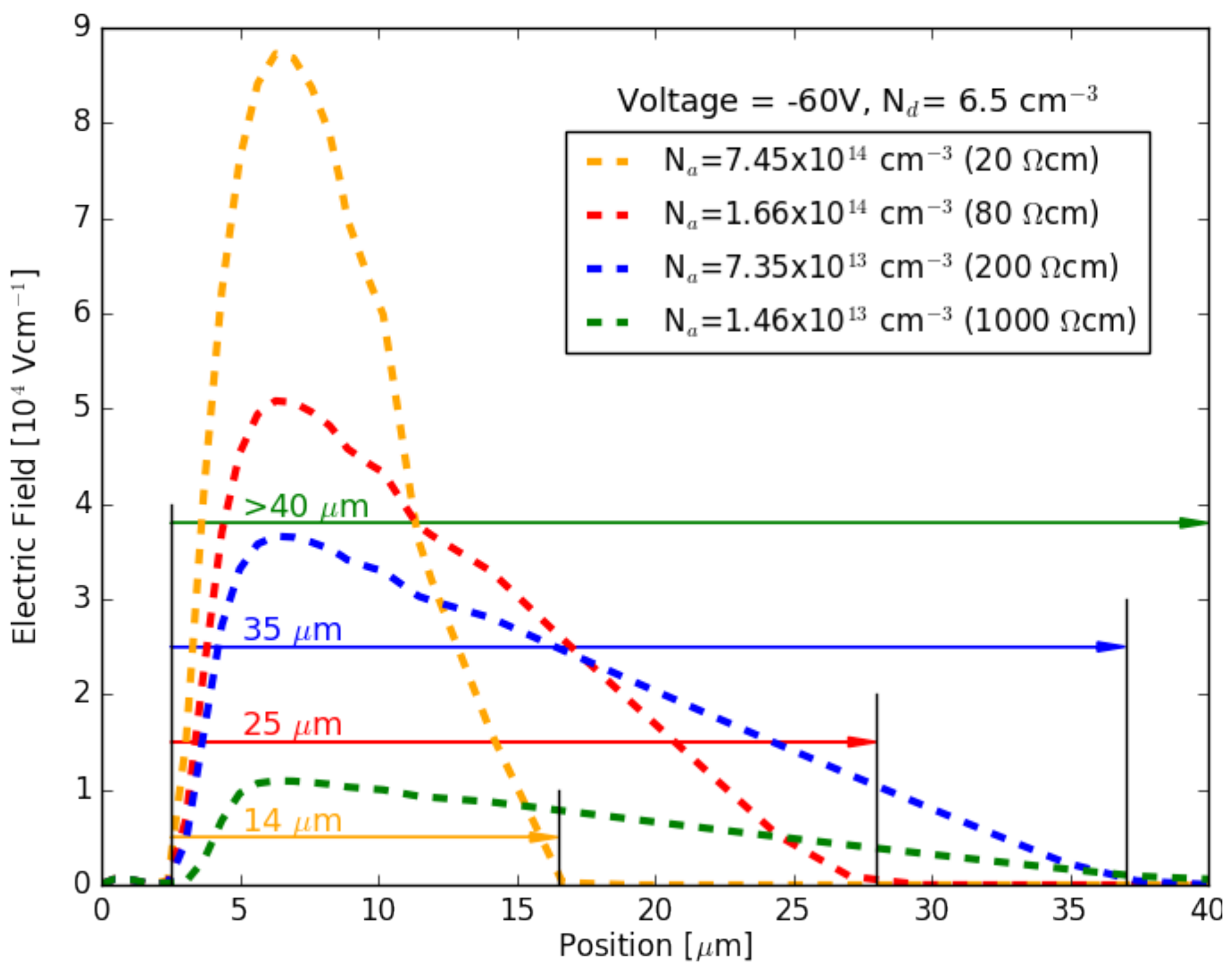

Figure 3: Electric Field in a reverse bias p-n junction

Pixel Dimensions

- **Diode Capacitance (C_0)**

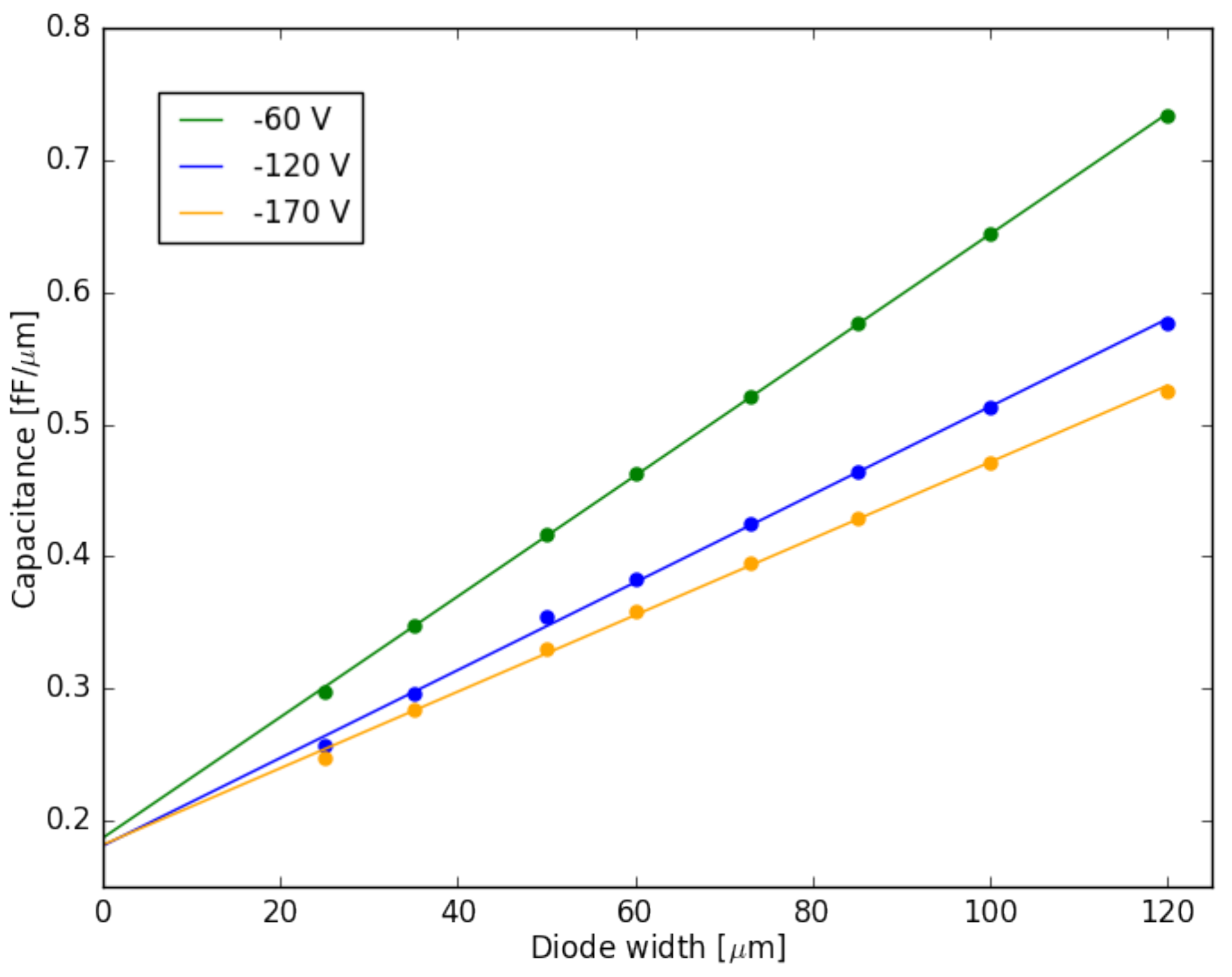

Figure 4: Normalized diode Capacitance in a 80 Ωcm

$$\frac{C_0}{\mu m} = (-1.538 * |V| + 539) * 10^{-5} * width + 0.18$$

Technology Computer-Aided Design

Use computer simulations to develop and optimize semiconductor technologies and devices

Why TCAD?

- Fabrication process and electrical behavior
- Tiny and complex structures in 2D and 3D
- Save time and money
- Complement to laboratory measurements
- Estimation and optimization of essential properties of the sensor performance (Breakdown Voltage, Charge collection time, Pixel Capacitance, ...)

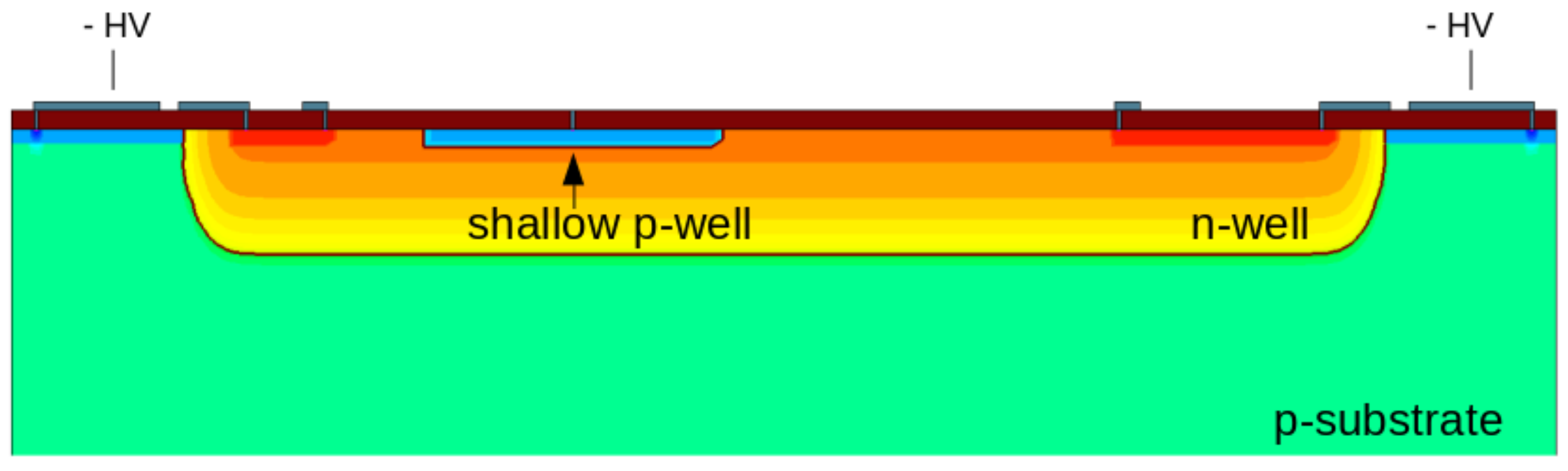

Figure 2: MuPix8 pixel cell design

Process Flow

1. Structure Simulation (Device structure and doping profiles)
2. Device Simulation (Physical models: mobility, recombination, avalanche)
   - Quasistationary (Breakdown Voltage, Capacitance, Electric Field ...)
   - Transient simulation of Minimum Ionizing Particle (MIP) (Charge collection process)

Pixel Isolation

Why? Electron accumulation layer due to a positive charge density in Si-SiO2 interface from 10^{11} to 10^{12} cm^{-2}

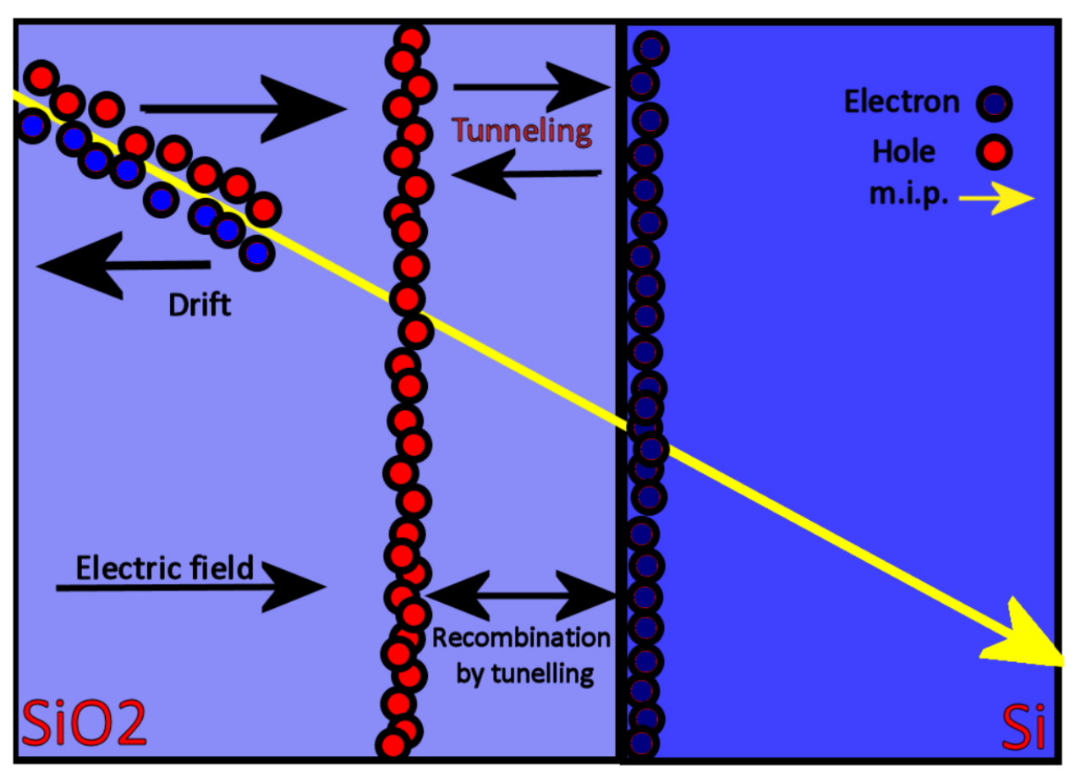

Figure 5: Radiation damage effect at Si-SiO2 interface

MuPix8 Interpixel Capacitance: ∼ 20 fF without isolation @ -60 V, 80 Ωcm

- **p-stop**
- **p-spray**

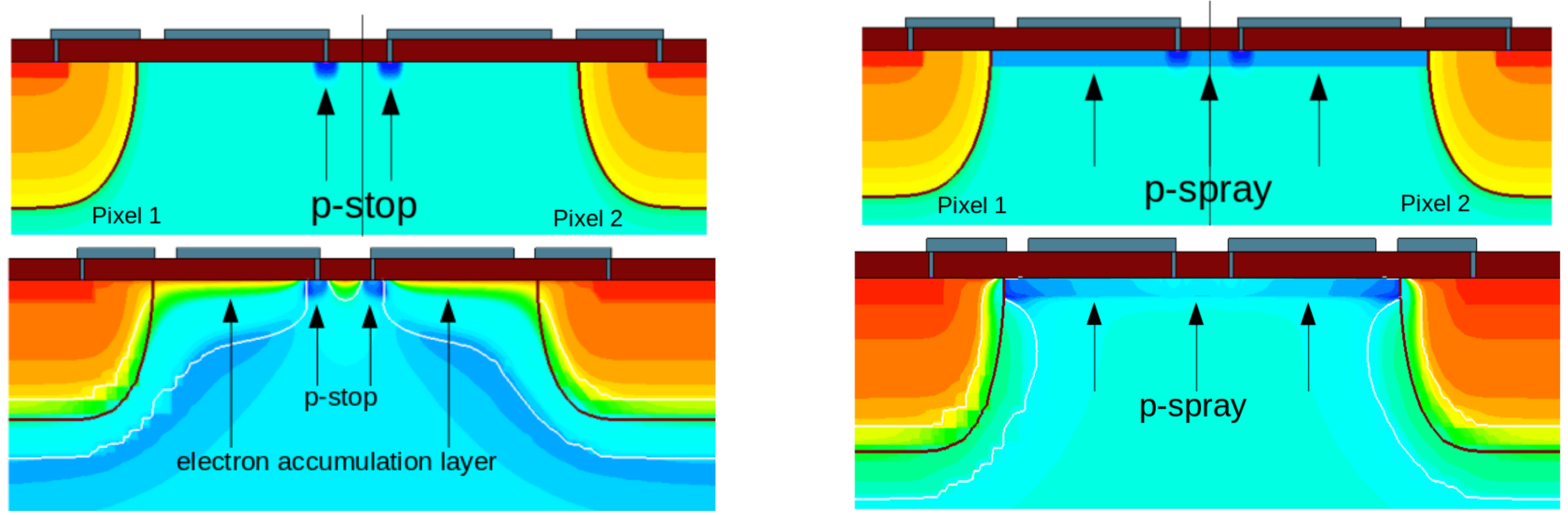

Figure 6: Isolation techniques for adjacent n-well implants (top) and electron concentration (bottom)

- **Breakdown**

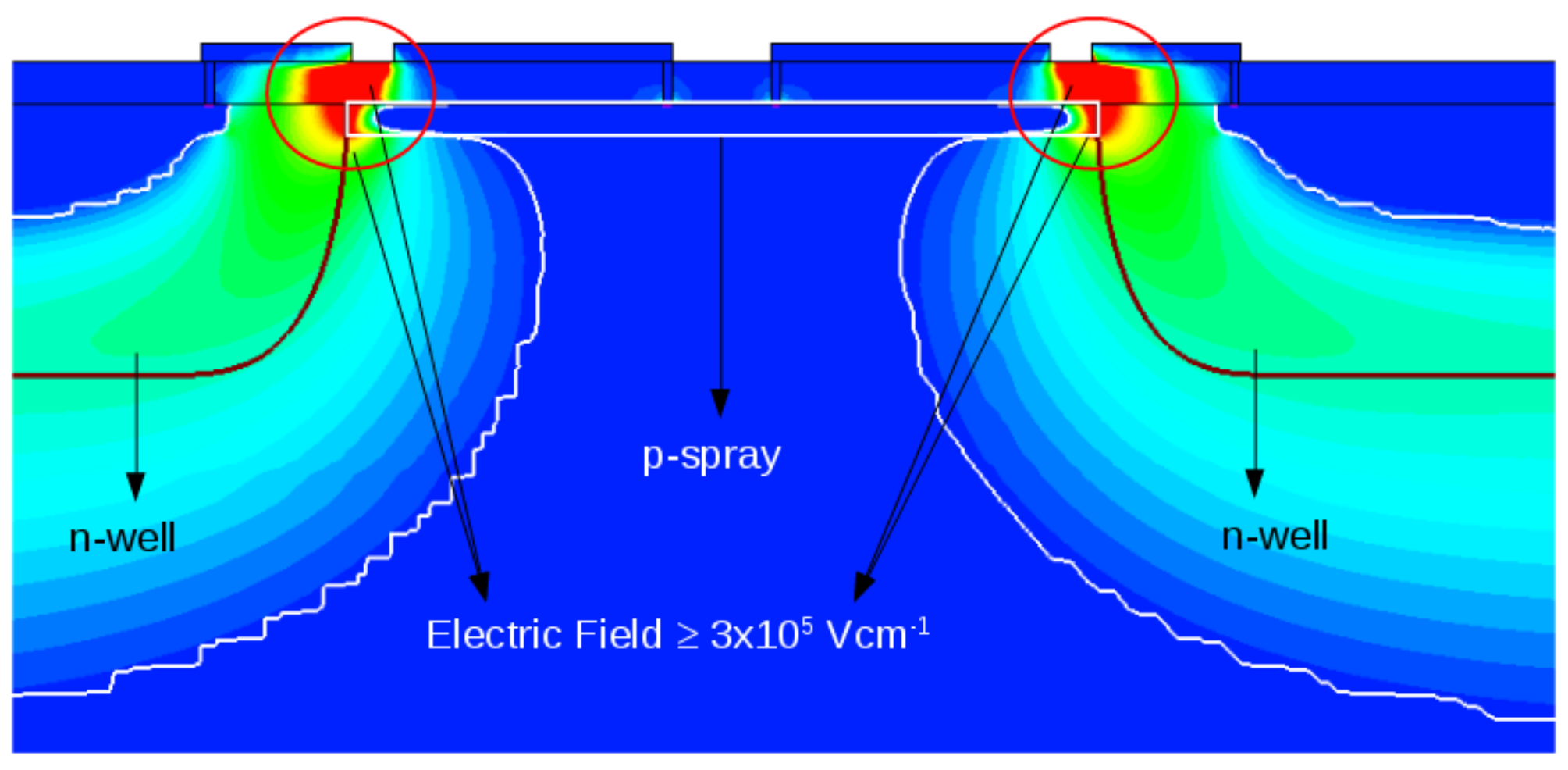

Figure 7: Maximum Electrical Field

Where?

1. p-spray - n-well junction
2. Between HV and diode first metal layer

- **Interpixel Capacitance (C_1)**

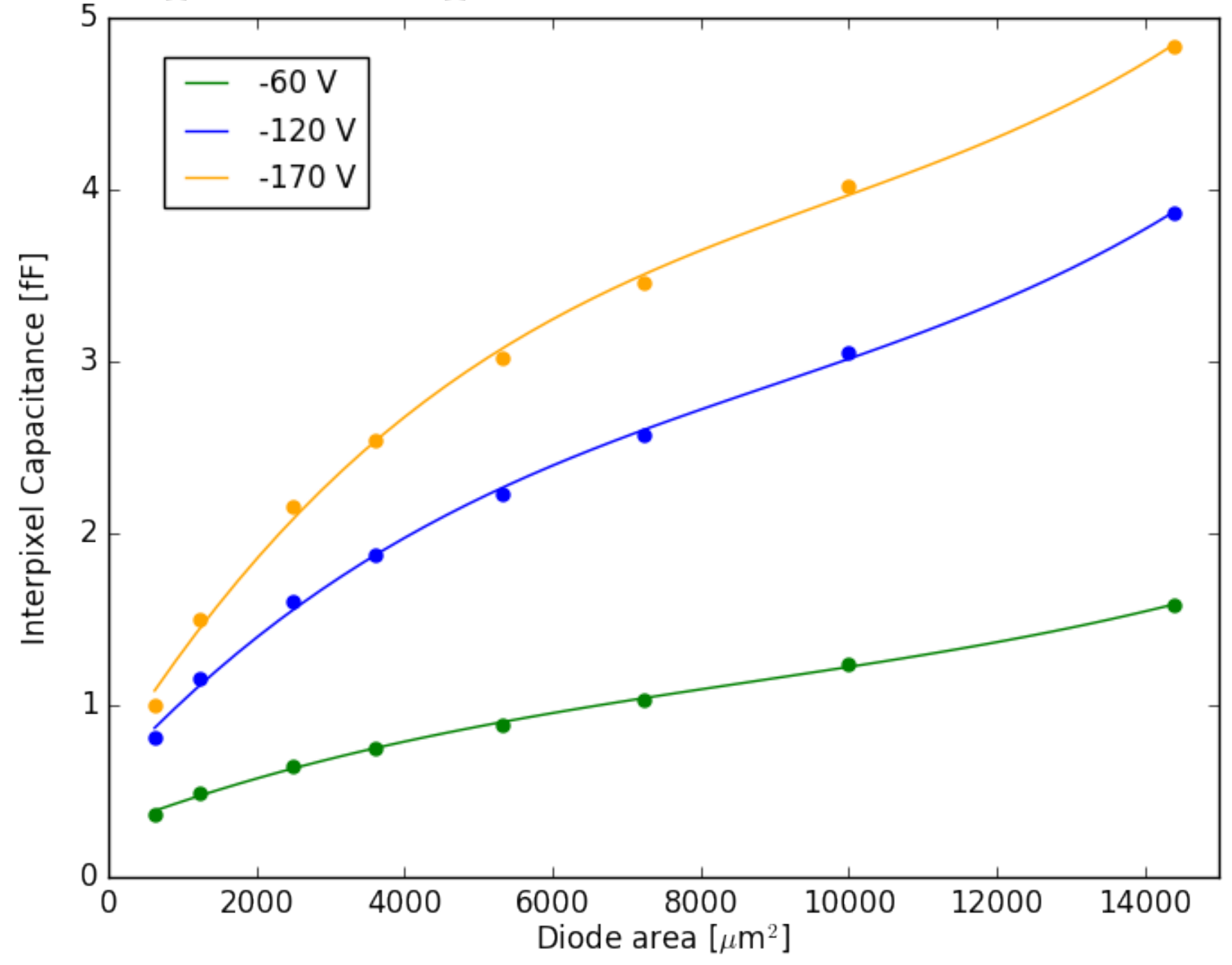

Figure 8: Interpixel Capacitance in a 80 Ωcm, for p-stop isolation and 18 µm distance between diodes

Shallow p-well

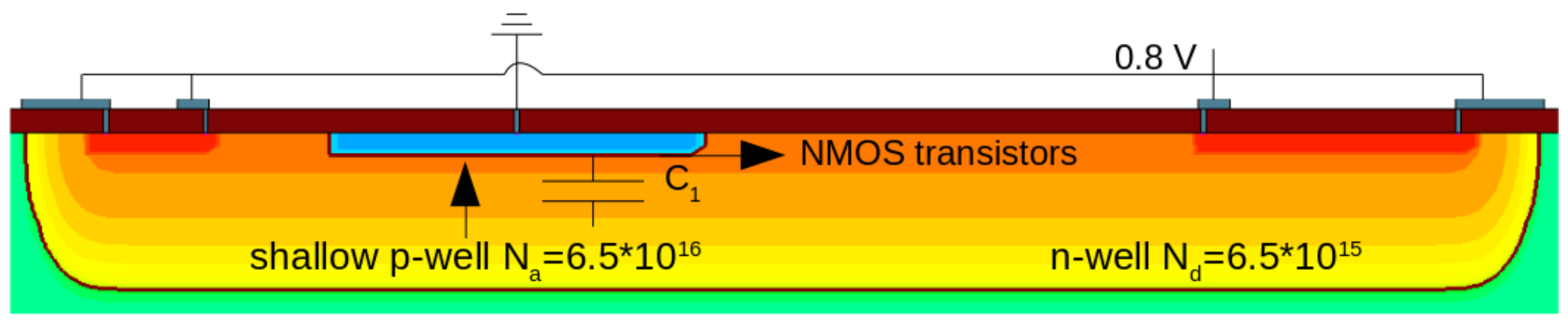

Figure 9: Shallow p-well embedded in the n-well

- **Capacitance (C_2)**

$$\frac{C_2}{\mu m} = 0.251 * width + 0.507$$

MuPix prototypes

MuPix7

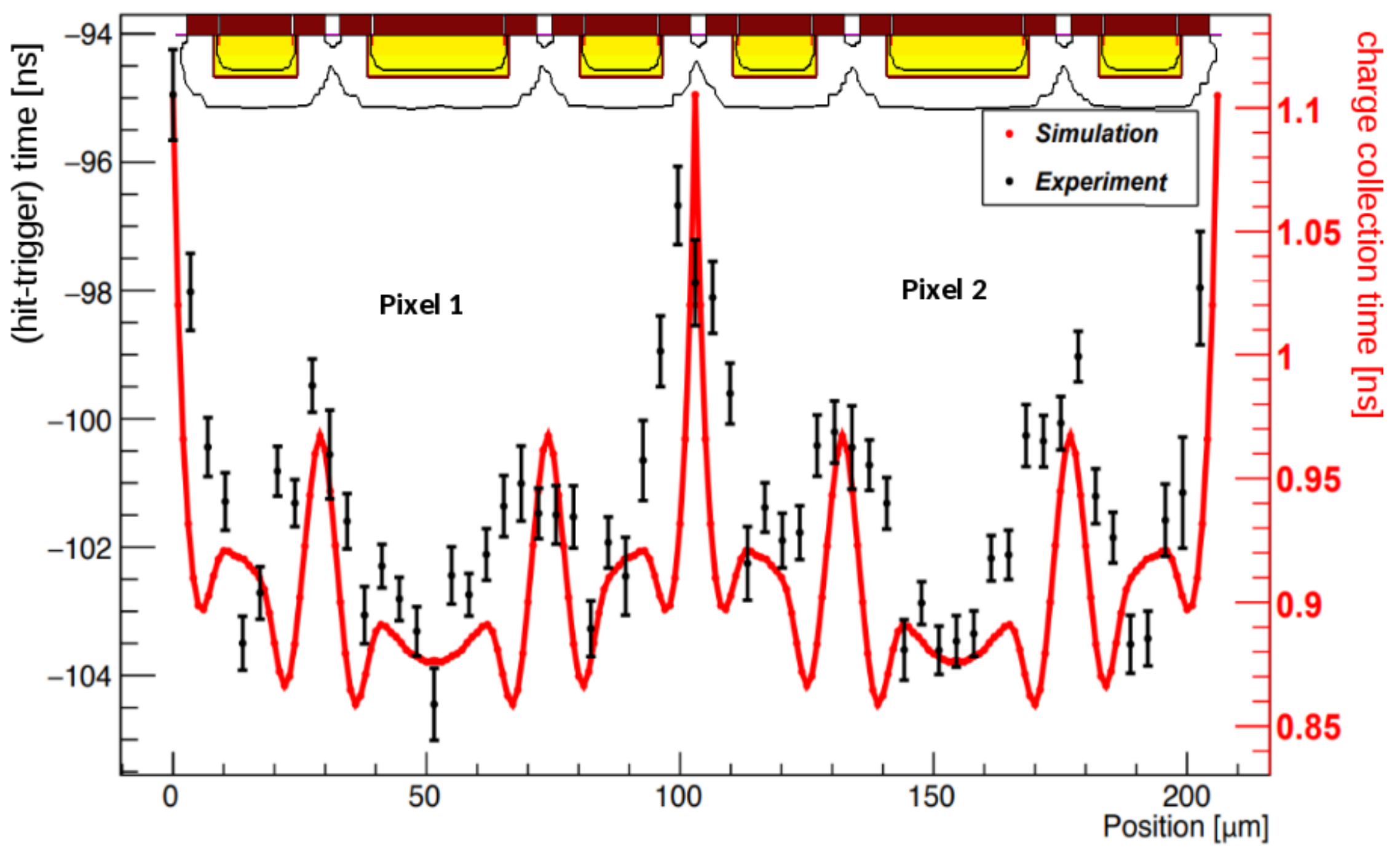

Figure 10: Comparison of the measured delays (left scale) and the simulated charge collection times (right scale) at -40 V (NIM A902 (2018) 158-163)

1. Experiment: 4 GeV DESY II testbeam facility
2. Simulation: LET → 2x10^{-5} pC/µm

MuPix8

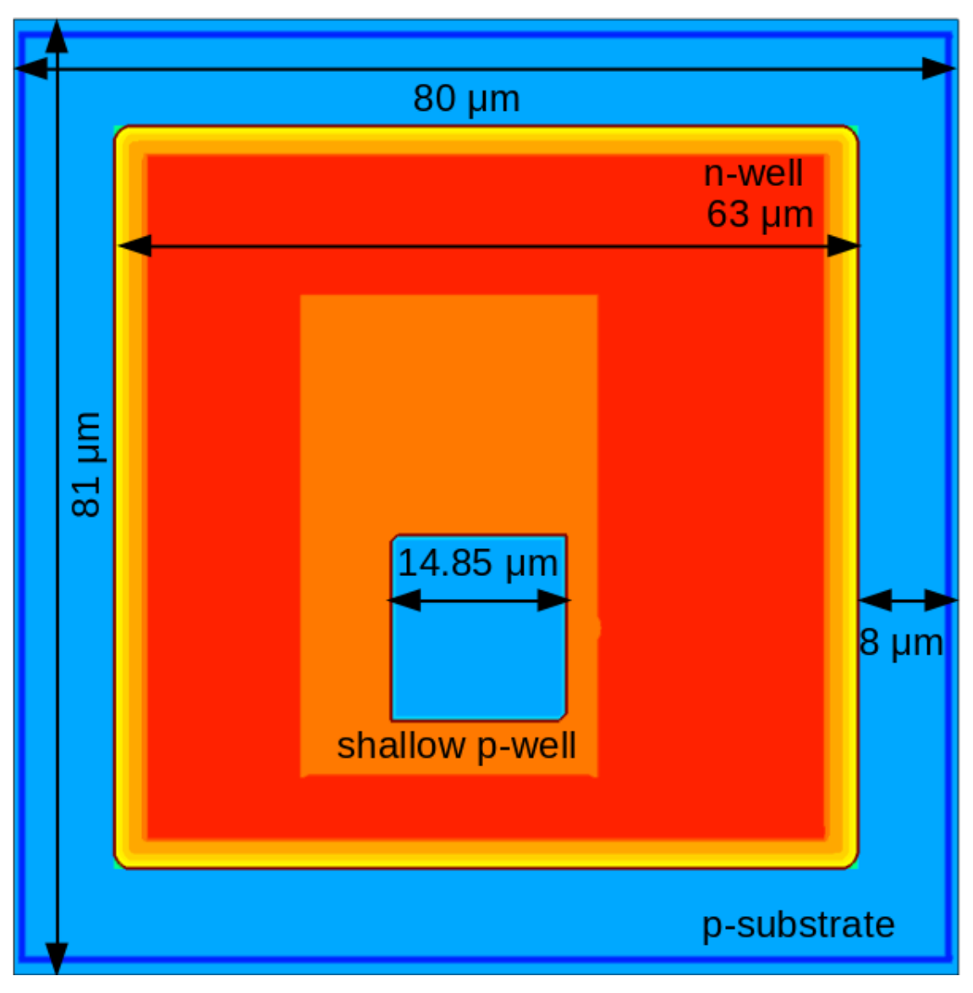

Figure 11: TCAD top view

- **Total Capacitance** at -60 V, 80 Ωcm

C_t = C_0+C_1+C_2

C_0 = 37.38 fF
C_1 = 0.61 fF
C_2 = 60.13 fF
C_t = 98.12 fF

- **Breakdown voltage**

Substrate resistivity	20 Ωcm	80 Ωcm	200 Ωcm	1000 Ωcm
Exp.	-48.0	-63.0	-60.2	-46.4
Sim.	-48.0	-59.8	-58.5	-51.4

AtlasPix3

*On production

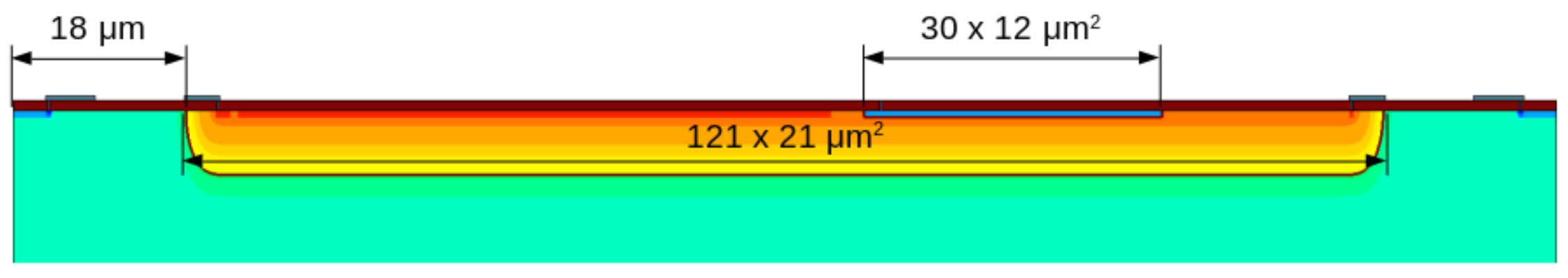

Figure 12: 2D TCAD Simulation of pixel design

- **Breakdown voltage**

Simulation: > -120 V

- **Total Capacitance** (at -60 V, 80 Ωcm)

C_t = 15.13 fF + 0.64 fF + 96.44 fF = 112.17 fF

Outlook

- Radiation damage studies in HV-MAPS with TCAD
- Use TCAD in combination with ALLPix^2 to predict HV-MAPS sensors behavior under test beam conditions