XIDer - An X-Ray Integrating Detector for the ESRF-EBS Upgrade

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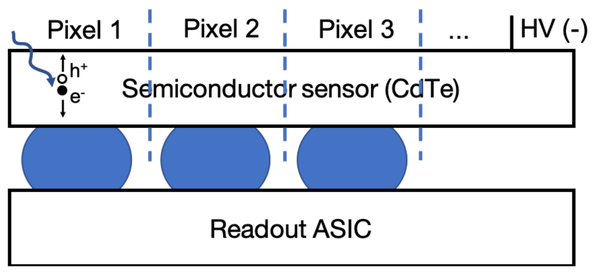
Introduction

XIDer is a collaboration between the European Synchrotron Radiation Facility (ESRF) and the Heidelberg University. It has been launched with the aims to:

- Build a 2D hybrid high-energy x-ray radiation pixel detector tailored to the requirements set by the ESRF's Extremely Brilliant Source (EBS) upgrade program



- Provide a multi-purpose platform for any kind of x-ray diffraction experiment performed by users of the ESRF

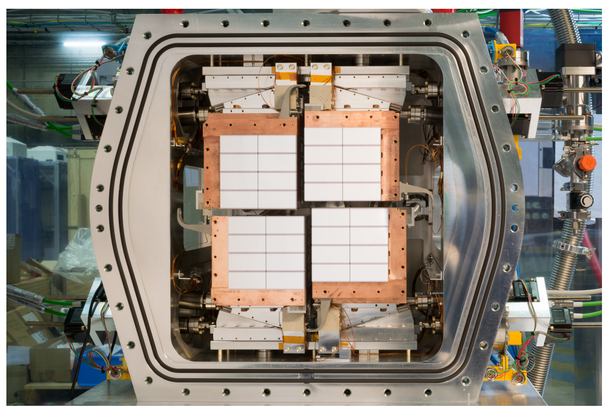
European Synchrotron Radiation Facility (ESRF)

- One of the world's largest third-generation high-energy electron synchrotrons
- Produces highly brilliant synchrotron radiation that allows performing X-ray spectroscopy, tomography and diffraction experiments
- Identifies itself as a user facility: ~9000 scientists visit the ESRF per year to work on their own projects

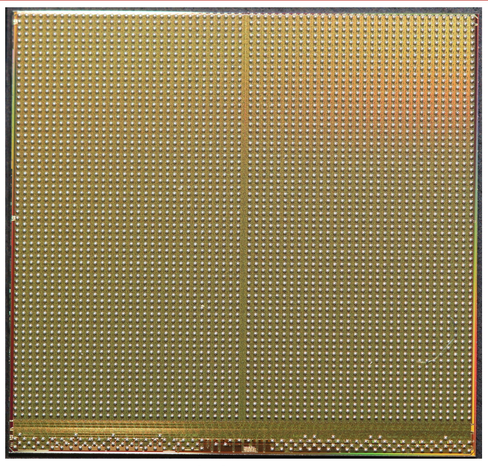
Installation of an EBS girder

- Started the EBS (Extremely Brilliant Source) upgrade program in 2015 to provide users with even more brilliant and coherent x-ray beams for more precise measurements
- Needs novel detectors to fully exploit the upgraded source
  $\Rightarrow$ **XIDer**

Experience with Similar Projects - DSSC @ XFEL



DSSC camera: 32 monolithic sensors, 256 ASICs



Readout ASIC with 4096 pixels

Intro

The DSSC (DePFET Sensor with Signal Compression) is a low noise x-ray pixel detector used at the European XFEL. Our research group played a crucial role in the readout ASIC implementation, characterisation and DAQ. XIDer directly benefits from knowledge and experience gained in this project.

Specs

- 0.5-6 keV
- Single photon sensitivity
- Dynamic range of $>10^4$ ph
- Burst data rates of 150 Gbit/chip/s

What is special about XIDer?

Due to the detector's multi-purpose nature, there is a broad range of requirements. The most **challenging** and **unique** are:

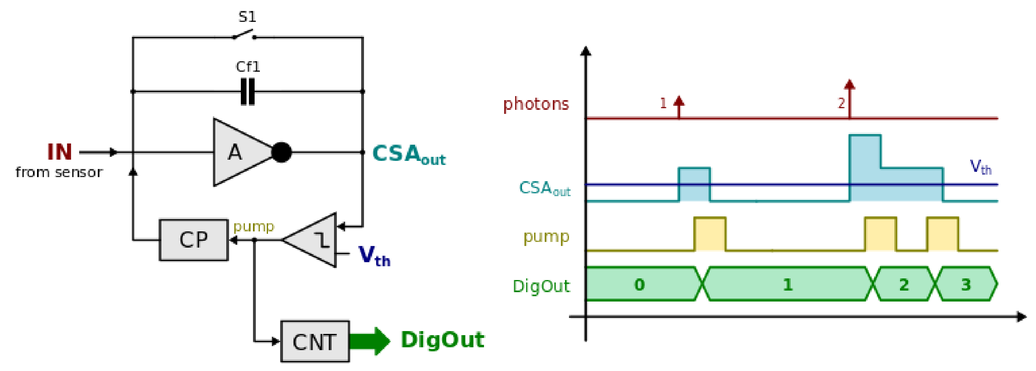
- **High dynamic range**: Single photon sensitivity & **high rates** of more than 10^9 ph/pxl/s
- **Handling of vastly different storage ring bunch modes**: Single pulses vs. **quasi-continuous detector illumination**
- **Energy range of 30-100 keV**: High photon energy demands the use of high-Z materials like cadmium telluride which complicate the design process

My Contribution to XIDer

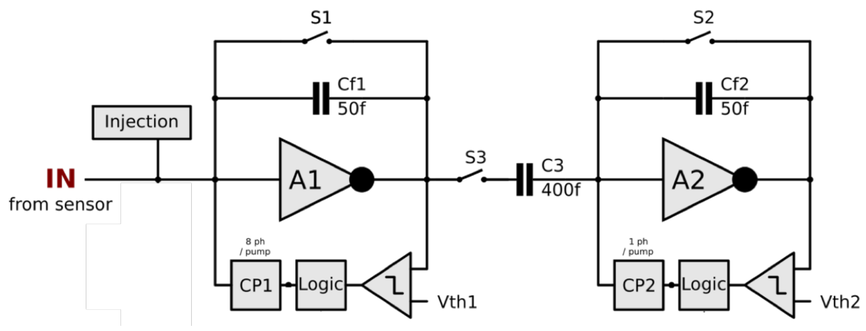
In the scope of an R&D phase, my work revolves around designing the readout ASIC including tasks like:

- Verify project feasibility on readout ASIC side
- Design and characterise small scale prototypes
- Prepare large scale integration of full system

Readout ASIC - Charge Integrating Frontend

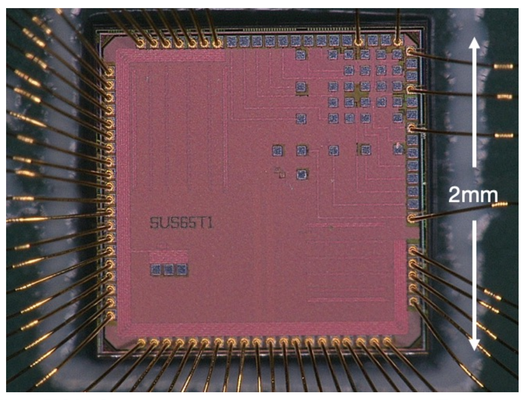


- Incoming charge is integrated by a charge sensitive amplifier (CSA)
- If $\mathrm{CSA}_{out} > \mathrm{V}_{th}$, the comparator activates the charge pump (CP)
- The charge pump subtracts well-defined charge packets from the input node IN until CSA_{out} is back below the threshold V_{th}
- A counter (CNT) tracks the amount of charge packets
- Real design uses more complicated two-stage approach



The Status Quo

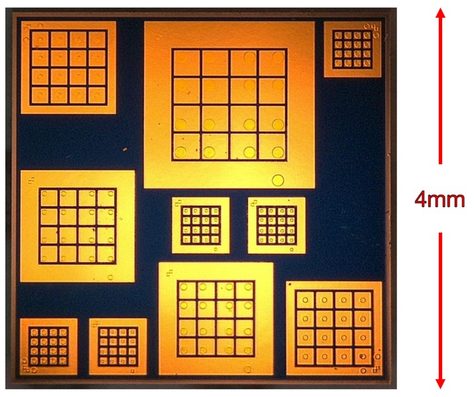
Readout ASIC



First TSMC65 prototype manufactured in Feb 2019

- Includes: charge integrating frontend, JTAG interface, digital control block, serial output data link & infrastructure for sensor characterisation
- Characterisation ongoing to verify the simulated rate of 6×10^8 ph/pxl/s

Sensor



First CdTe prototype manufactured in Mar 2019

- Several pixelated areas, varying pixel pitches from 100 µm to 300 µm
- Characterisation as well as investigation of possible bonding procedures ongoing