3D Integrated Single Photon Avalanche Diode

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New Trend: 3D Single Photon Avalanche Diode

Advantages of 3D approach :

- photon detection efficiency enhanced by maximized Fill Factor
- noisy pixel control by using vertical control circuitry
- heterogeneous fabrication technology for SPAD and CMOS circuits
- capability of using different materials for SPAD and processing unit
- Possible applications : Darwin Project, Biomedical Imaging, LIDAR etc.

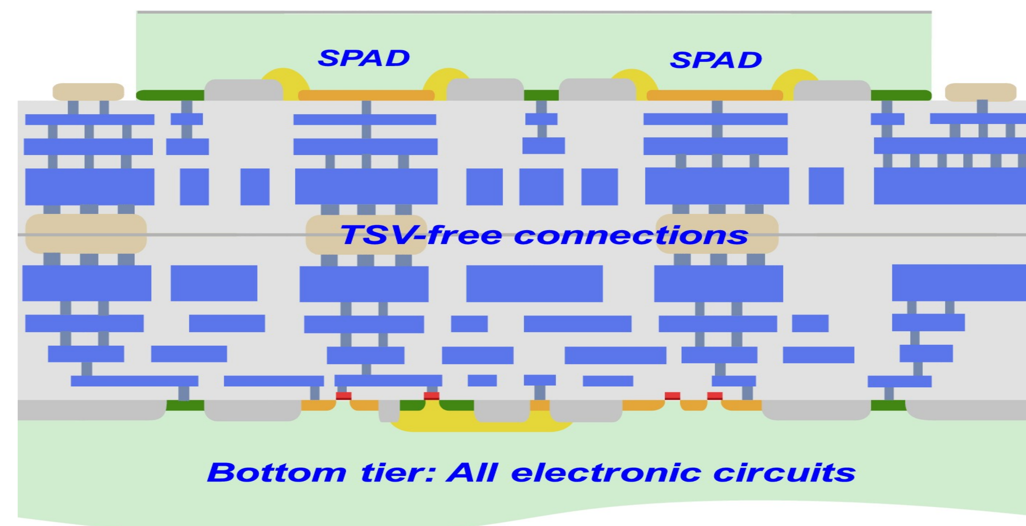


Figure 1: Cross-sectional view of 3D Integrated Back-side Illuminated CMOS SPAD

Cons of 2D implementation :

- loss of photon sensitivity due to low Fill Factor
- same process for SPAD & CMOS

Reasons for 3D Integrated BSI structures

2 other 3D structures show some drawbacks

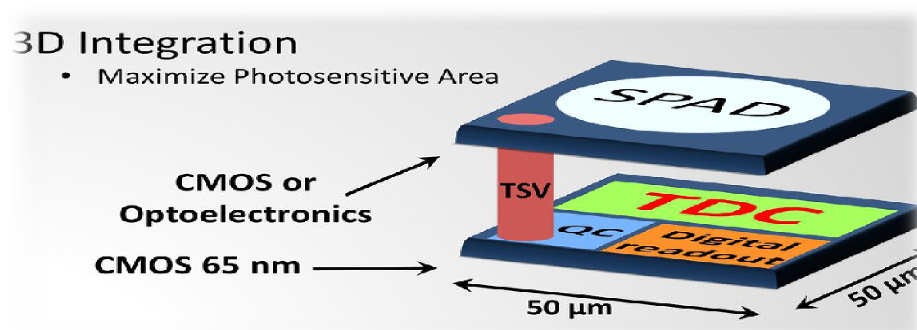


Figure 2: Through Silicon Via Front-side Illumination (FSI)

- certain diameter and clearance (5 µm diameter dead area)
- extreme low yield for TSV formation (60 %)

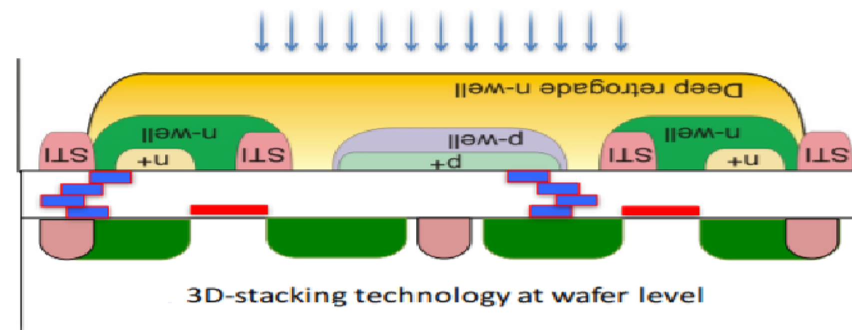


Figure 3: flipped FSI with Direct Bond Interconnection

- red/infrared sensitive due to the junction depth
- not possible to process the top surface after thinning

Proposed 3D BSI Structures

Top Tier :
SOI based SPADs array

- device layer 3 µm thick, medium doping
- handling wafer 650 µm

Bottom Tier :
standard CMOS circuits (Active quenching, pixel TDC, counting control etc.)

- 180 nm used for first prototyping
- 65 nm or below foreseen for further development

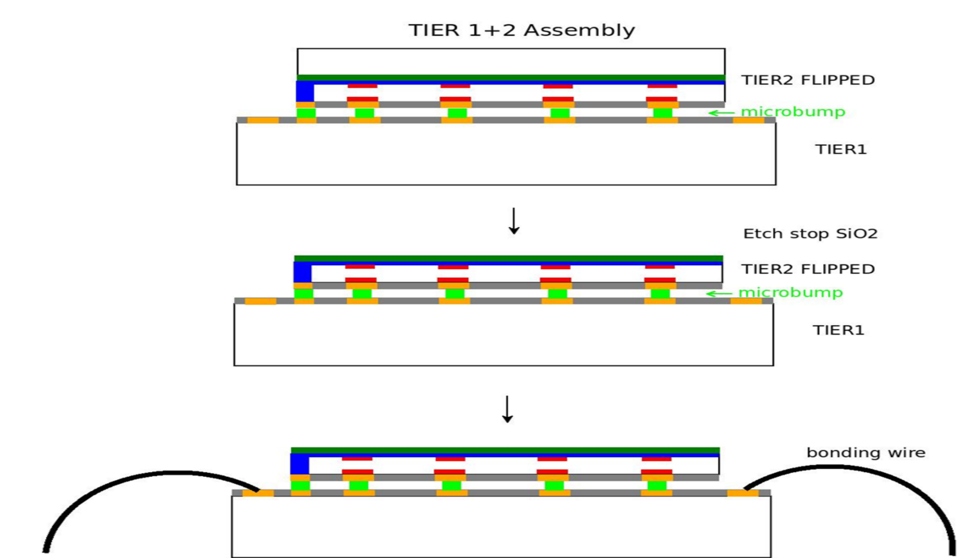
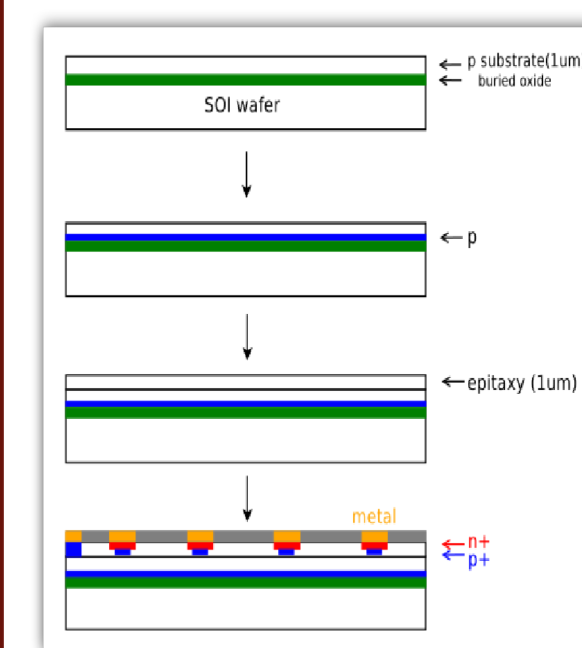


Figure 4: Proposed Back-side Illuminated structure



- BOX layer used as an etching stop during wafer backside etching process
- epitaxy layer to prevent premature breakdown

Figure 5: 3D BSI Blue/UV structure

TCAD Simulation Results

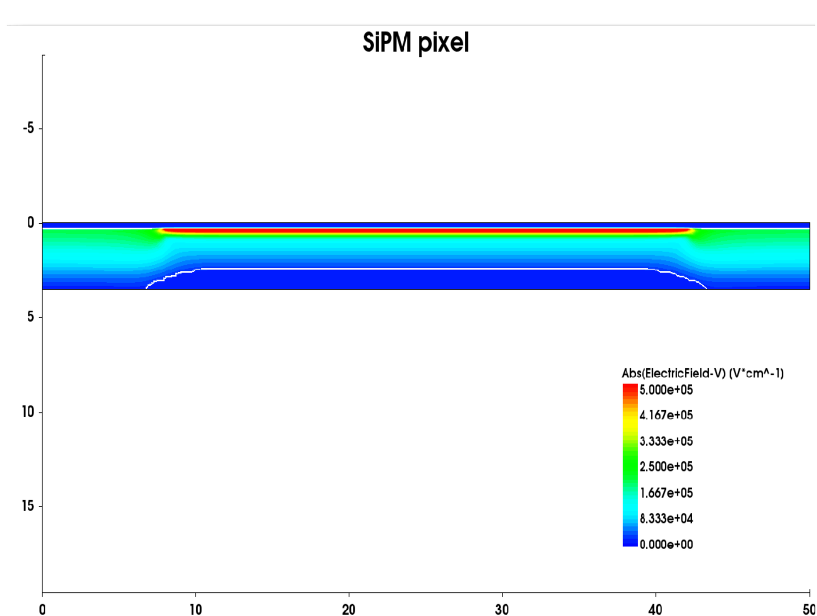


Figure 6: Electric Field color map

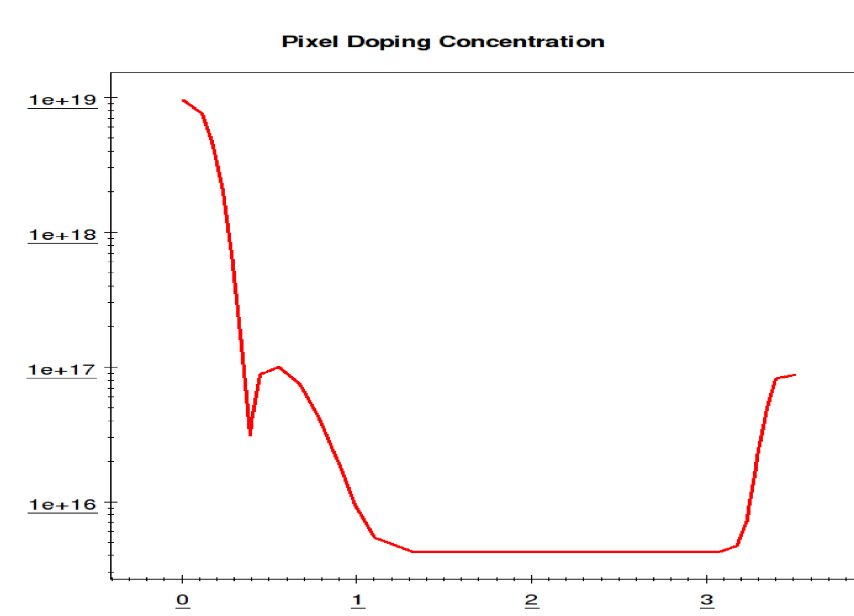


Figure 7: Pixel doping profile in which photons enter from right side (x-axis scale is in microns)

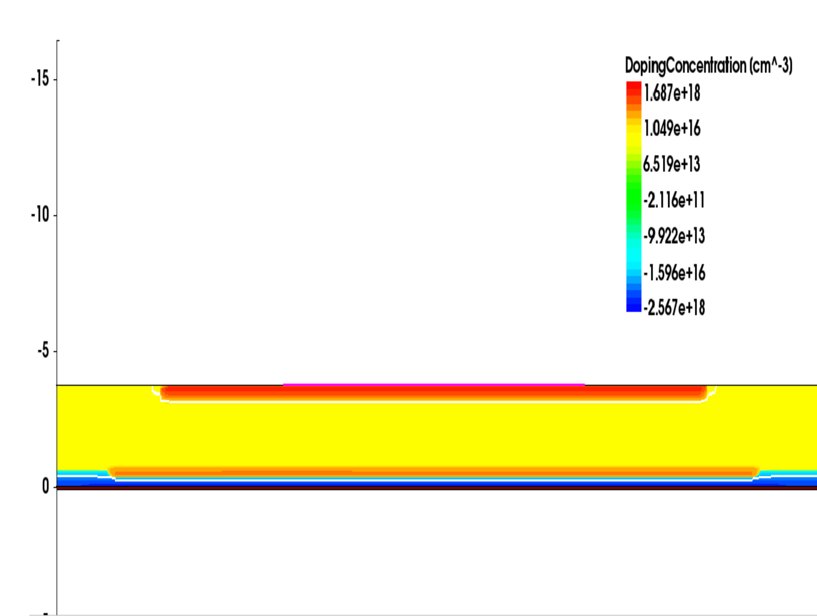


Figure 8: Doping gradient profile to prevent early breakdown

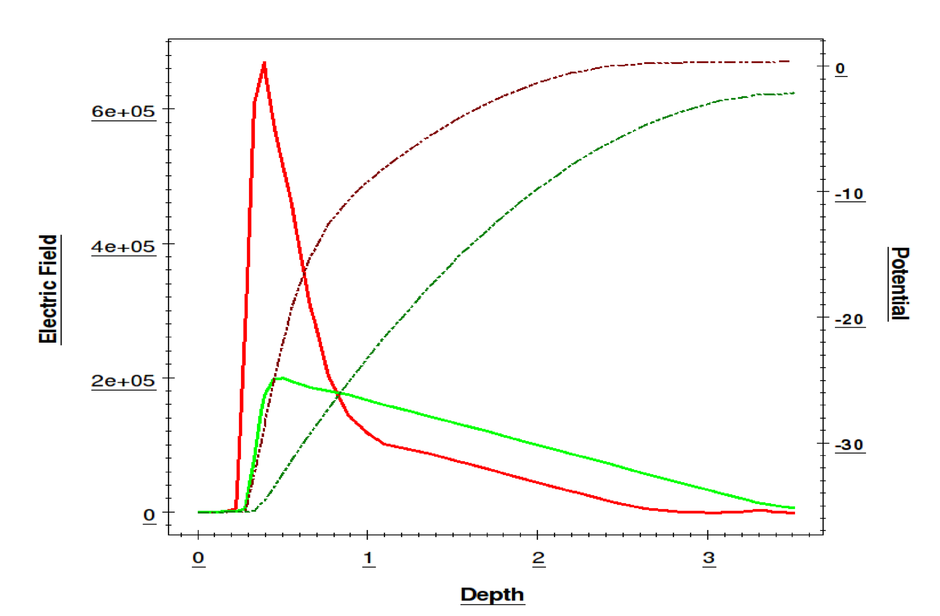
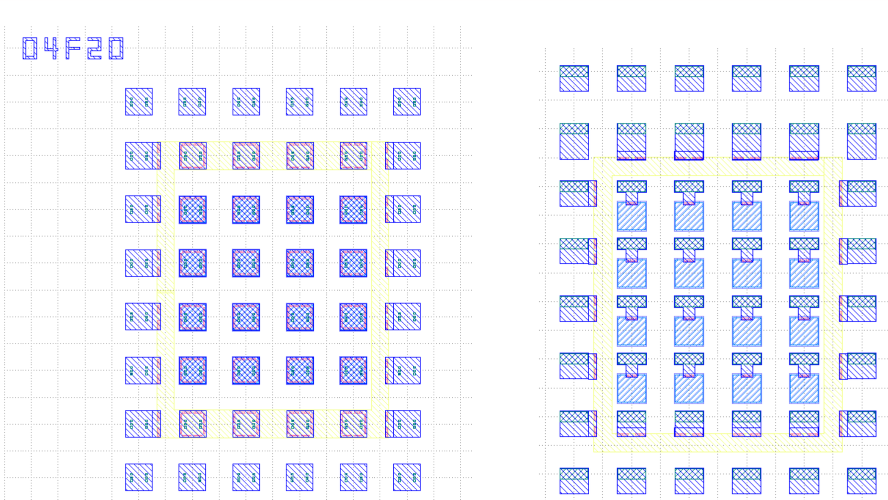


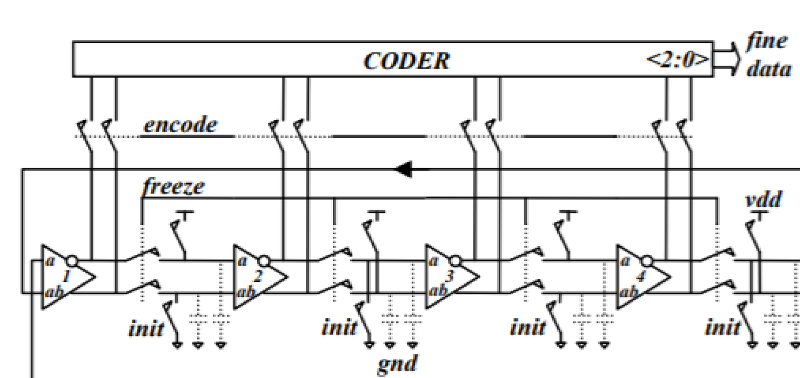
Figure 9: Coorelation among depth, epi-doping and electric field (red=junction area, green=non-junction area)

GDS Files for Mask Production



- in total 2 structures will be tested with 48 variations concerning different guard rings, flip-options, trenches etc.
- masks are under fabrication

CMOS Readout Tier for SPADs



- pixel TDCs are under development
- gated ring oscillator structure under design
- TDC binsize 50ps, pixel processing circuitry

References

[1] M. Lee, P. Sun, G. Pandraud, C. Bruschini and E. Charbon, *First Near-Ultraviolet and Blue-Enhanced Backside-Illuminated Single-Photon Avalanche Diode Based on Standard SOI CMOS Technology*, vol. 25, no. 5, pp. 1-6, Sept.-Oct. 2019, Art no. 3800206 doi: 10.1109/JSTQE.2019.2918930

[2] Myung-Jae Lee, Pengfei Sun, and Edoardo Charbon, *A first Single Photon Avalanche Diode fabricated in standard SOI CMOS technology with a full characterization of the device*, Opt. Express 23, 13200-13209 (2015).