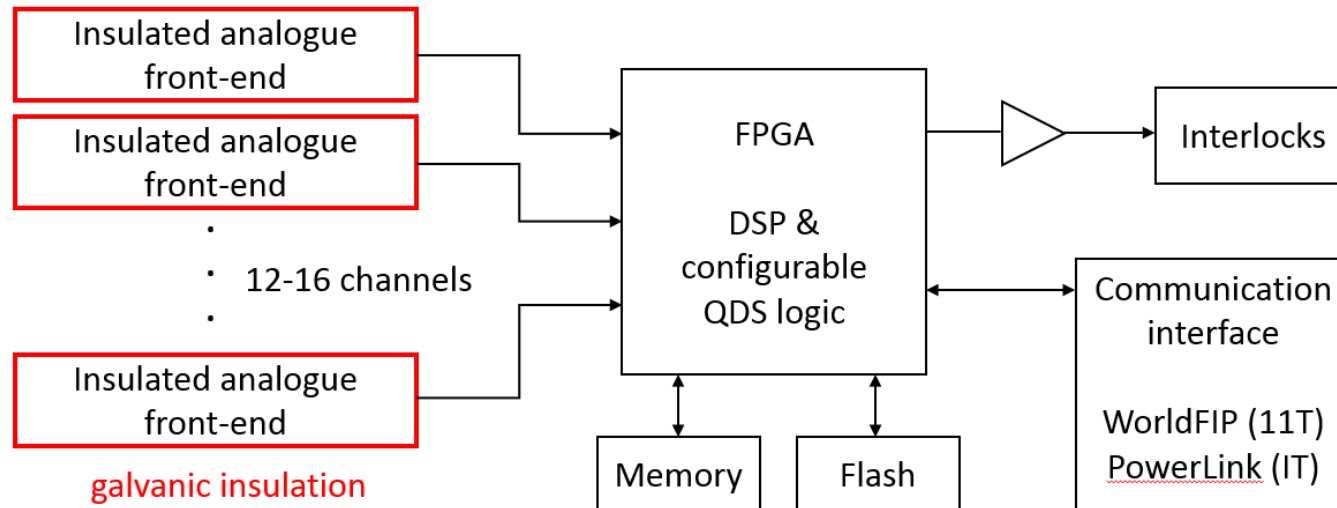# QPS for SFRS TB at CERN

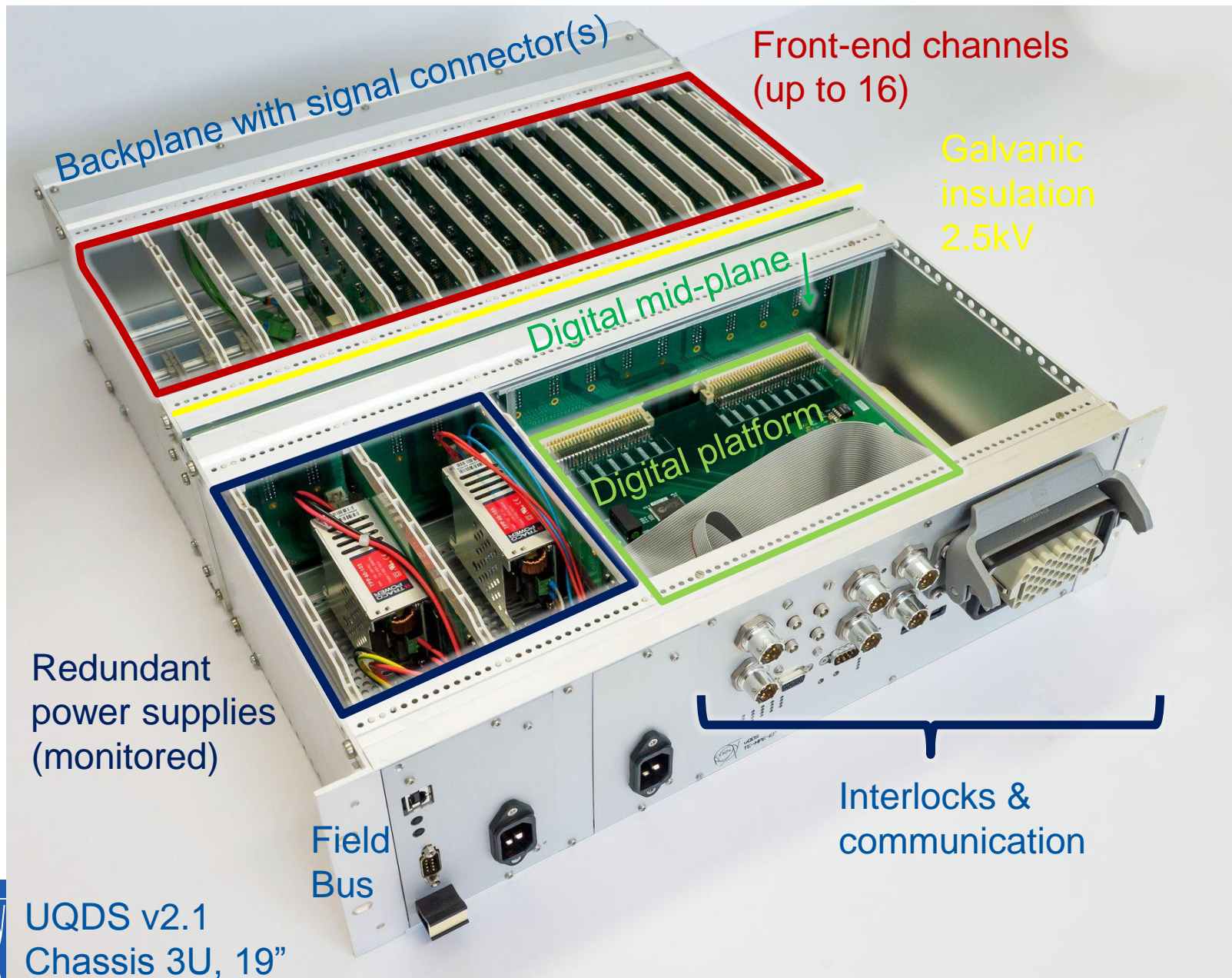Jens Steckert on behalf of TE-MPE-EP

Contents

- UQDS short intro

- Protection scheme

- Thresholds and settings

- Installation

- EE systems

- Commissioning

- Conclusion

UQDS concept

- Multiple front-end channels connected to one logic device performing the QDS tasks
- QDS function defined by FPGA firmware
- Front-ends flexible enough to cope with all required input signals
- Modular concept, one platform for various tasks

UQDS version 2.1 implementation

Backplane with signal connector(s)

Front-end channels (up to 16)

Galvanic insulation 2.5kV

Digital mid-plane

Digital platform

Redundant power supplies (monitored)

Field Bus

Interlocks & communication
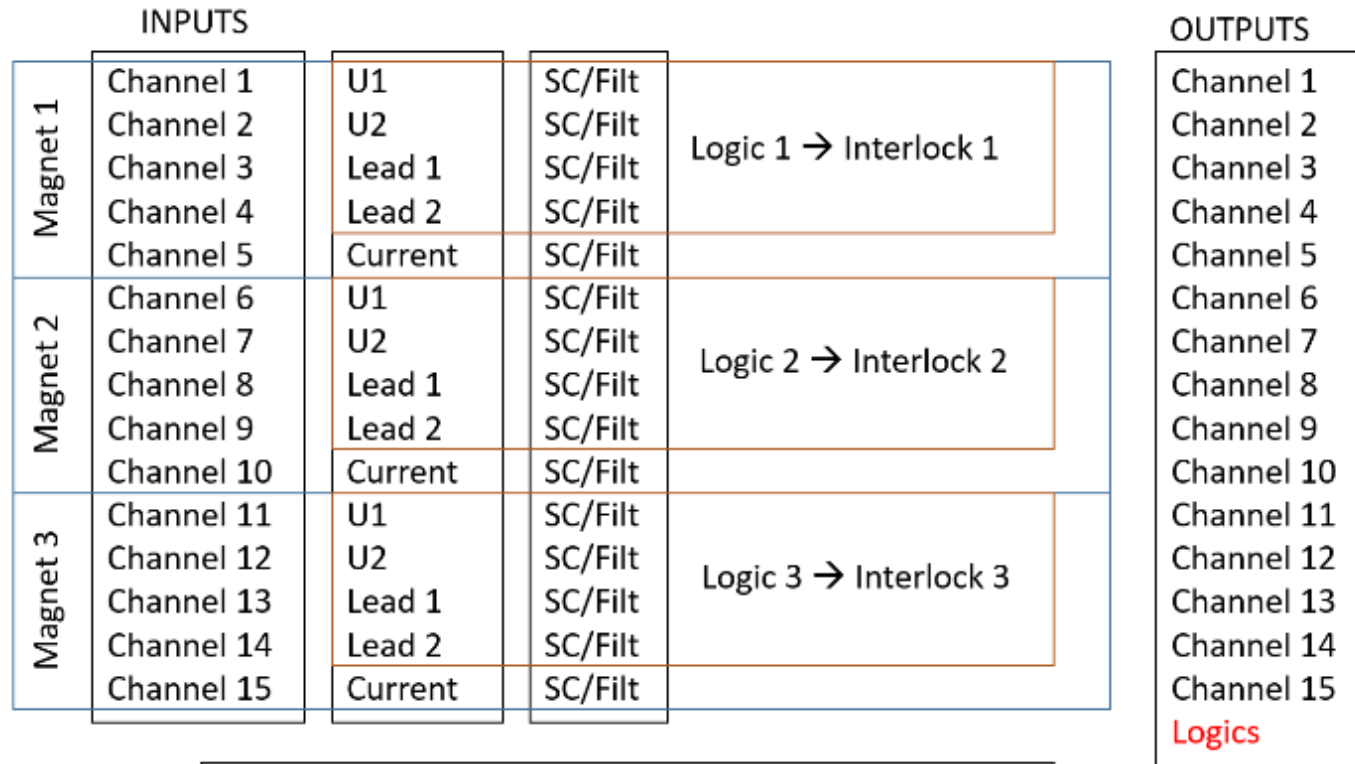
UQDS v2.1 Chassis 3U, 19"

Front-end channel specs

- Magnet voltages: High input range (with divider) up to +/-128V

- Current leads: Standard range (+/-22.5V)

- Resolution: 20 bits

- Analogue bandwidth: 100kHz

- ADC speed (SFRS TB firmware): 307kHz

- Common mode voltage withstand to GND: 2.5kV/30s

- Differential over voltage withstand: 1kV/1s

FPGA firmware

- Protection function is entirely implemented in FPGA firmware

- Most of the parameters are adjustable to adapt to requirements

- Data acquisition of signals used by QDS logic recorded in post-mortem buffer

- One UQDS box serves three circuits generating three independent interlocks

Partition of UQDS box

INPUTS				OUTPUTS
				Channel 1
Magnet 1	Channel 1	U1	SC/Filt	Channel 2
	Channel 2	U2	SC/Filt	Channel 3
	Channel 3	Lead 1	SC/Filt	Logic 1 → Interlock 1	Channel 4
	Channel 4	Lead 2	SC/Filt	Channel 5
	Channel 5	Current	SC/Filt	Channel 6
Magnet 2	Channel 6	U1	SC/Filt	Channel 7
	Channel 7	U2	SC/Filt	Logic 2 → Interlock 2	Channel 8
	Channel 8	Lead 1	SC/Filt	Channel 9
	Channel 9	Lead 2	SC/Filt	Channel 10
	Channel 10	Current	SC/Filt	Channel 11
Magnet 3	Channel 11	U1	SC/Filt	Channel 12
	Channel 12	U2	SC/Filt	Logic 3 → Interlock 3	Channel 13
	Channel 13	Lead 1	SC/Filt	Channel 14
	Channel 14	Lead 2	SC/Filt	Channel 15
	Channel 15	Current	SC/Filt	Logics

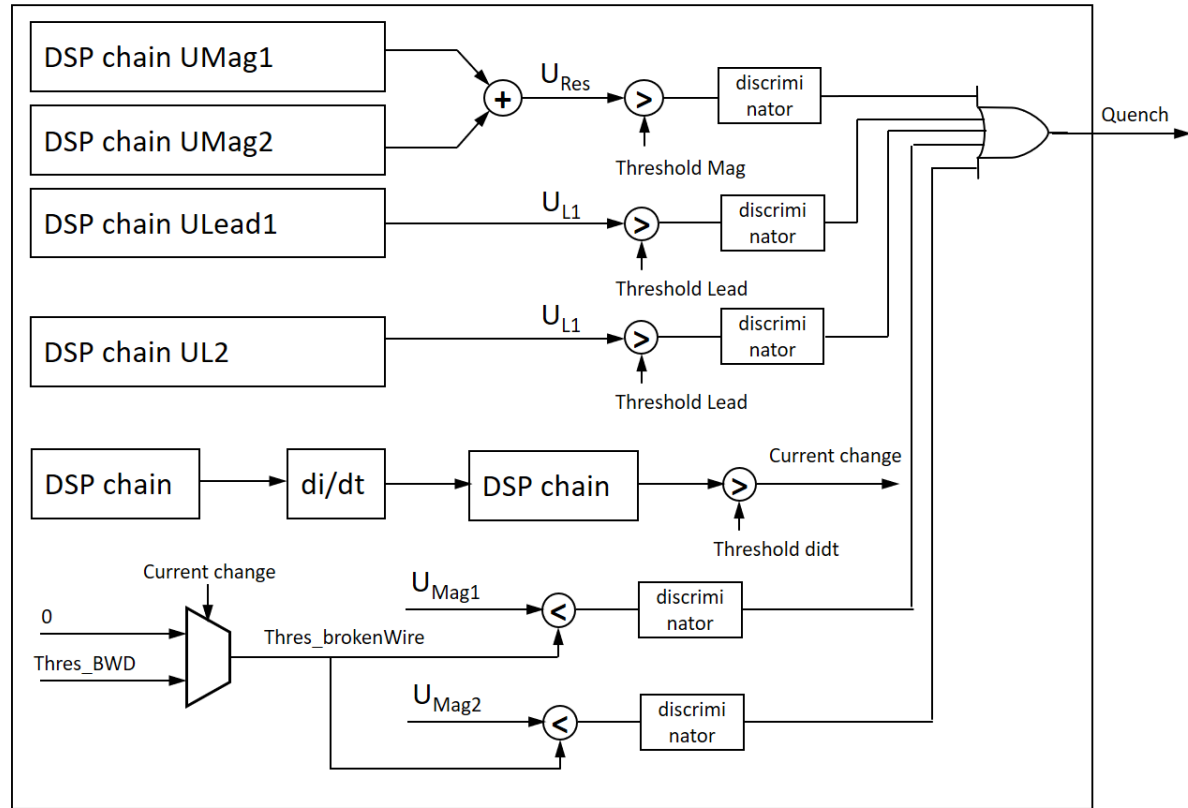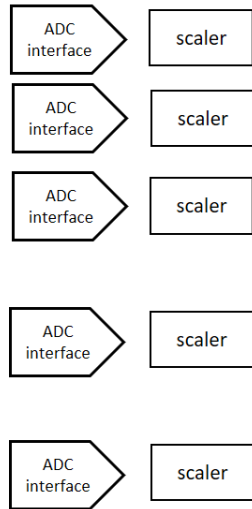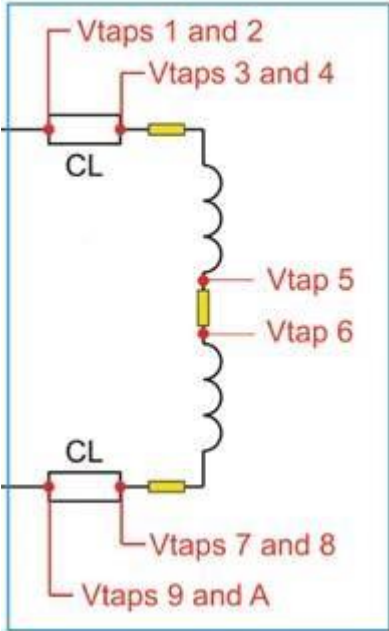Logic 1 OR Logic 2 OR Logic 3 OR SyncIN → PM Buffer

Logic 1 OR Logic 2 OR Logic 3 → SyncOUT

- Inputs: analogue inputs (Vtaps from magnet)
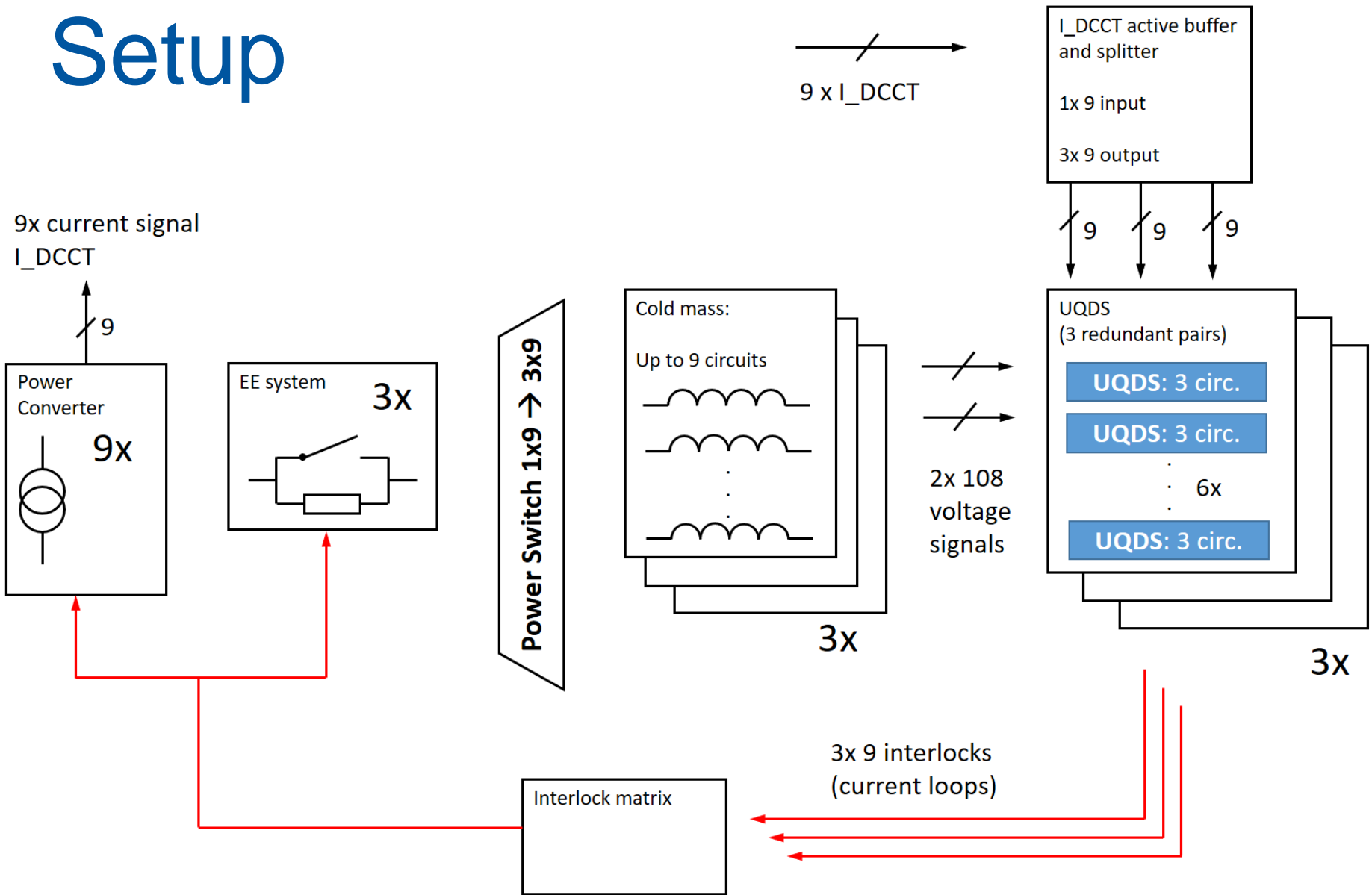- Outputs: Logging data, and logic triggers

Quench detection Logic

Thresholds and settings

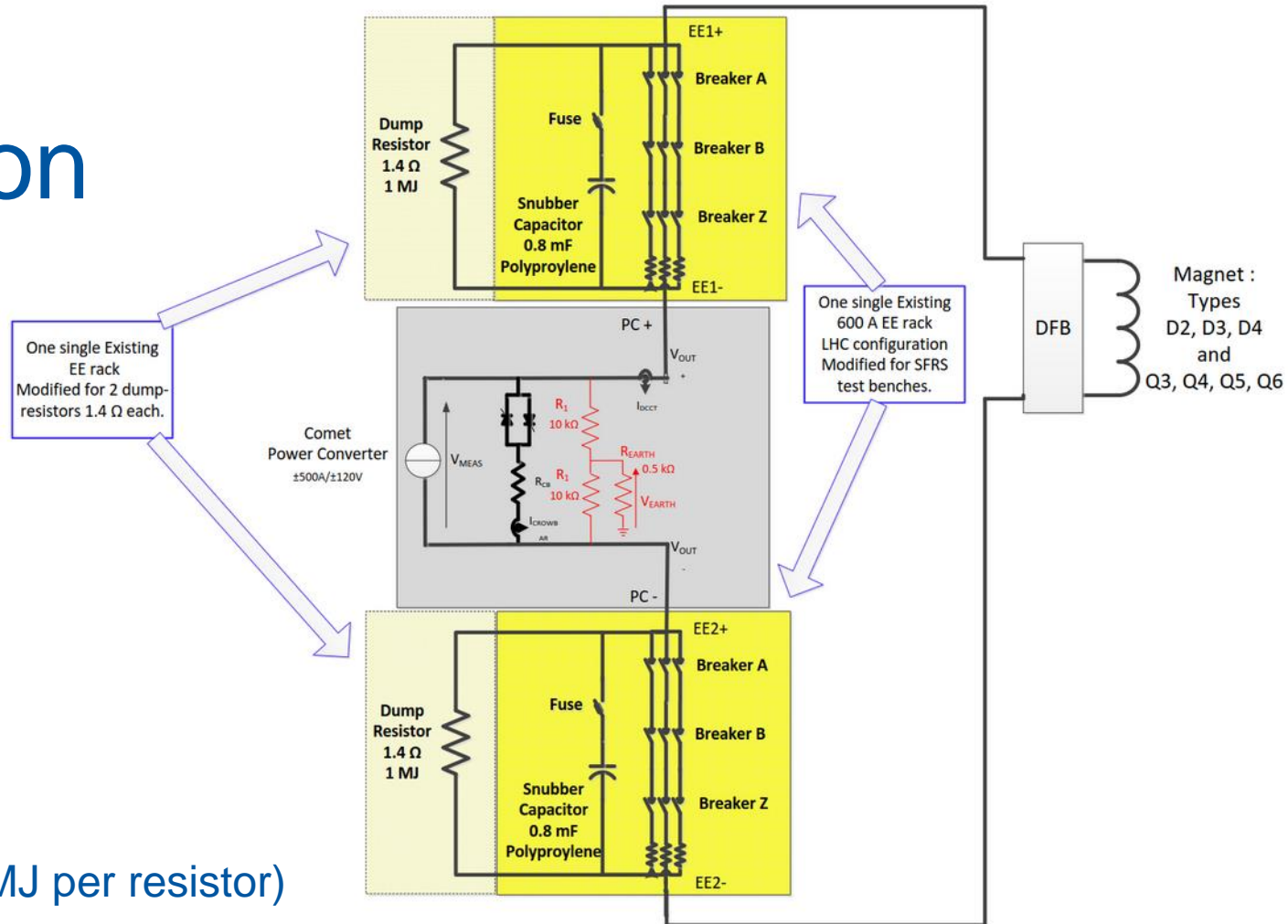| Parameter	Value	Comment
Sampling rate ADC	307.2 kHz	
Decimation factor	32	
QD and DSP frequency	9.6 kHz	Also defines PM freq.
Moving average filter	150 Hz	3rd harmonic of 50Hz
Threshold (Magnet)	600 mV	
Evaluation time (magnet)	6 ms	
Threshold (Lead)	120 mV	
Evaluation time (lead)	6 ms	
PM frequency	9.6 kHz	
PM depth (points)	16384	Can be changed according to user requirements
PM depth (time)	+/-853 ms	
PM readout time	1634 s	

Full installation

- 3 Test benches with up to 9 circuits each

- One UQDS box can handle 3 circuits

- 3x UQDS per TB: 9 boxes

- Each box is redundant: 18 UQDS boxes required

Setup

9 x I_DCCT

I_DCCT active buffer and splitter

1x 9 input

3x 9 output

9 9 9

9x current signal
I_DCCT

9

UQDS
(3 redundant pairs)

UQDS: 3 circ.

UQDS: 3 circ.

6x

UQDS: 3 circ.

3x

Power
Converter

9x

EE system

3x

Power Switch 1x9 → 3x9

Cold mass:

Up to 9 circuits

3x

2x 108
voltage
signals

3x 9 interlocks
(current loops)

Interlock matrix

Energy Extraction

Max load: 2MJ (1MJ per resistor)

Grounding principle: Mid-point of total dump-resistor of 2.8 Ω .

Maximum: 450 V per 1.4 Ω dump-resistor during extraction (Q6 at I_ulti of 321 A)

Power converter voltage during extraction:

Common mode: gnd. In case of earthfault (worst-case): 450V

Commissioning

- Connection test by ELQA → completed

- Commissioning at low currents:

  - Setup of parameters, thresholds etc.

  - Setup of di/dt based vtap supervision

  - Measurement of gain balance

  - Filter settings (depending on real noise condition)

  - Interlock test → only valid if whole system is operational

Status

- UQDS based system installed

- Gateway installed and running

- Patch box installed

- Current splitter box installed

- Firmware in final verification

➔ Ready for commissioning

Conclusion/Outlook

- Application of UQDS to FAIR TB
- Dedicated channel with wide input range (+/-128V) for magnet voltages developed
- Additional hardware (Patch box and current splitter box) produced and commissioned
- Dedicated firmware for FAIR TB
- Hardware installed
- Next step: Commissioning

Broken wire detection
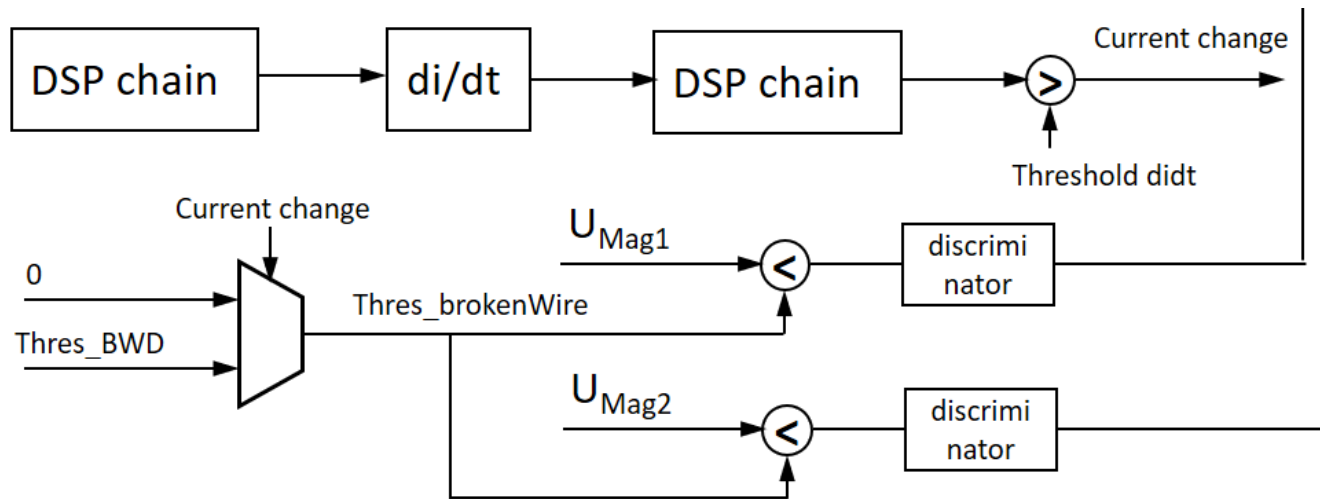
- Derivative of current serves as indicator to detect ramps
- If di/dt threshold is exceeded, system assumes a current ramp
- During a current ramp, system expects a voltage drop over the magnet coils
- A current ramp without voltage drop triggers an abort
- Thresholds for ramp detection & U_{mag} have to be set in the field during commissioning