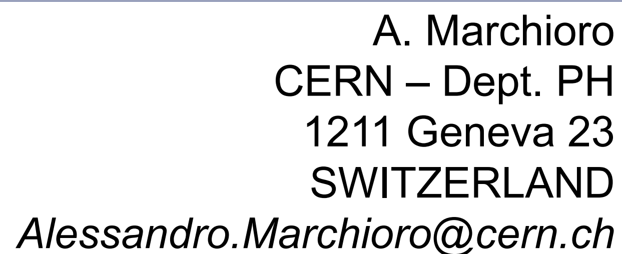
Microelectronic technologies for HEP Instrumentation



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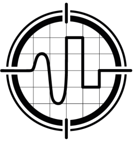
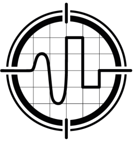
Question



- *Why is microelectronics so important for building detectors for particle physics?*

1. Because it allows more compact detectors
2. Because it allows cheaper detectors
3. Because it allows more “intelligent” detectors
4. Because it allows more “sensitive” detectors
5. Because it allows more “precise(*)” detectors
6. All of the above

(*): space, time, energy



Mythology on "Sensitivity"

Commercial cameras FWC

Canon 5D	*CMOS*	*80,000*
Canon 1DMII	*CMOS*	*79,900*
Canon 1DMIII	*CMOS*	*70,200*
Canon 5DIII	*CMOS*	*68,900*
Canon 5D II	*CMOS*	*65,700*
Nikon D3	*CMOS*	*65,600*
Canon 1D IV	*CMOS*	*55,600*
Canon 30D	*CMOS*	*51,400*
Canon 20D	*CMOS*	*51,400*
Canon 20Da	*CMOS*	*51,400*
Canon 300D	*CMOS*	*45,500*
Canon 10D	*CMOS*	*44,200*
Canon 40D	*CMOS*	*43,400*
Canon 350D	*CMOS*	*43,000*
Nikon D300	*CMOS*	*42,000*
YM-3170A	*CMOS*	*35,000*
Canon 50D	*CMOS*	*27,300*
Canon 7D	*CMOS*	*24,800*
Canon 60D	*CMOS*	*24,800*
MT9D131	*CMOS*	*17,000*

IEDM 2019: Samsung 64MP Sensor with 0.8um Dual CG Pixel

December 27, 2019 By Vladimir Koifman   Leave a Comment

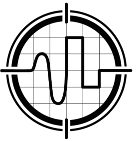
Image Sensors World   Go to the original article...

Samsung IEDM 2019 paper "A 0.8 µm Smart Dual Conversion Gain Pixel for 64 Megapixels CMOS Image Sensor with 12k e- Full-Well Capacitance and Low Dark Noise" by Donghyuk Park, Seung-Wook Lee, Jinhwa Han, Dongyoung Jang, Heesang Kwon, Seungwon Cha, Mihye Kim, Haewon Lee, Sungho Suh, Woong Joo, Yunki Lee, Seungjoo Nah, Heegeun Jeong, Bumsuk Kim, Sangil Jung, Jesuk Lee, Yitae Kim, Chang-Rok Moon, and Yongin Park presents the company's latest generation sensor:

"A 0.8 µm-pitch 64 megapixels ultra high resolution CMOS image sensor has been demonstrated for mobile applications for the first time. Full-well capacity (FWC) of 6k e- was achieved in 0.8 µm pixels as the best in the world, and the advanced color filter (CF) isolation technology was introduced to overcome sensitivity degradation. Dual conversion gain (CG) technology was also first applied to mobile applications to improve the FWC performance of Tetracell up to 12k e-. In addition, highly refined deep trench isolation (DTI) and photodiode design significantly improved dark noise characteristics."

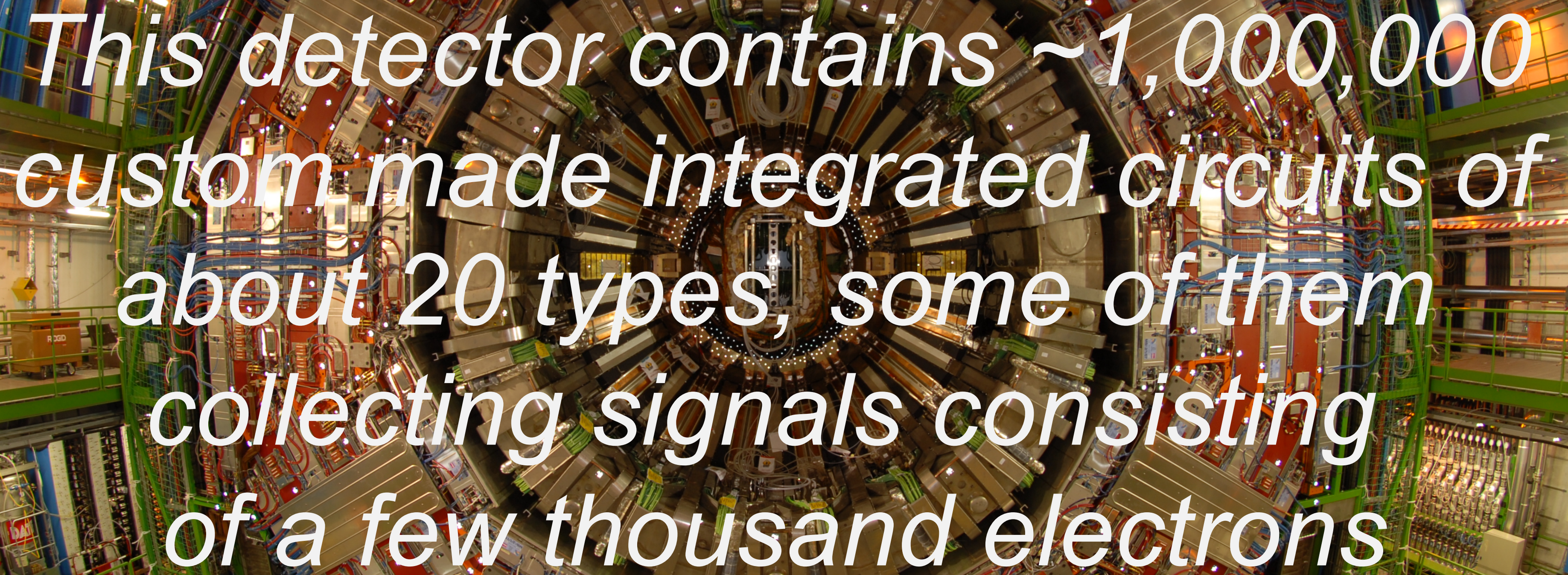
from: https://image-sensors-world.blogspot.com/2019/10/iedm-2019-sony-presents-48mp-all-pixel.html

Topics



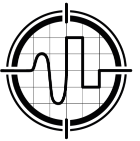
- Motivations
- What is microelectronics ?
- Trends and upcoming limitations

- What can you do with microelectronics ?
- Take home message

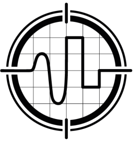


This detector contains ~1,000,000 custom made integrated circuits of about 20 types, some of them collecting signals consisting of a few thousand electrons

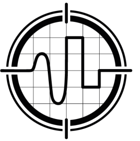
Motivations and Trends in HEP



- Generation 0.1 (1980's) of chips for experiments where essentially integrated custom amplifiers for sensing detector signals
- The LHC 1.0 generation (late '90s) are full multichannel systems to cover large surfaces of silicon detectors and/or large number of calorimeter channels
  - Pixels and strip electronics are essentially position sensitive detector with little if any high level discrimination capabilities
- Next generation:
  - Larger areas at lower cost
  - Much improved functionality (meaningful data out, not just DN)
  - Digital can help analog (like in so many commercial devices)
    - E.g.: simplify tedious calibration and stability monitoring tasks
  - Embedded processing: digital filtering, particle discrimination, cluster reduction …
    - Energy and/or momentum (vector)
    - Timing
  - Unique digital functionality
    - Example: Associative Memories for Fast track recognition
  - Full channel digital signal processing (but physicists need to be educated…)



Microelectronics in HEP



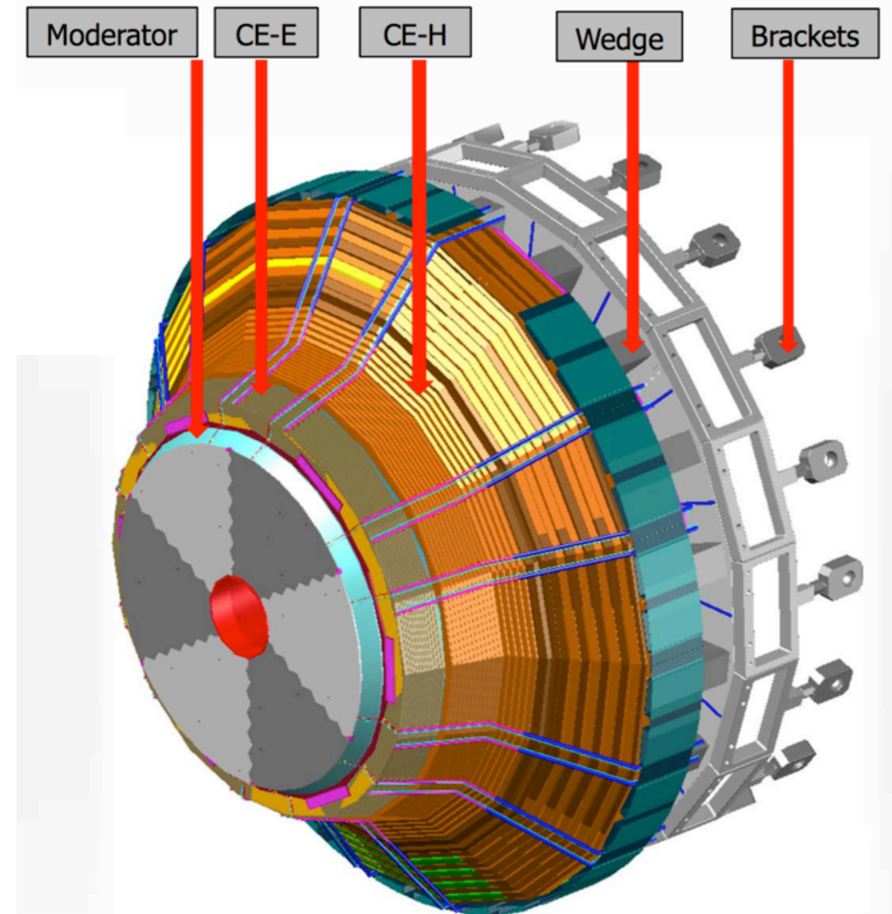
Microelectronics in HEP

Key Parameters:

- *CMS-HGCAL covers $1.5 < \eta < 3.0$*
- *Full system maintained at -30°C*
- *~600m² of silicon sensors*
- *~500m² of scintillators*

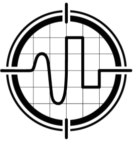
- *6M Si channels, 100K custom chips:*
  - *0.5 / 1.1 cm² cell size*
  - *~27000 Si modules*

  - *$30 \times 6\ 10^6 \times 40\ 10^6 =$*
    $7.2\ 10^{15}$ bits/sec
  - *~16 bit dynamic range*
  - *220 KW*



E-H Calorimeter in CMS

Electronic Camera



Simulation of HL-LHC pileup events in CMS

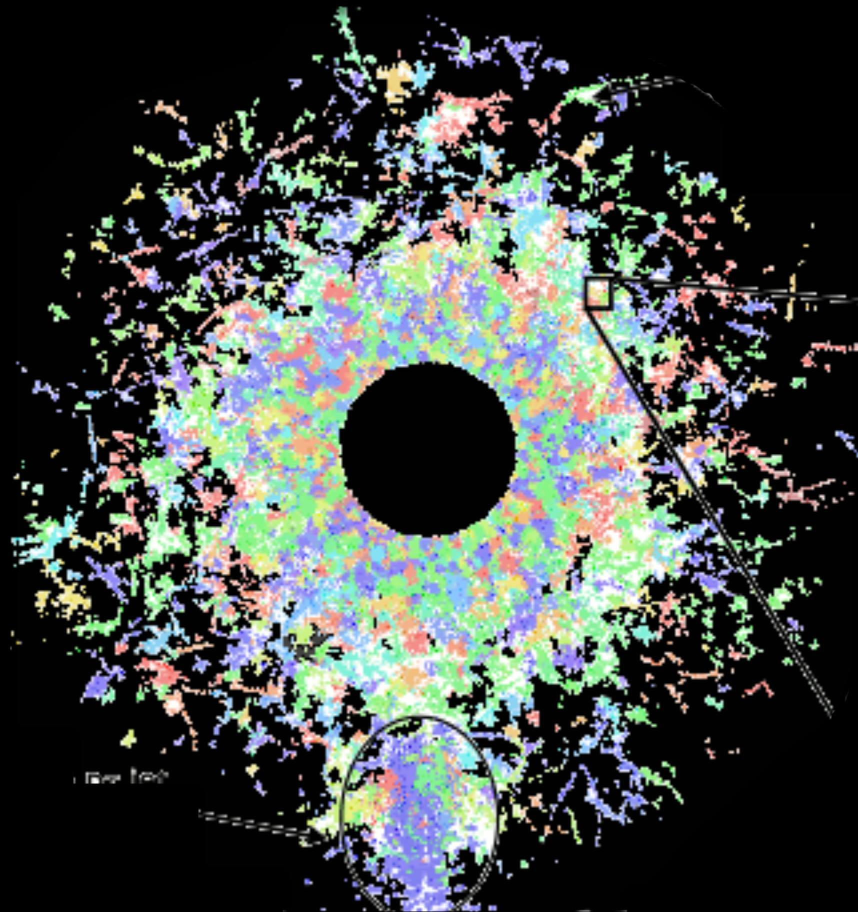
Tracks and clusters clearly identifiable by eye throughout most of detector.

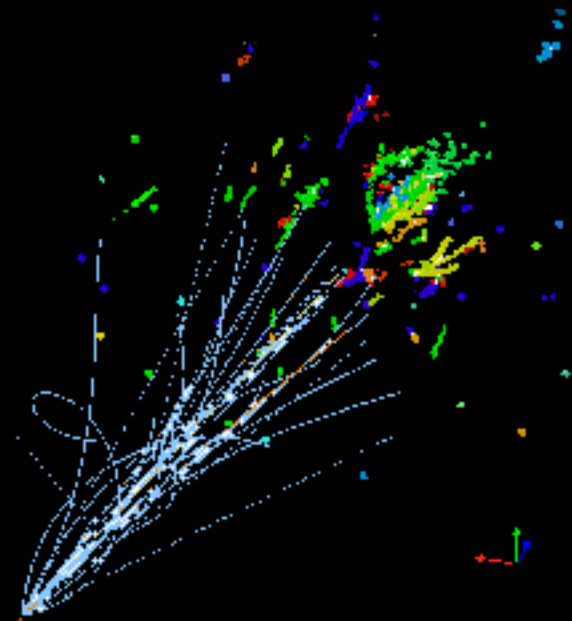
the longitudinal shower footprint

CMS Experiment at LHC, CERN
Data recorded: Thu Jan 1 01:00:00 1970 CEST
Run/Event: 1 / 10
Lumi section: 1

high p_T jet
O(500 GeV)

Electronic Camera

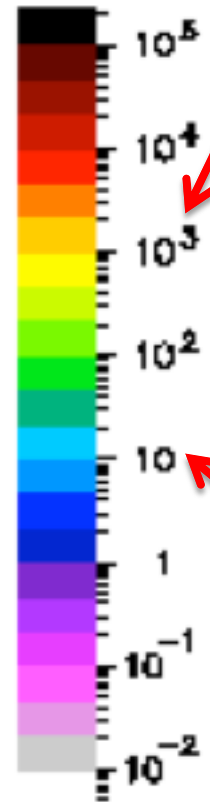




Extra wishes

Extreme environment

Radiation levels in Atlas run 1:
Charged particles, full view



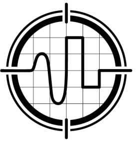
Typical space environment

Mortal dose for humans

Gy/10y

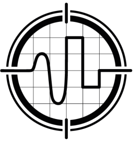
What is microelectronics?

And why is digital important



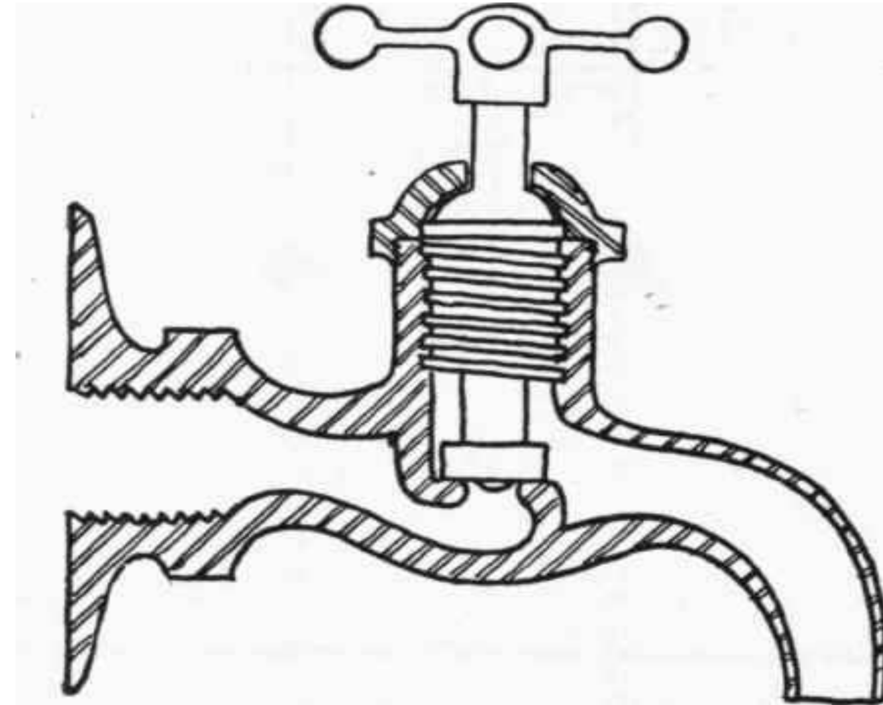
What is microelectronics?

- Combination of two factors
  - Technology
    - Capability to “print” on a piece of silicon of about 1 cm^2 some 10^9-10^{11} transistors (working mostly as “switches”) of size < 10 nm, each one of which has to work perfectly for 10+ years
    - repeat the above for ~100M pieces
    - … and then sell them for O(10$) / pc.
  - Tools
    - Capability to manage the design and the fabrication of these extremely complex systems-on-chip designed by teams of 100+ engineers



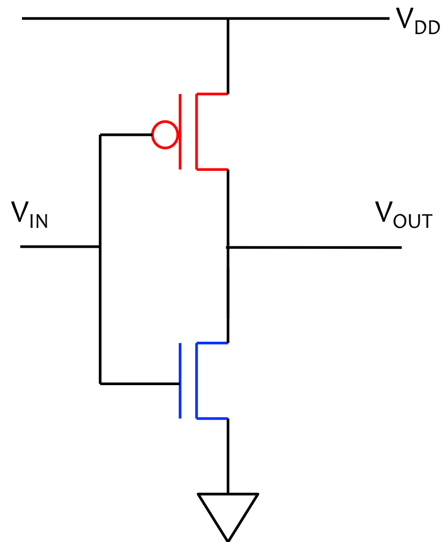
What do we want from a transistor anyway? (sorry analog engineers…)

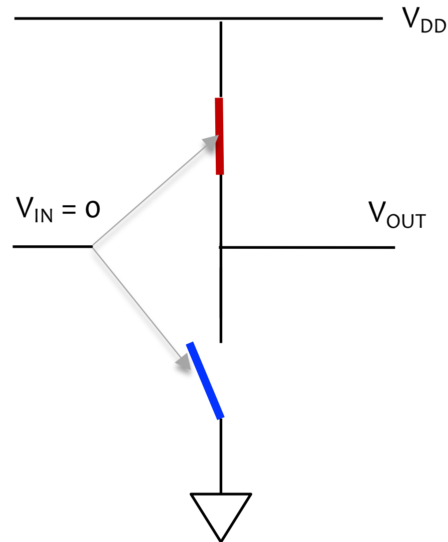
- A transistor (a digital transistor) is a device that "should" have the following characteristics:
  - works as a switch (*on* or *off*), if bi-directional it is even better
  - three terminals: an input, an output, a control
  - makes a "sharp" transition between the two states (open or closed) in a time as short as possible (i.e. carry charge quickly through it)
  - no leakage current when off (I_{on}/I_{off} >(>) 10^6)
  - … while delivering high current when on (drive strongly the load), $I_{on,min}$ ~ 1mA/um
  - the control terminal induces a transition between the two states with a voltage drive (V_{tr}) as small as possible: $P = ½ C V_{dd}^2$ (today V_{tr} ~ 1/3 V_{dd})
  - the control terminal should not be influenced by input/output terminal(s)
  - be physically small (otherwise other "parasitics" ruin the party)
  - must have complementary type (i.e. a second type which is turned on when the first is turned off using the same "control").

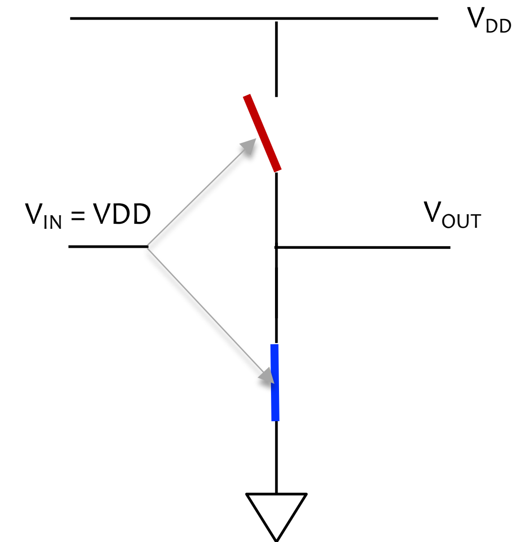


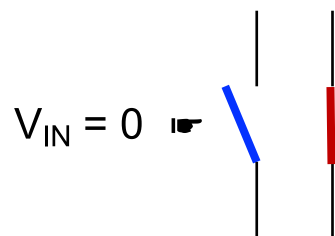
- "Good analog" characteristics are desirable but by far not necessary or even important for the the majority of applications.
  - In fact modern deep-submicron devices have "horrible" analog characteristics and analog designers have a very hard time to achieve what was "easy" 20 years ago

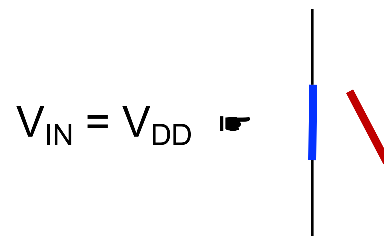
Simple Inverter Gate



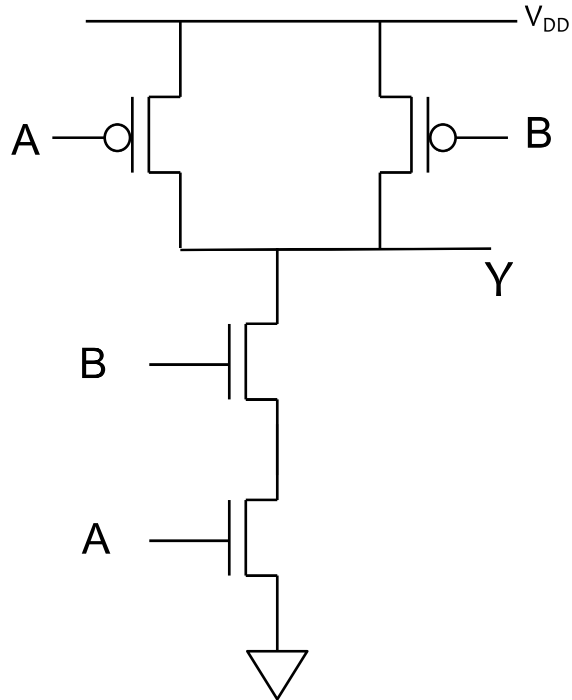


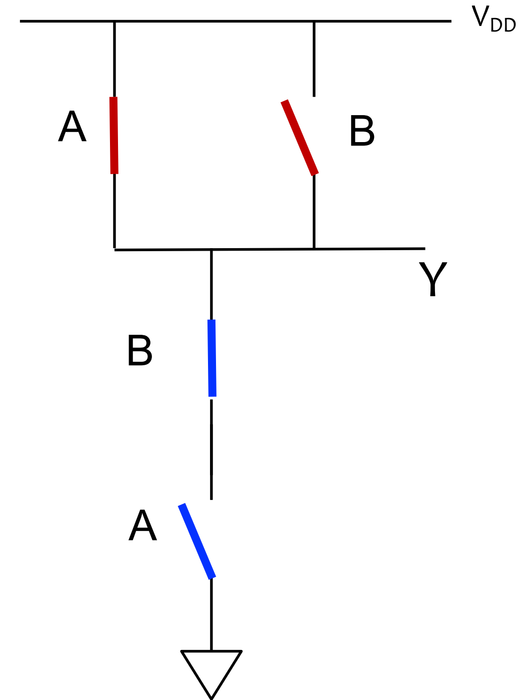






Simple NAND Gate

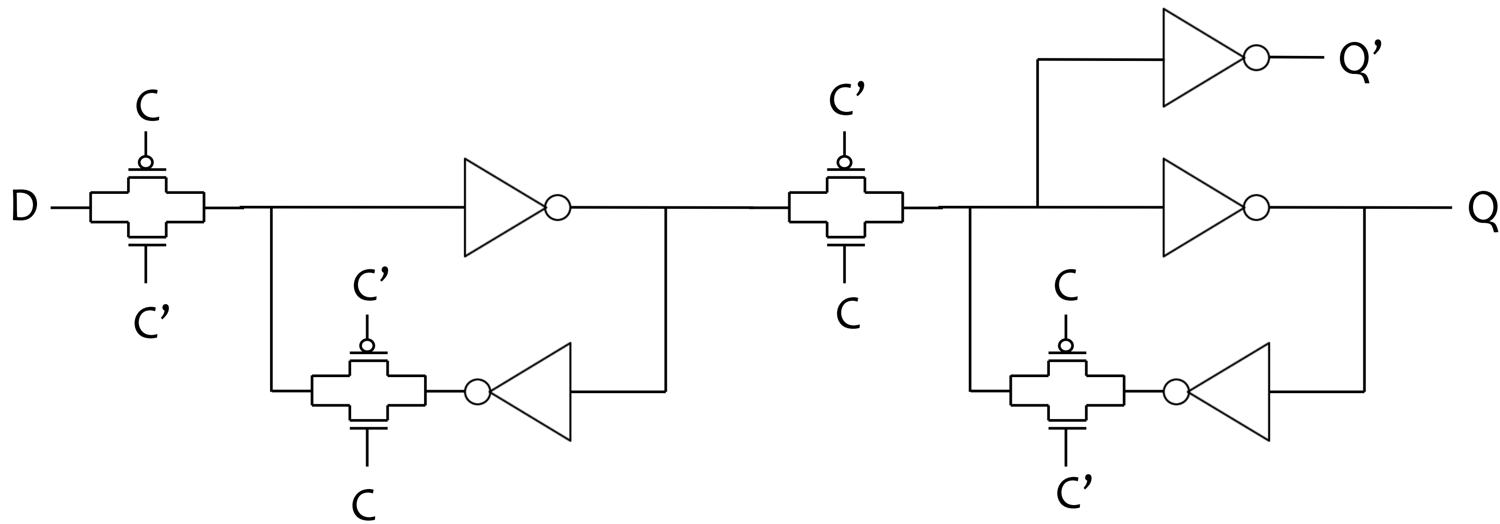


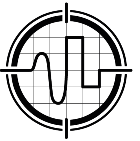


NAND

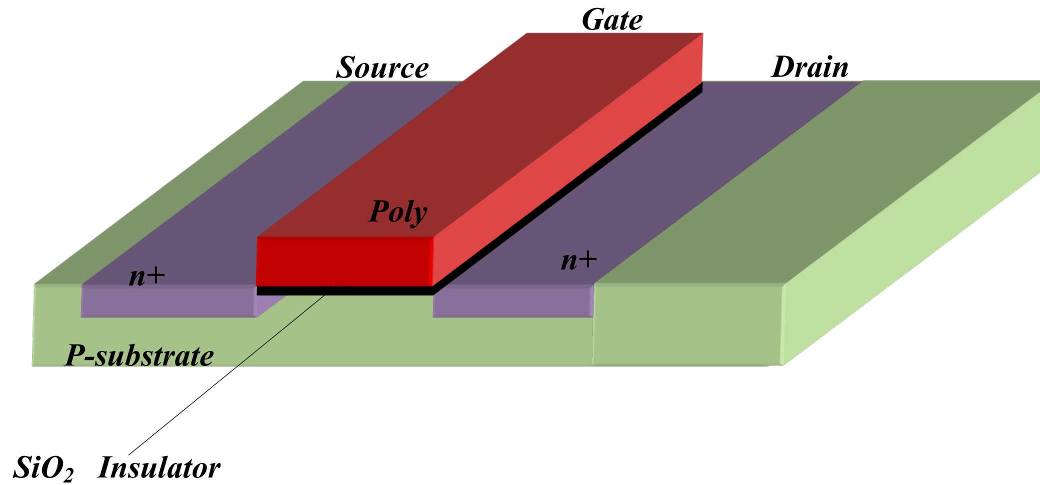
A = 0, B = 1 ☛ Y = 1

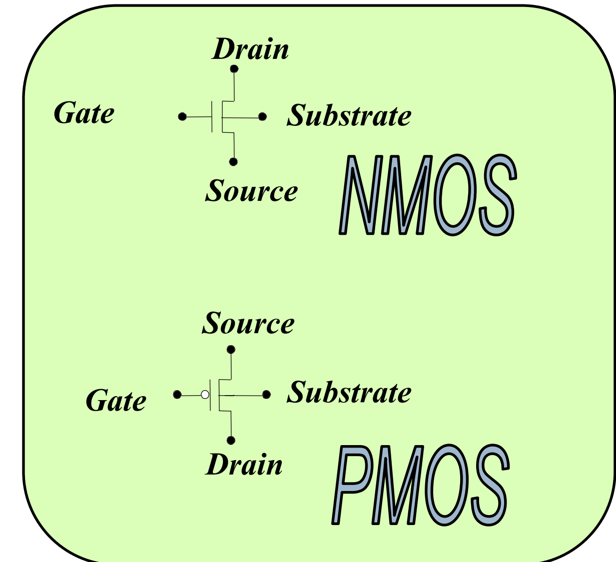
Flip-Flop Memory Element



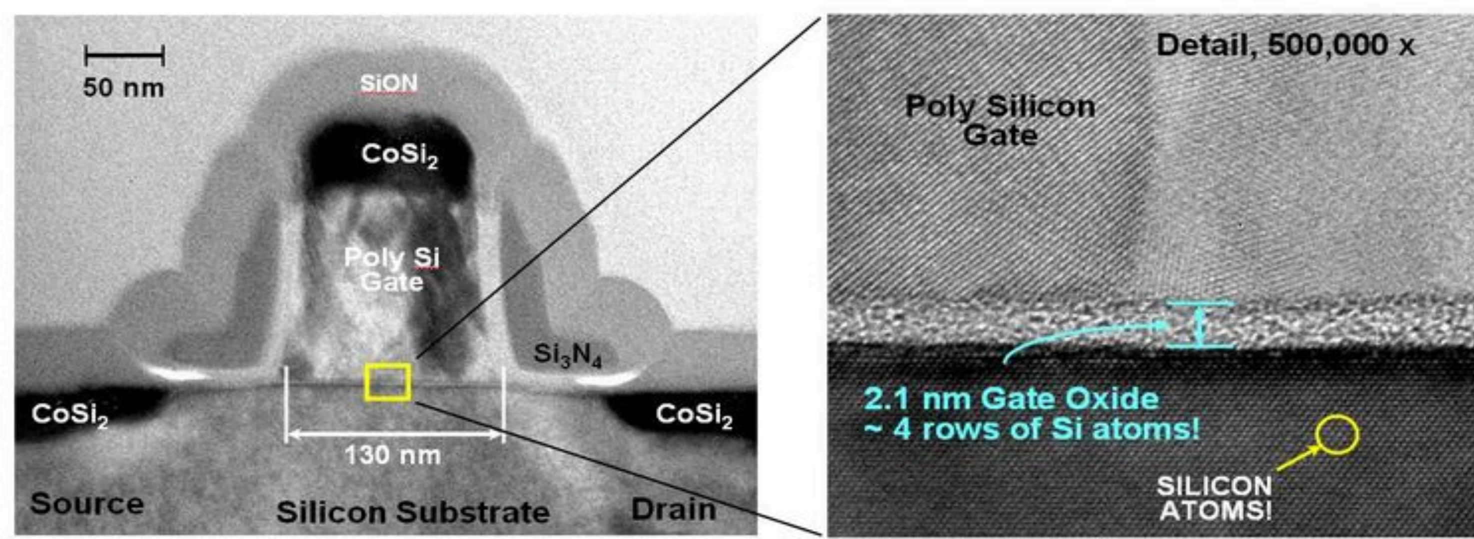


MOS transistors





MOS tra



GATE

SiO_2

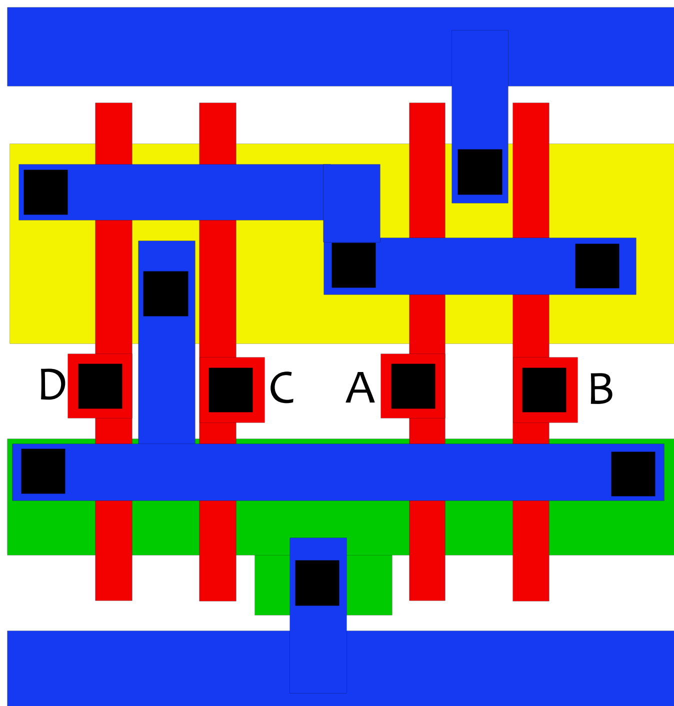
n+

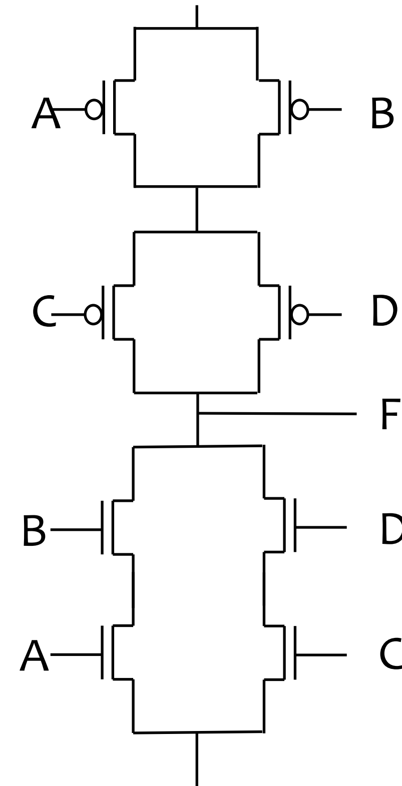
n+

SOURCE

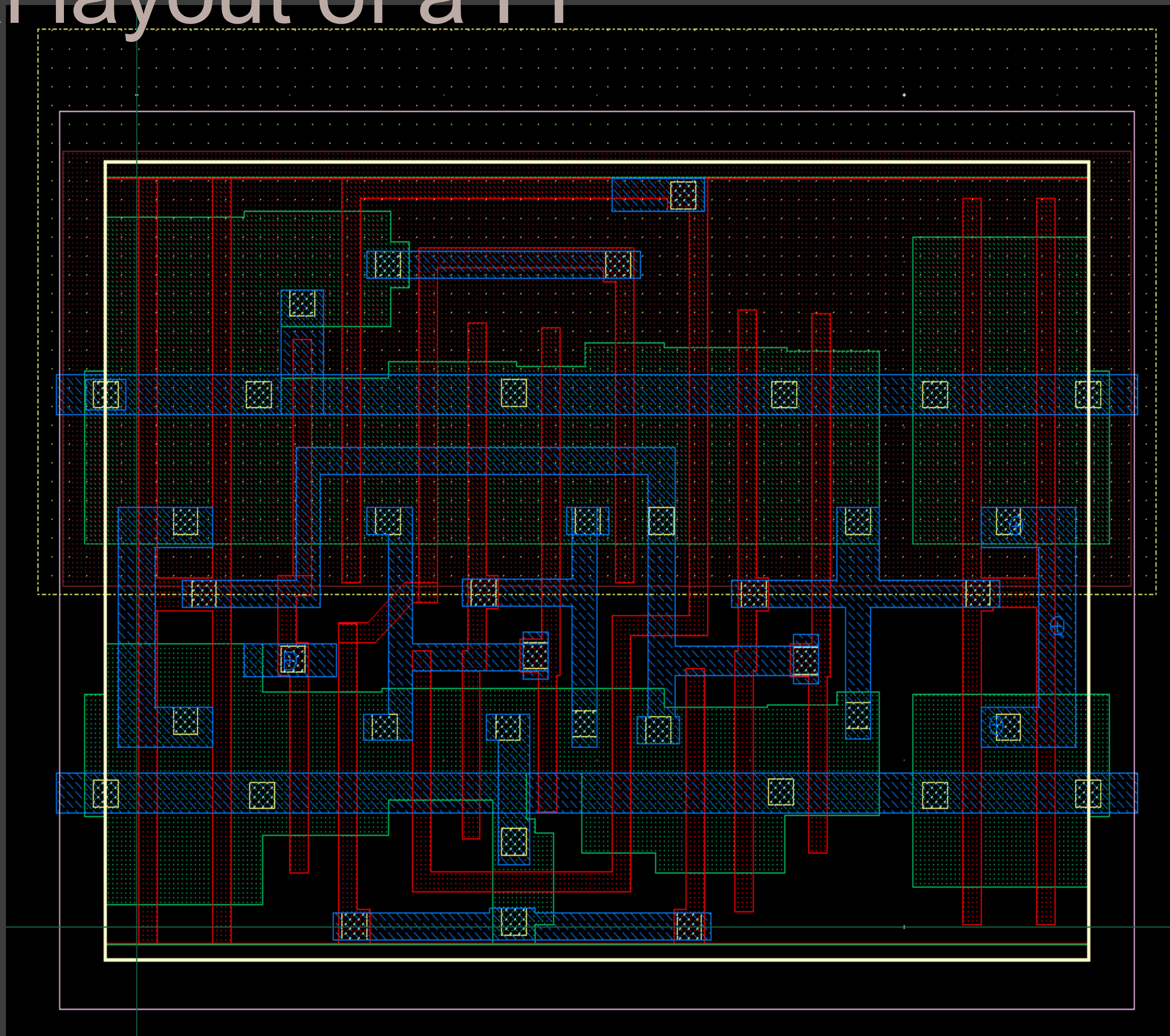
DRAIN

Simplified layout of a logic gate

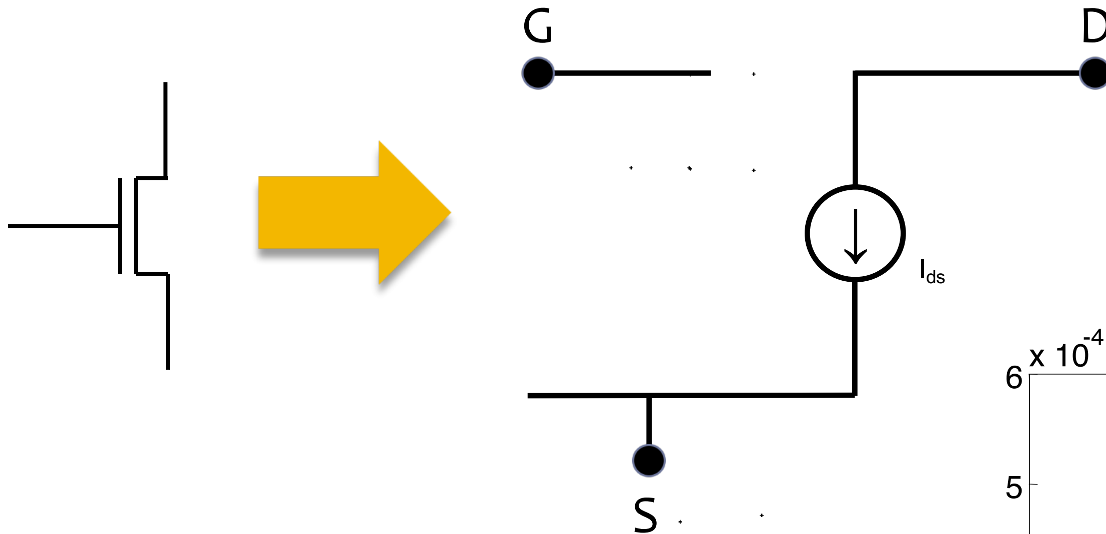


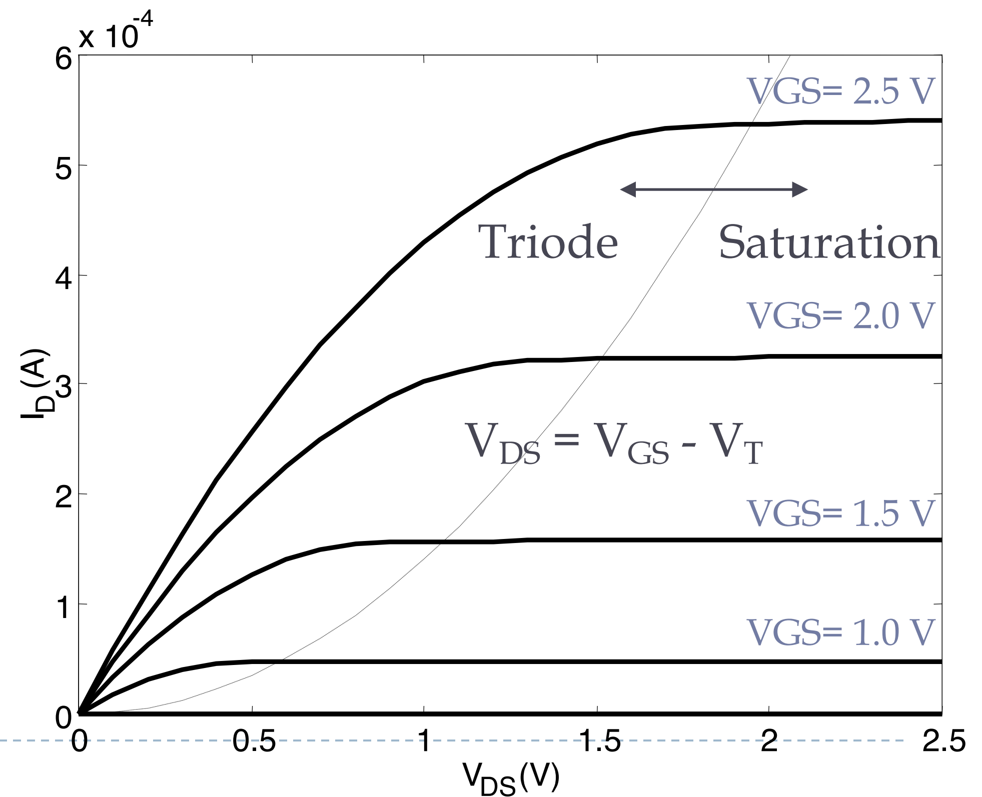


Real layout of a FF

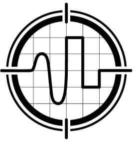


MOS (very) simple model





MOS Transistor equations



$$I_{ds} = \frac{\mu\varepsilon}{t_{ox}} \frac{W}{L} \left((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right) \quad Non-saturation$$

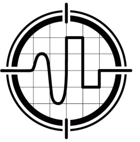
$$I_{ds} = \frac{\mu\varepsilon}{2t_{ox}} \frac{W}{L} (V_{gs} - V_t)^2 \quad Saturation\ region$$

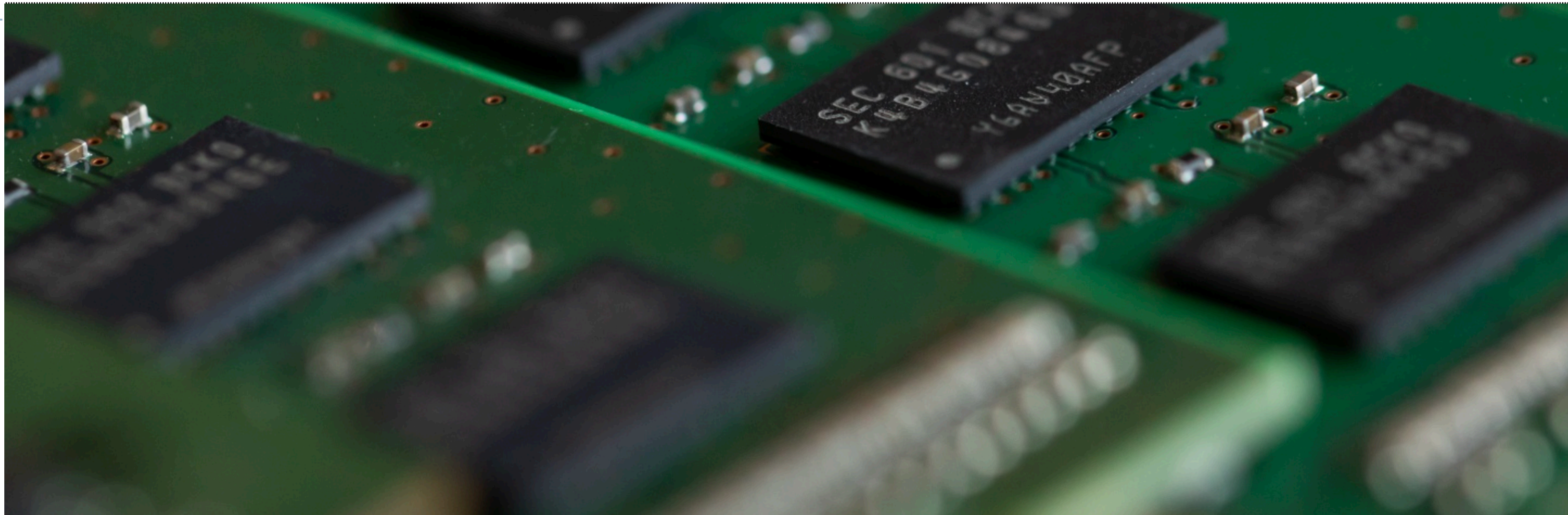
Manufacturing parameters,
can't be changed on a given technology

Geometric parameters
Defined at layout time

Electrical parameters
Depend on circuit behavior

https://www.bloomberg.com/news/articles/2019-12-23/behind-samsung-s-116-billion-bid-for-chip-supremacy





Photogra

Technology

Behind Samsung's $116 Billion Bid for Chip Supremacy

By Sohee Kim

December 23, 2019, 1:50 AM GMT+1

- Custom chips are the future that Samsung wants to profit from
- Laying the foundation for expanding its semiconductor empire

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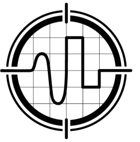
How one Taiwanese firm uses unrivalled technology to dominate the world's chip-making industry



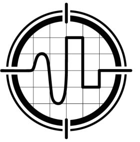
One of the difficulties: Lithography

Contact
1978

32nm SRAM
Cell 2008

1 µm

Lithography (2)



45 nm MOS

193 nm light

Metal

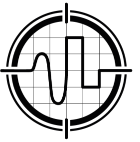
High-k

SiGe

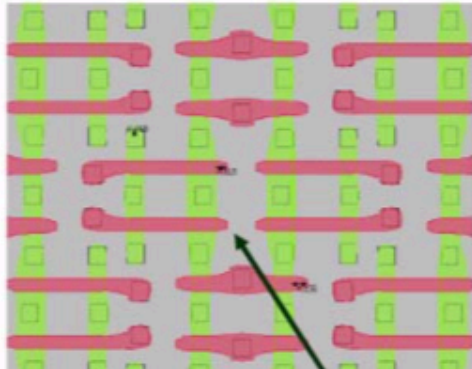
SiGe

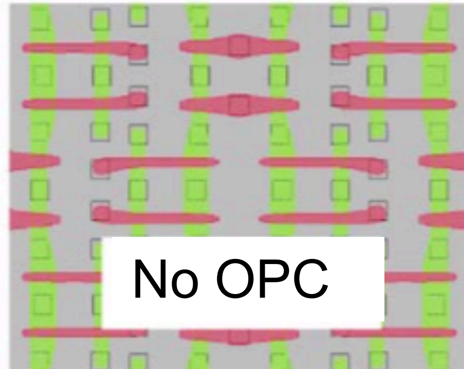
Silicon

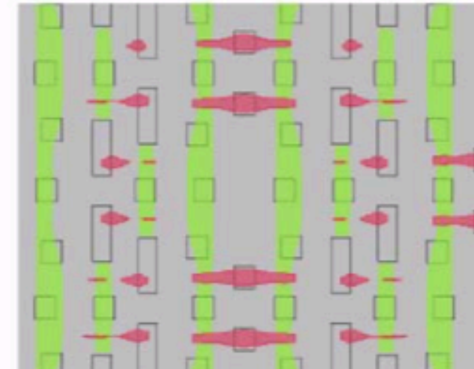
Visible light



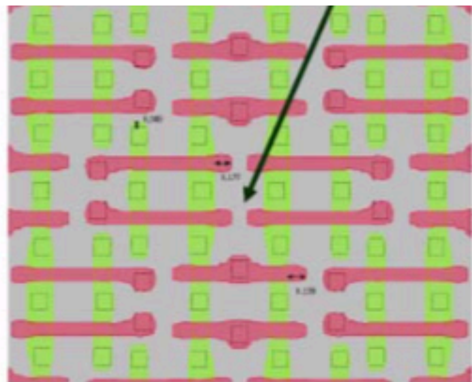
Lithography (3)

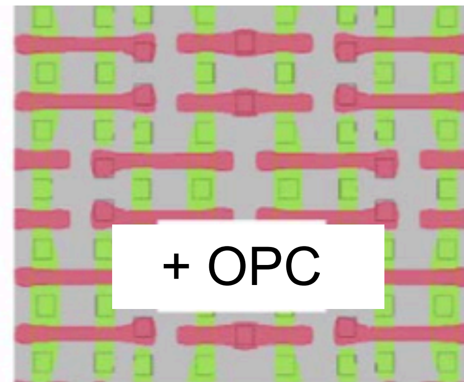


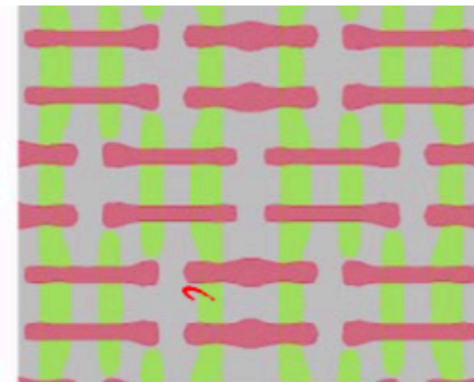




120 nm tech 90nm 65nm

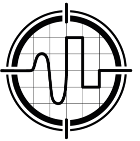






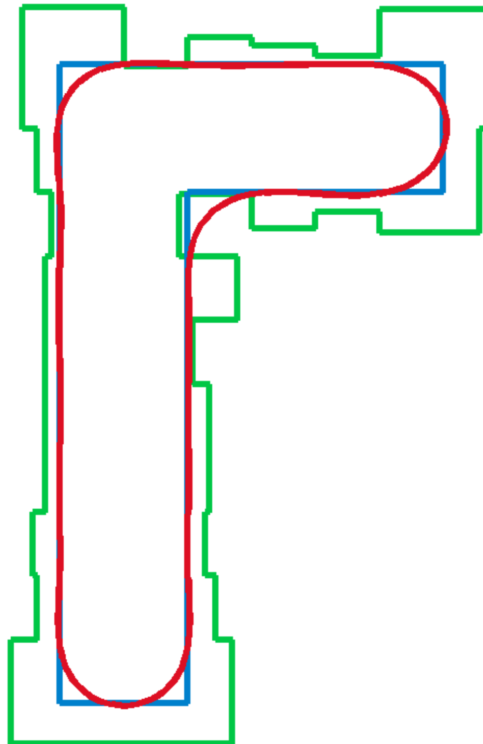
120 nm tech 90nm 65nm

Technology

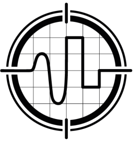


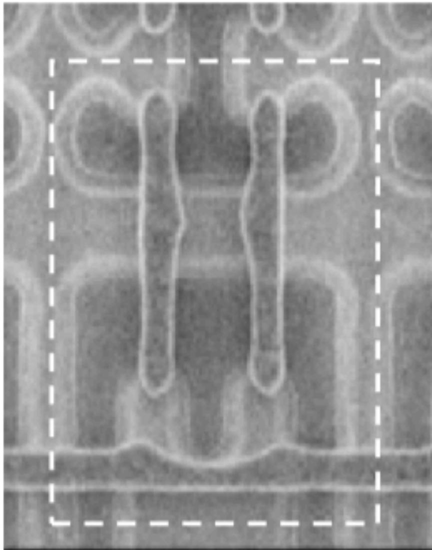
Lithography (4)

- Optical Proximity Correction Techniques (Computational Lithography)

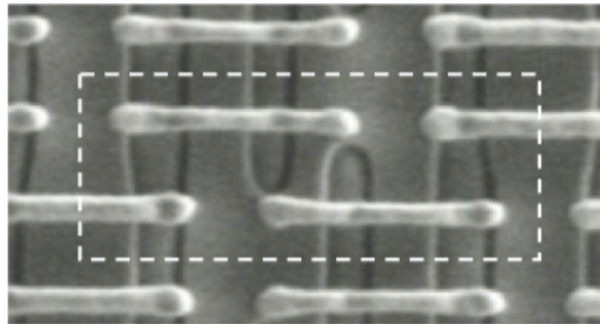


Lithography (5)

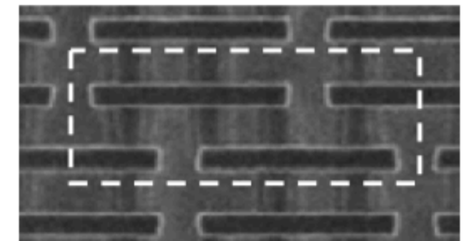




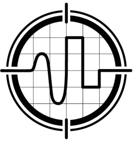
90nm – TALL
1.0 μm²



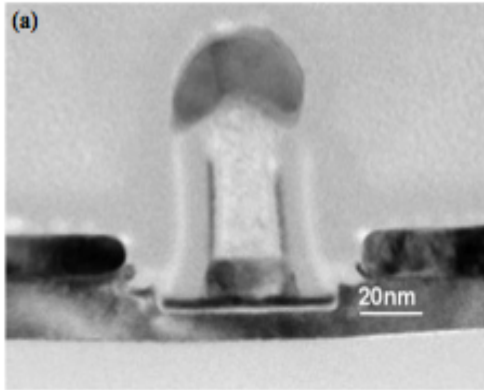
65nm – WIDE - 0.57 μm²



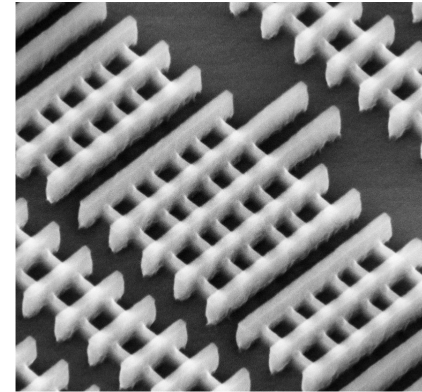
45nm – WIDE
w/ patterning
enhancement 0.346 μm²



Some advanced devices

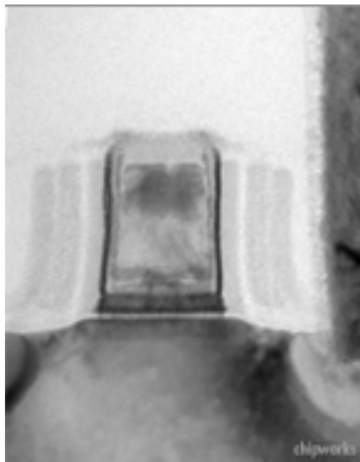


20 nm FDSOI from ST

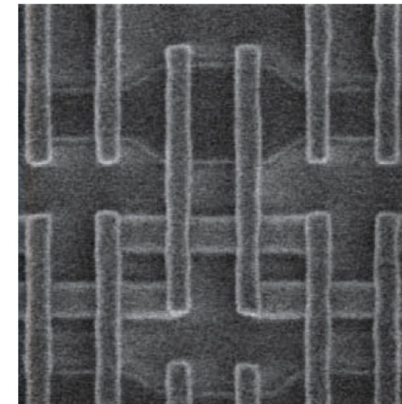


22 nm TriGate from Intel

Various sources

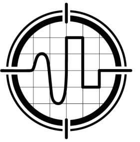


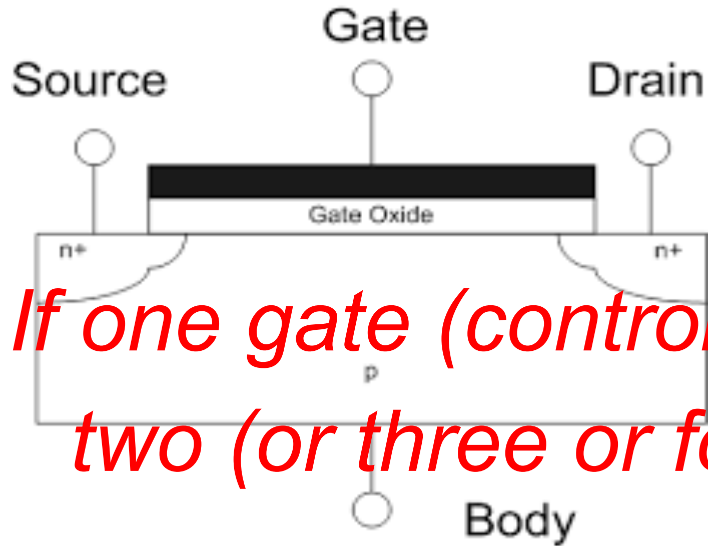
28 nm planar from TSMC



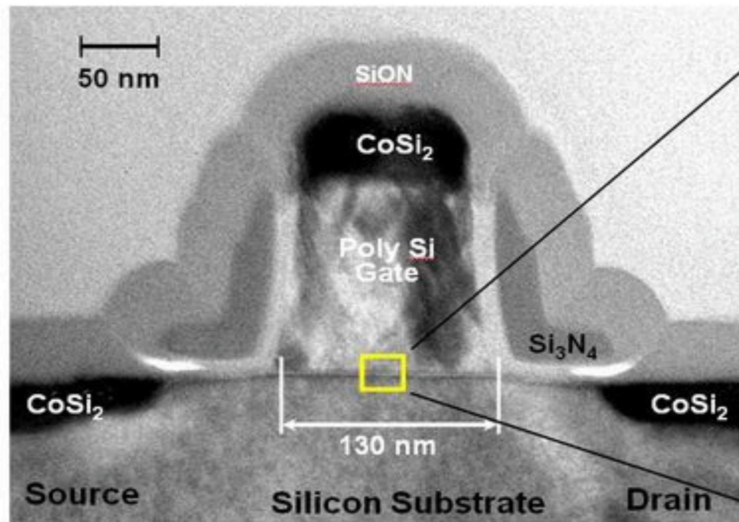
32 nm SOI from IBM

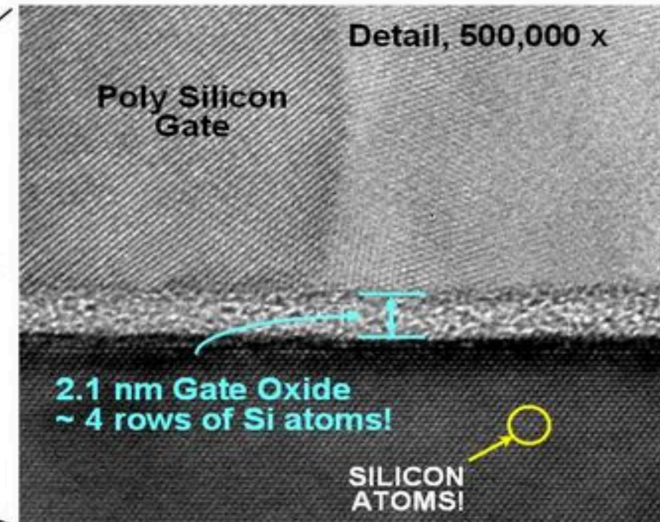
Multi-gate devices





If one gate (controlling surface) is good, two (or three or four) are even better





Toshiba 1983

Solid-State Electronics Vol. 27, Nos. 8/9, pp. 827–828, 1984
Printed in Great Britain

0038-1101/84 $3.00 + .00
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CALCULATED THRESHOLD-VOLTAGE CHARACTERISTICS OF AN XMOS TRANSISTOR HAVING AN ADDITIONAL BOTTOM GATE

(*Received* 30 *May* 1983; *in revised form* 24 *August* 1983)

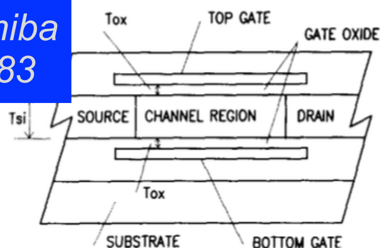


Fig. 1. Schematic cross-sectional structure of an XMOS transistor having an additional bottom gate which is symmetrically placed to a top gate with a channel region between them. "X" originates from Greek capital letter of xi as this structure resembles its shape.

Electronic Device Division,
Electrotechnical Laboratory,
Sakura-mura,
Ibaraki, 305,
Japan

T. Sekigawa and
Y. Hayashi

Hitachi 1989

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 38, NO. 6, JUNE 1991 1419

Impact of the Vertical SOI "DELTA" Structure on Planar Device Technology

Digh Hisamoto, *Member, IEEE*, Toru Kaga, *Member, IEEE*, and Eiji Takeda, *Senior Member, IEEE*

***Abstract*—A fully depleted lean channel transistor (DELTA) with its gate incorporated into a new vertical ultra-thin SOI structure is presented. In the deep-submicrometer region, selective oxidation produces and isolates an ultra-thin SOI MOSFET that has high crystalline quality, as good as that of conventional bulk single-crystal devices. Experiments and three-dimensional simulations have shown that this new gate structure has effective channel control, and that the vertical ultra-thin SOI structure provides superior device characteristics: reduction in short-channel effects, minimized subthreshold swing, and high transconductance.**

is required. Moreover, it is evident that these structures are difficult to contact to the substrate, and thus suffer from a substrate floating effect.

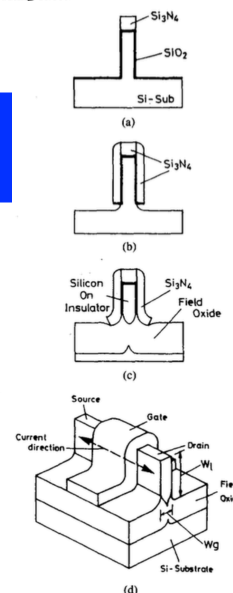


Fig. 1. (a)–(c) Process flow of selective oxidation. (d) Schematic cross section of DELTA.

Berkely 2000

2320 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 47, NO. 12, DECEMBER 2000

FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm

Digh Hisamoto, *Member, IEEE*, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, *Member, IEEE*, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, *Fellow, IEEE*, and Chenming Hu, *Fellow, IEEE*

***Abstract*—MOSFETs with gate length down to 17 nm are reported. To suppress the short channel effect, a novel self-aligned double-gate MOSFET, FinFET, is proposed. By using boron-doped $Si_{0.4}Ge_{0.6}$ as a gate material, the desired threshold voltage was achieved for the ultrathin body device. The quasiplanar nature of this new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.**

***Index Terms*—Fully depleted SOI, MOSFET, poly SiGe, short-channel effect.**

I. Introduction

To develop sub-50-nm MOSFETs, the double-gate structure has been widely studied. This is because

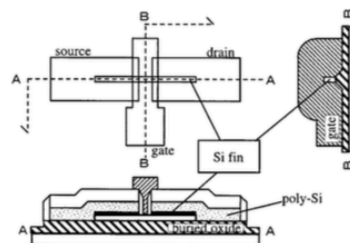
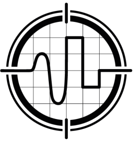


Fig. 1. FinFET typical layout and schematic cross sectional structures.

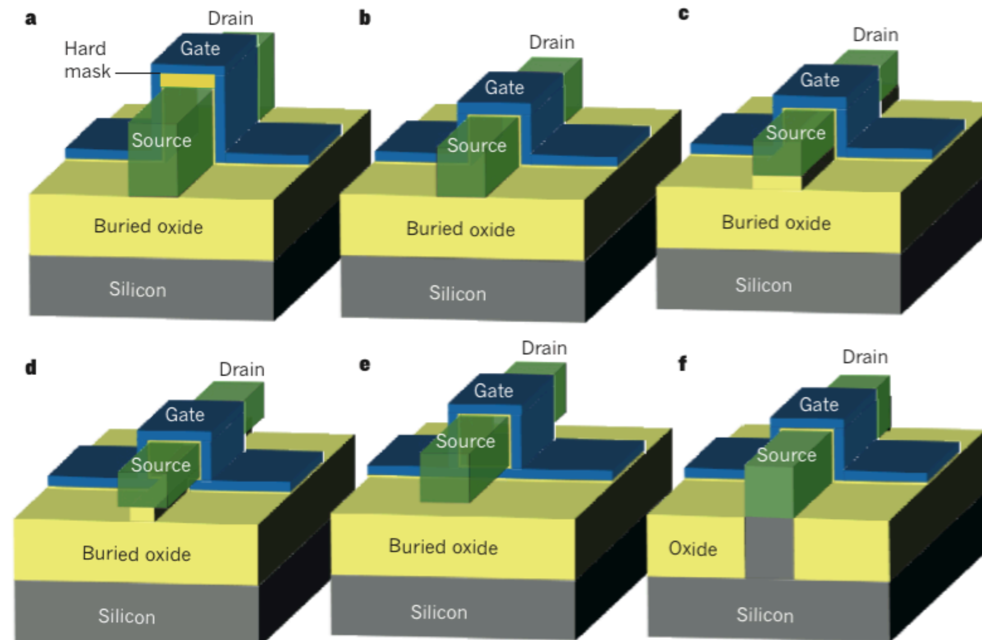
IBM 1994

Figure 1: Schematic views of the double-gate SOI MOSFET's.

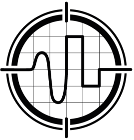


Multi-gate devices

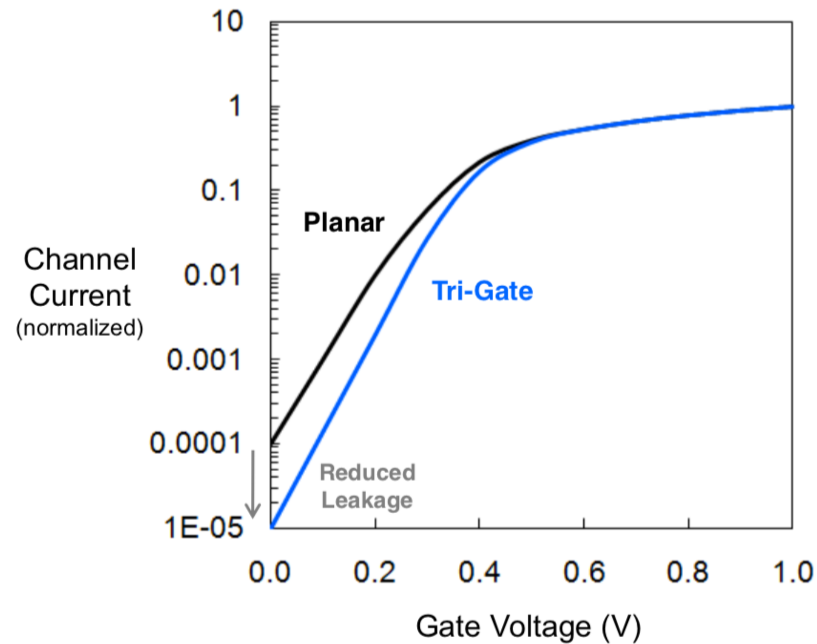
- Intel: Tri-gate
- TSMC, GF, Samsung: Finfets



from: Ferain, "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors ",

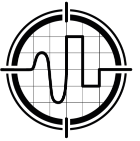


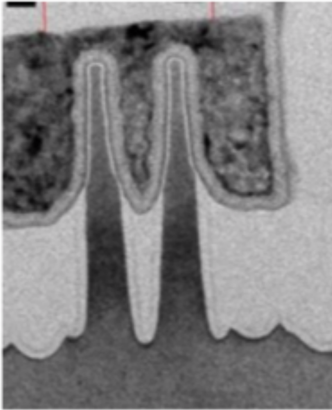
Subthreshold slope improvement

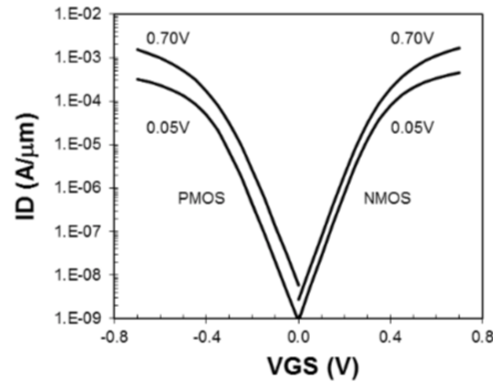


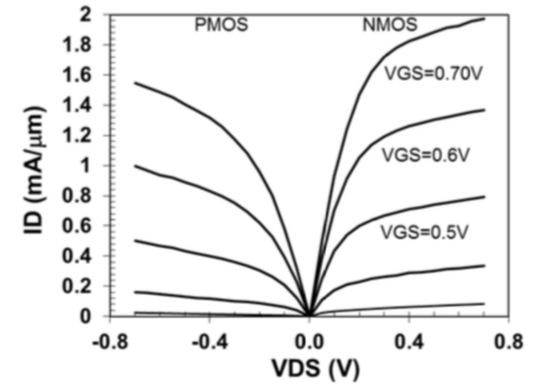
from: M. Bohr (Intel) , Intel's Revolutionary 22 nm Transistor Technology, May 2011

10 nm Finfet



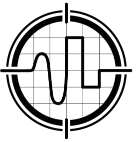




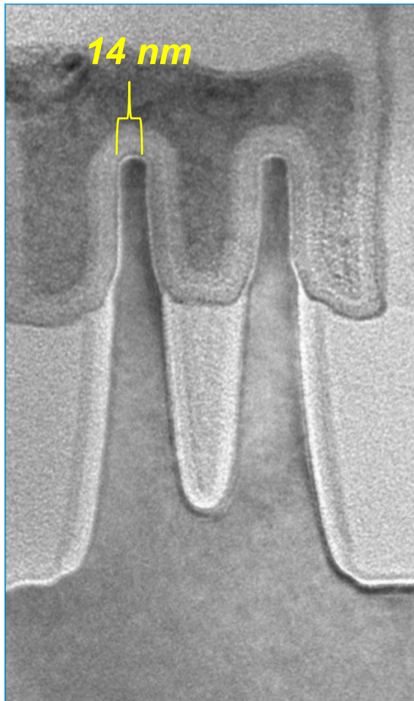


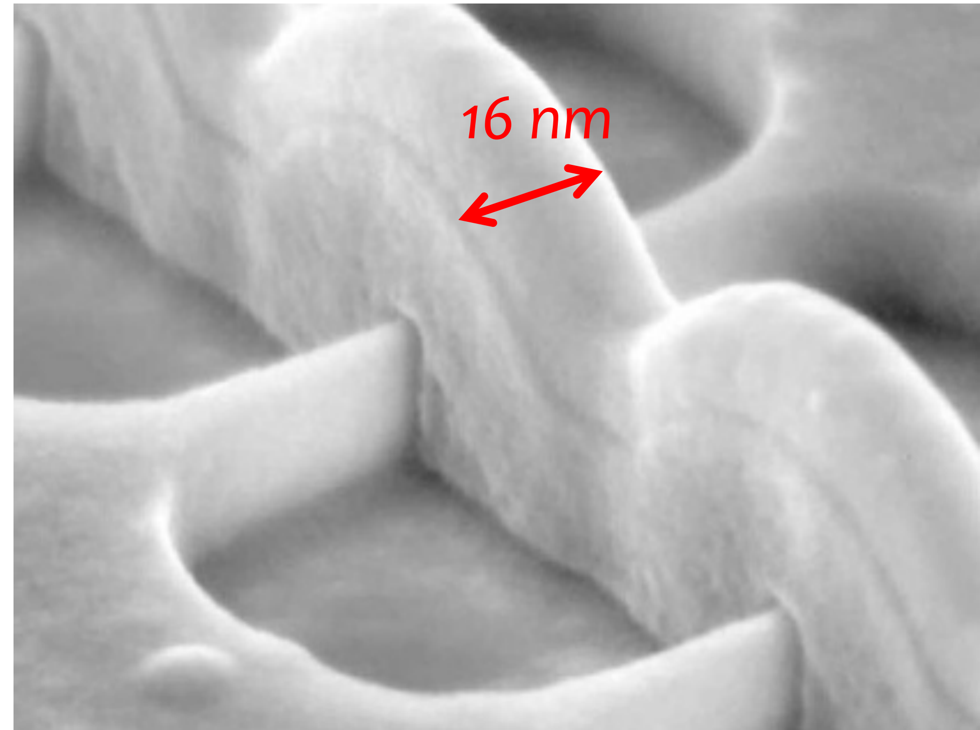
from: A. Auth (Intel), A 10nm High Performance and Low Power CMOS Technology…, IEDM 2017

State of the Art examples: FINFETs



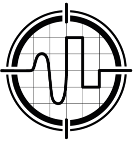
Source: Intel





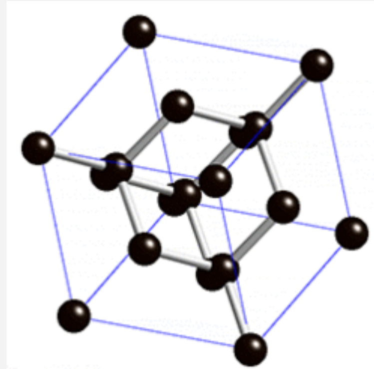
Source: TSMC

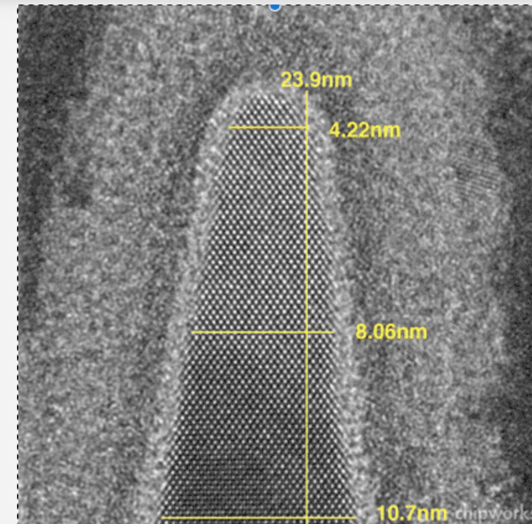
Typical FinFET dimensions

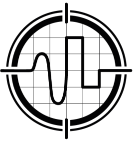


From the ITRS 2011 report

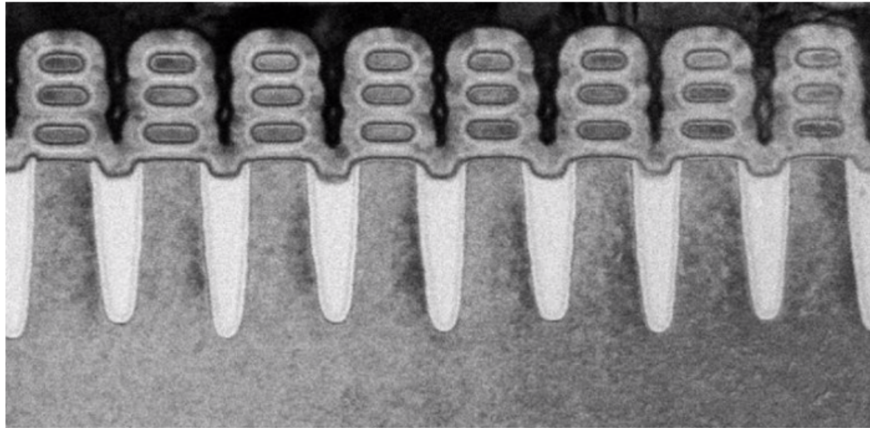
Year of Production	2013	2015	2017	2019	2021	2023	2025	2028
FinFET Fin Width (new) (nm)	7.6	7.2	6.8	6.4	6.1	5.7	5.4	5.0

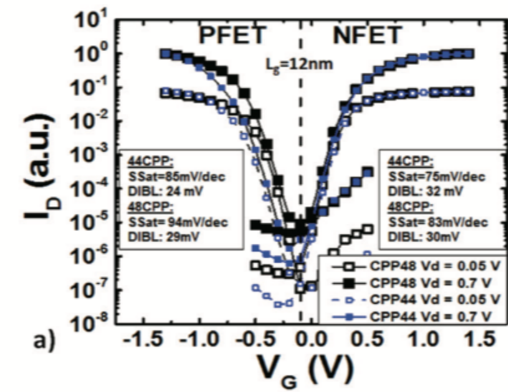




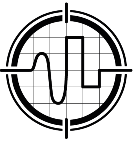


FINFET++ = GateAllAround (GAA)



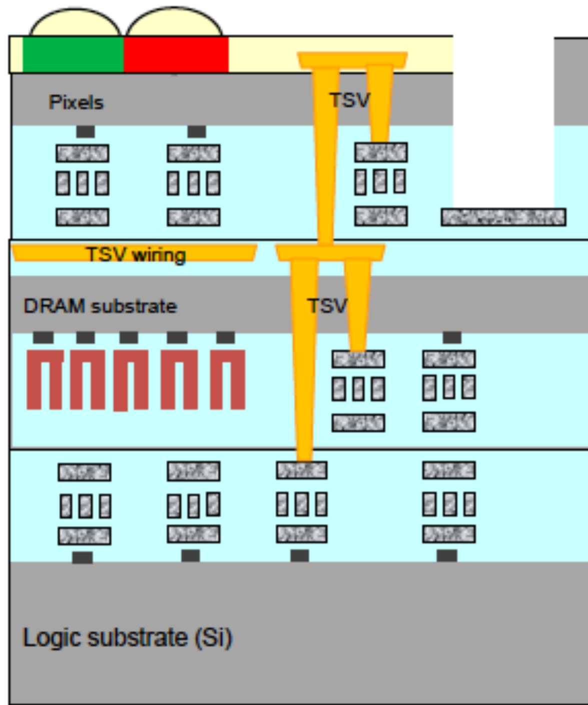


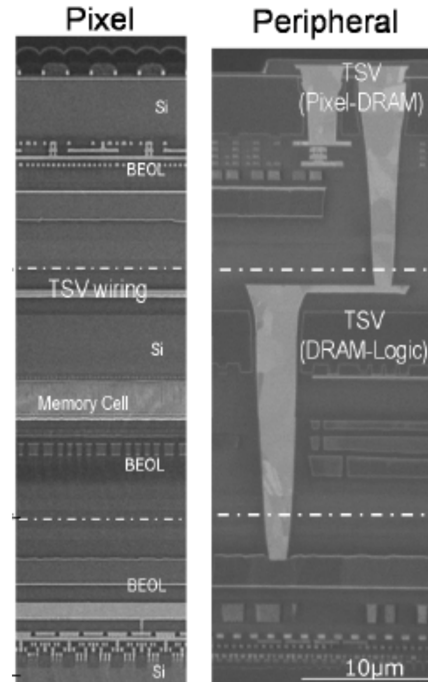
From N. Loubet – IBM –
Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET – VLSI Symp 2017



3D technology

from: H. Tsugawa et al., - Somy - Pixel/DRAM/logic 3-layer stacked CMOS imagesensor technology - IEDM 2017



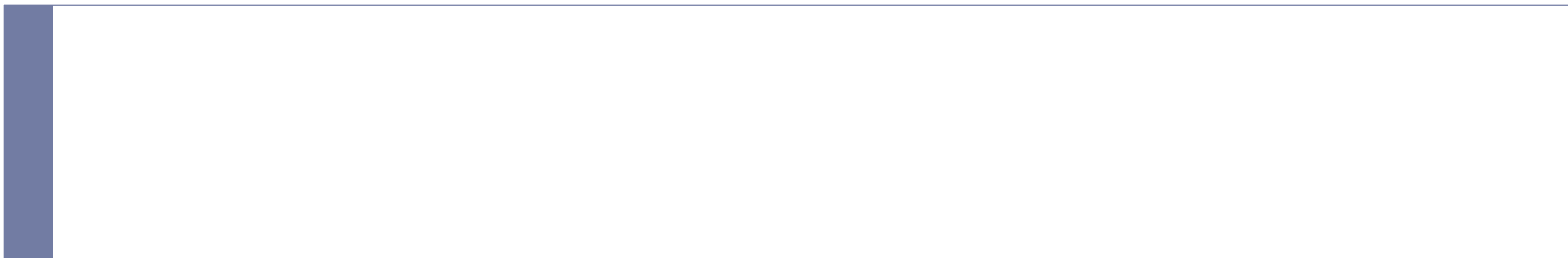


3 um

90 nm sensor tech

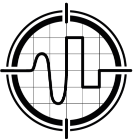
30 nm DRAM tech

40 nm logic tech



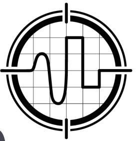
How to consume less energy in computation

Less energy per computation



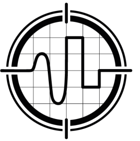
- Power consumption in digital circuits is determined by three factors:
  1. The energy necessary to charge/discharge the input of the next level of logic and the interconnecting wire
  2. The energy wasted by the switching device because of simultaneous conductance of the NMOS and PMOS devices during a transition
  3. The energy wasted by leakage currents through the transistors (the switches are unfortunately not “*ideal*”) even in static conditions

Power consumption in (digital) chips



$$P = \frac{1}{2} C\, V_{dd}^2\, \alpha\, f + I_{leak} V_{dd} + \Delta\tau_{sw}\, I_{sc} V_{dd}$$

V_{dd}: *supply voltage*
α: *activity factor*
C: *load capacitance*
f: *switching frequency*
I_{leak}: *leakage current*
I_{sc}: *short circuit current*
$\Delta\tau_{sw}$: *fraction of time in sc mode*

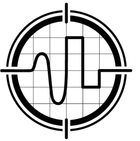


Improving in energy saving

- Make devices smaller:
  - C decreases
    - … but up to a point as the interconnect C becomes rapidly dominant and actually starts to increase
  - V_{dd} decreases
    - … but also up to a point, as threshold voltage behavior is limited by intrinsic physics and not by technology

  - Something drastic is required to save energy!

Any better transistor?

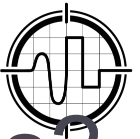


Today's devices make transitions around their threshold voltages which are determined by some fundamental physics related to the Boltzmann constant. Such devices require at least an input voltage change of 60 mV to increase their current by a factor of 10.

Devices with "very steep" transition regions between the OFF and the ON states are being researched, among these:

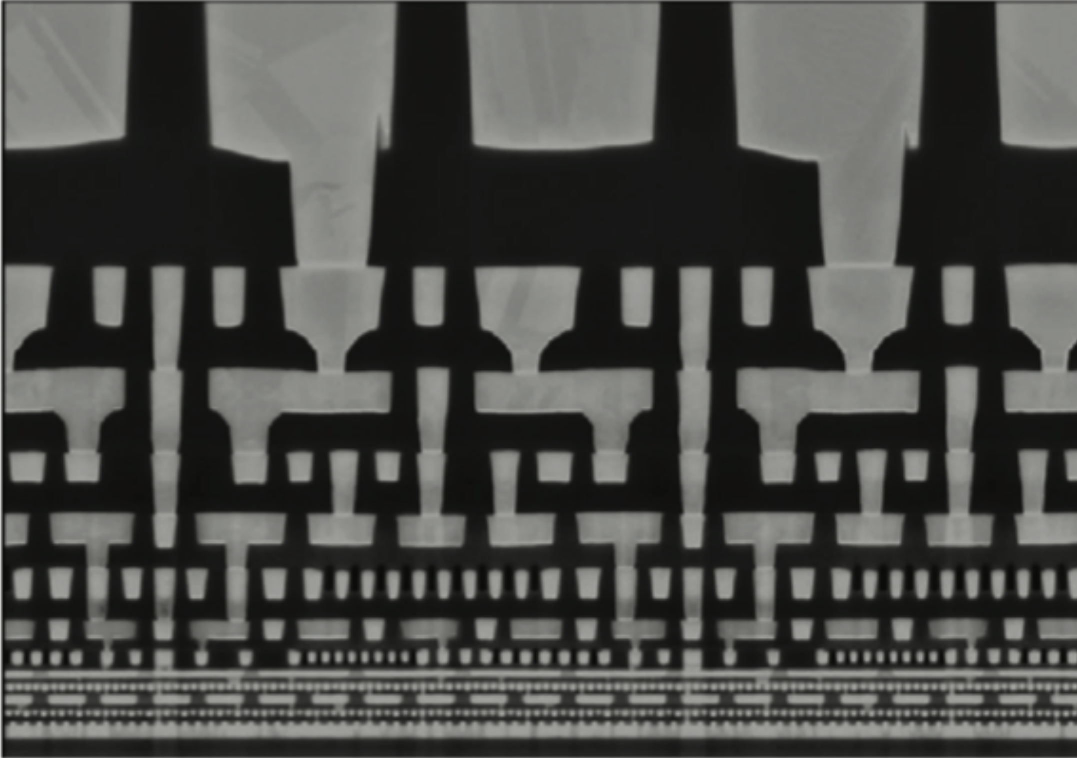
1. "Ferroelectric" (negative capacitance) transistors
2. Tunnel transistors
3. …

If available in the coming years these would lead to supply voltages in the 100-200 mV region and a power saving of about one order of magnitude



Who is more important: Transistors or wires?

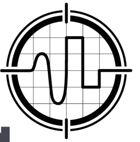
from K. Fischer – Intel - Low-k Interconnect Stack with multiple-layer gap…, IITC Conf. 2015



Metal	Pitch [nm]	Metal tickn.[nm]
0	56	40
1	81	42
2	73	40
3	76	37
4	80	75
..		
11	1000	1000

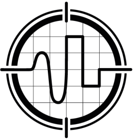
A 14 nm FINFET process metal stack

Wire resistance in “classical” scaling



Resistance for Classic M1 scaling

Tech [nm] (approx.)	Relative Resistance (approx.)
14	8.6
32	3.4
45	1.6
65	1.0



Ultra-scaled metals

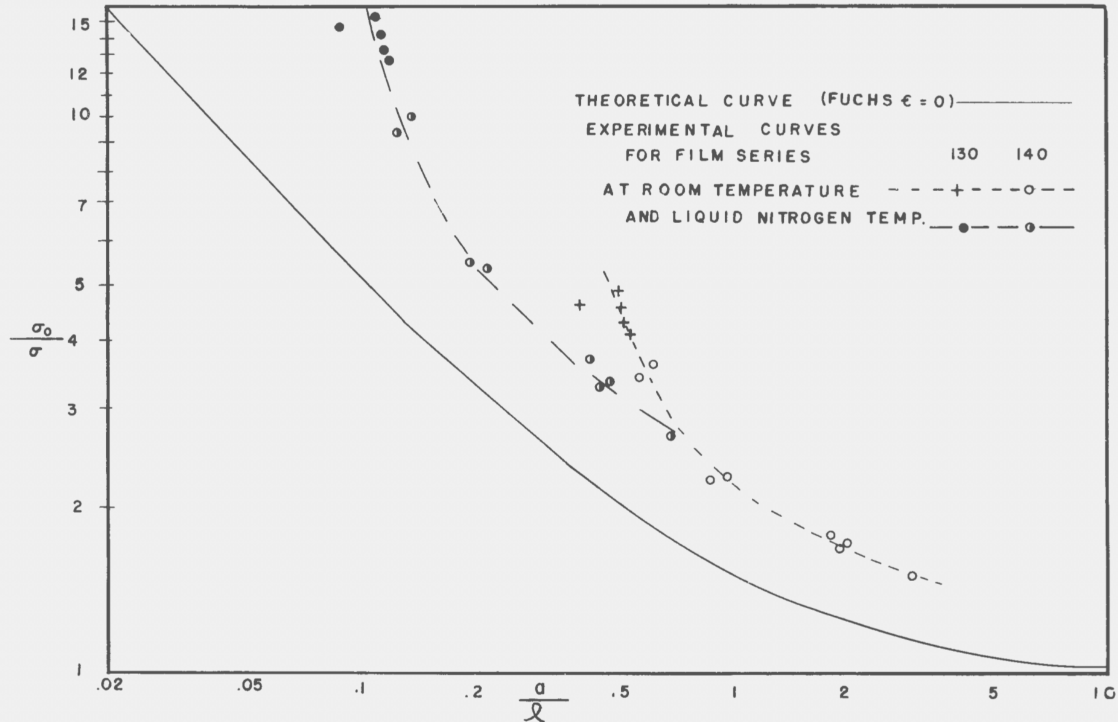


FIG. I. ELECTRICAL CONDUCTIVITY OF THIN SILVER FILMS.

UNITED STATES ATOMIC ENERGY COMMISSION

ISC-215

ELECTRICAL PROPERTIES OF THIN METALLIC FILMS

By
D. B. Barker
W. C. Caldwell

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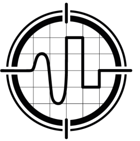
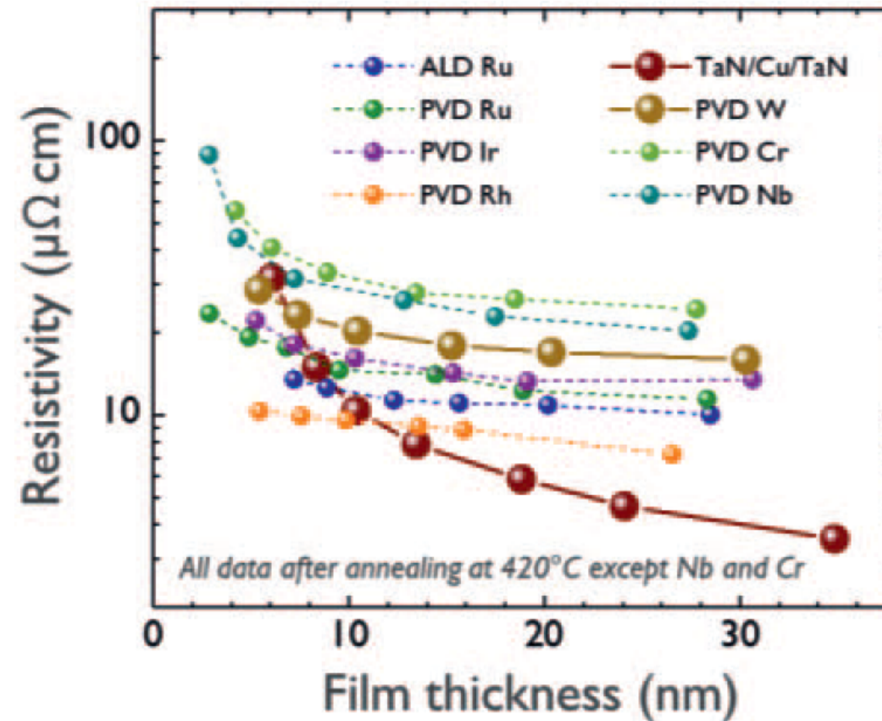
March 20, 1952

Ames Laboratory

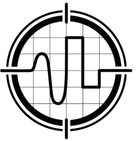


Ultra-scaled metals (2)



from K. Croes, IEDM 2018

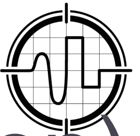
Summary on technologies



- Moore's Law worked for more than 50 years with spectacular results
- But fundamental limitations are being encountered in many areas
  - Thinness of materials
    - Leakage currents
    - Resistances (and Line Edge Roughness)
    - Complexity of fabrication
    - Physics:
      - Random dopants distribution
      - …
    - …
  - Cost of fabrication
- Another factor of 10 possible with 'brute force scaling'?
  - Hard to bet, but most likely not possible
- Fundamental research is nevertheless very active to develop new materials that allow switches to be built through new phenomena

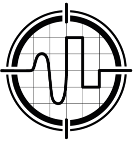
Basics on Radiation effects in CMOS

A "Bonus" or a "Miracle" ?



Ionizing particles in oxides (simple version)

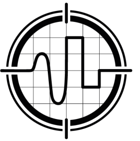
Illustration from F. Faccio: TWEPP Tutorial 2007
not to scale!

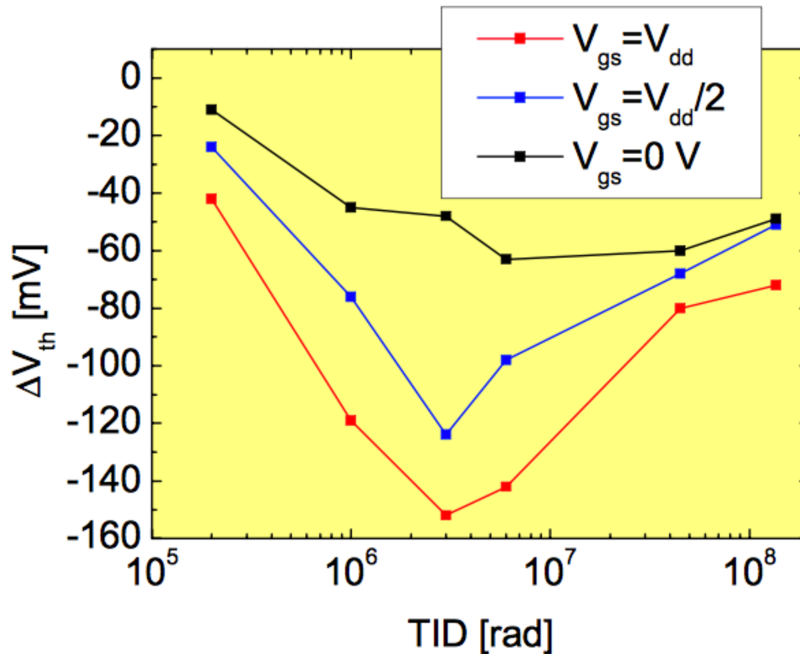


Consequences of trapped charge

- Charges on gate oxides:
  - Threshold Voltage of NMOS becomes lower
    - NMOS Devices are more difficult (or impossible) to turn off
    - Threshold Voltage shift (and therefore matching between devices) depends on biasing conditions!
    - Leakage current increases
  - Threshold Voltage of PMOS becomes higher
    - Devices are more difficult to turn on
    - Leakage decreases but drive current decreases too
    - Threshold Voltage shift (and therefore matching between devices) depends on biasing conditions!
- Charges in field oxides
  - Field transistors:
    - If field oxide gets heavily charged parasitic transistors can be formed “between” otherwise isolated diffusion areas (i.e. normally isolated regions such as sources and drains of different devices) causing very significant problems.

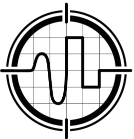
Bias dependence of ΔV_{th}





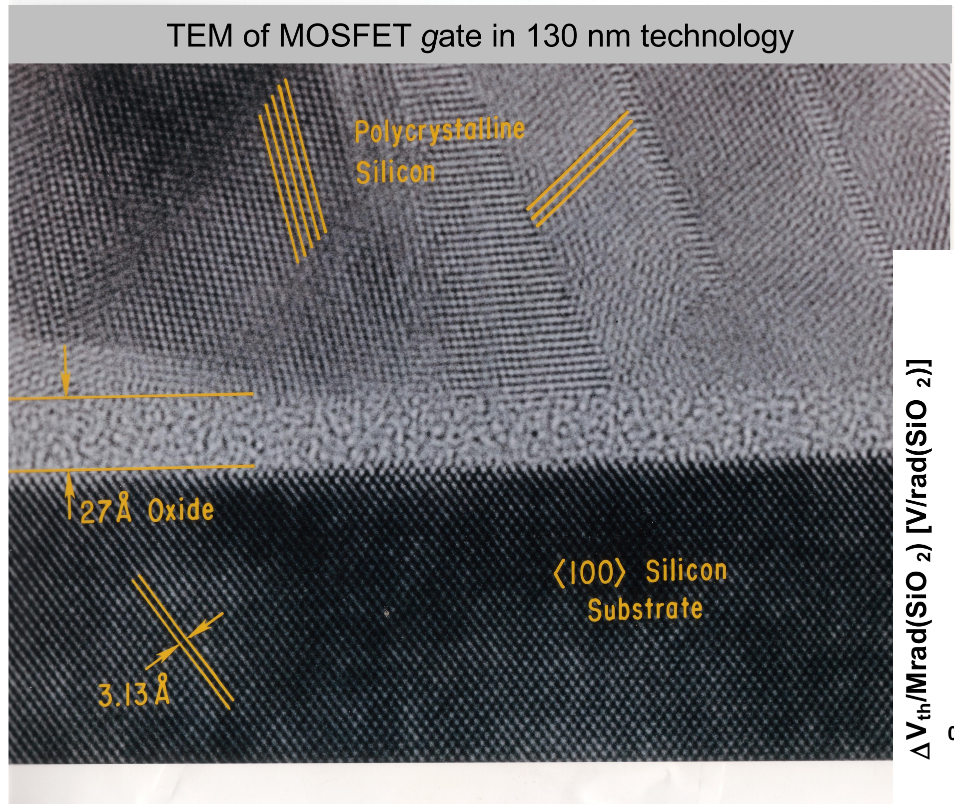
Minimum-Size NMOSFETs

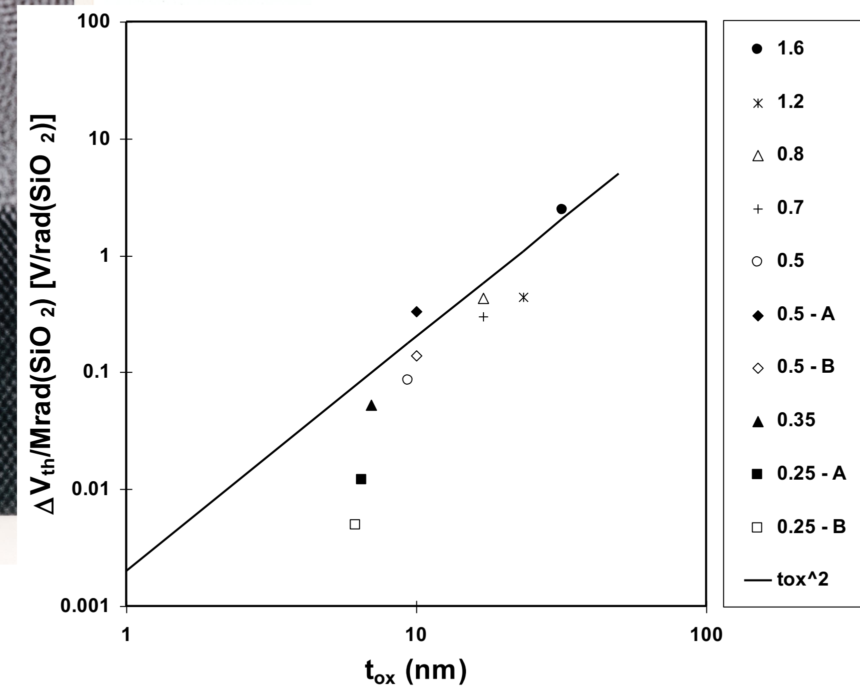
- Worst condition:
  - $V_{gs} = V_{dd}$
  - $\Delta V_{th,max}$=-150 mV
- Intermediate condition
  - $V_{gs} = V_{dd}/2$
  - $\Delta V_{th.max}$=-120 mV
- Best condition
  - V_{gs} = 0 V
  - $\Delta V_{th,max}$=-60mV



Charge trapped in gate oxides: DSM helps!

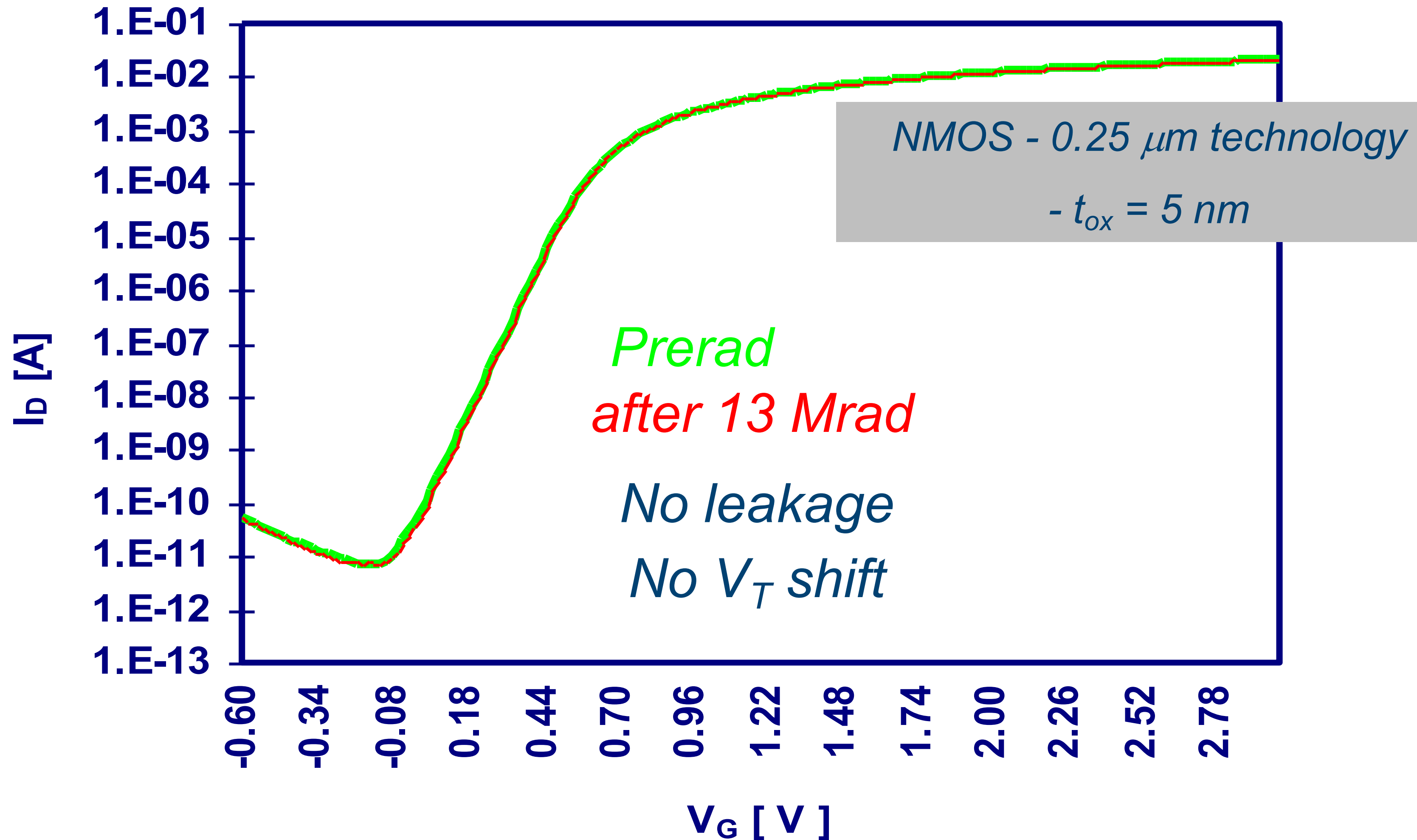
TEM of MOSFET *gate* in 130 nm technology



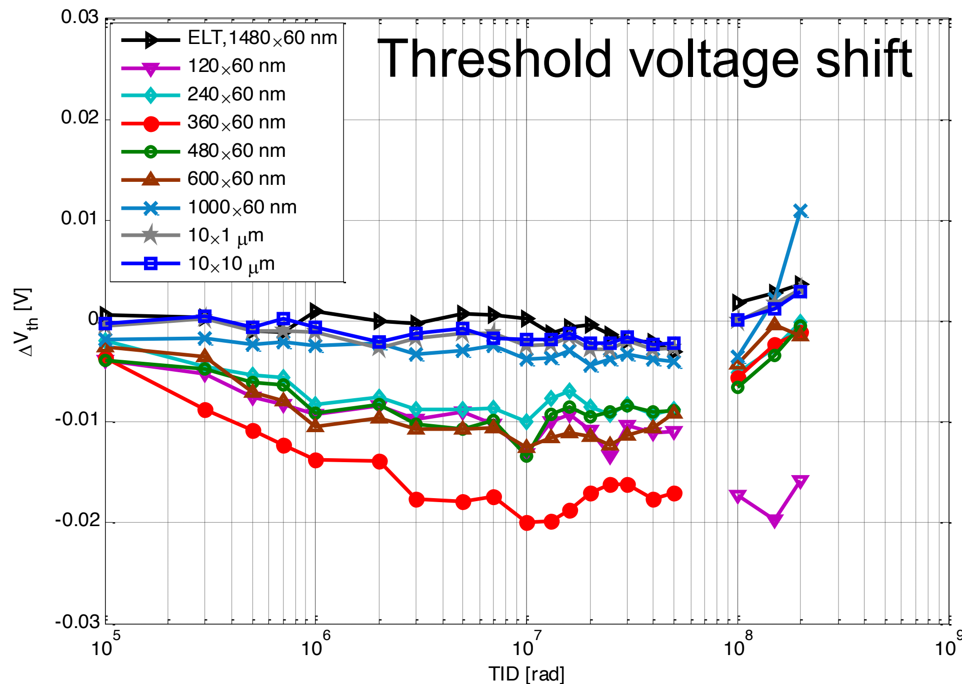


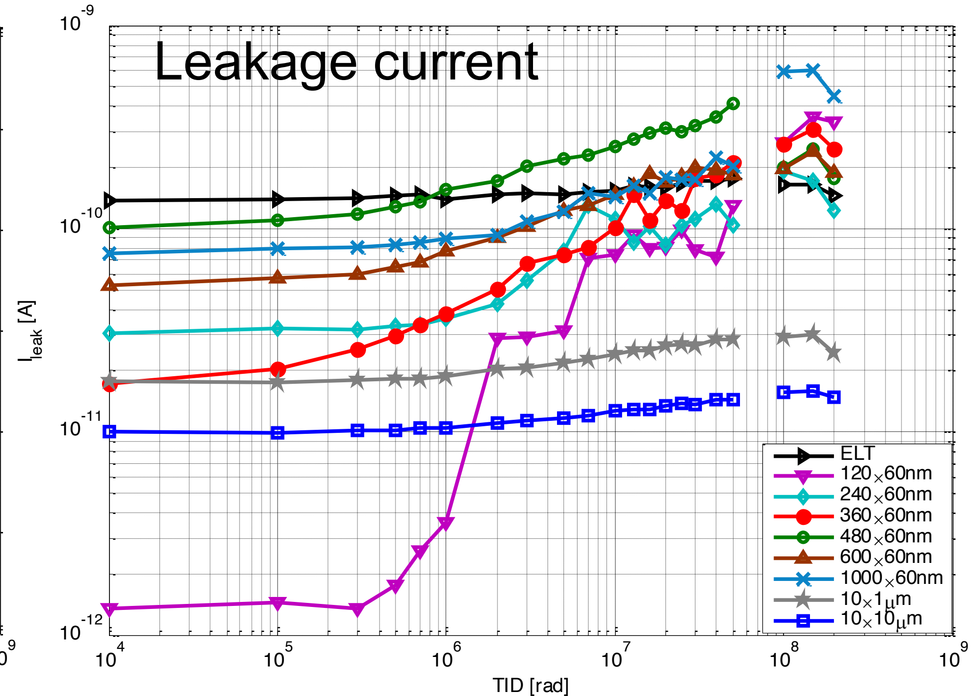
N.S. Saks et al., IEEE TNS, Dec. 1984 and Dec. 1986

More modern tech, with ELT



Irradiation of 65nm technology

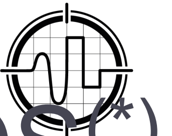




- Up to ~20mV shift for 200 Mrad
  - Some rebound effect visible for narrow devices
  - in 130nm: was 150mV
- At high doses Vth shift is positive for wide devices, negative for narrow devices
  - STI edge oxide traps considerable charge (RINCE)
- Subtreshold slope does not change significantly

- Less than 10× increase in leakage for wide devices (W > 360nm)
- Narrow devices have up to 2.5 orders of magnitude increase
- In 130nm:
  - All devices are peaking at ~100nA
  - Narrow devices increase leakage by 3 orders of magnitude
  - I_{leak} is ~1nA @136 Mrad

from: S. Bonacini, P. Valerio, CERN, TWEPP2011

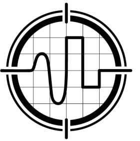


Short summary on rad effects in CMOS(*)

- "*Fortunately*" commercial CMOS introduced "thin-oxide" gates at the time when LHC instruments were being designed for the 1-100 MRad regime.
- If the CMOS development had been late by - say - 10 years, none knows what would have happened to LHC experiments.

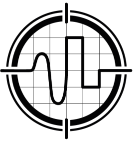
(*) Valid up to ~100 MRad, beyond this point matters become again complicated

Lesson learned



If you are working on a project for post-LHC HEP (and your experiment is very ambitious with radiation levels), beware of radiation effects, as another lucky coincidence may not be on the books!

Conclusions



- Powerful technologies and tools are here today, you have to invent how to use them to create new instruments.
  - Introduction of local computation (i.e. intelligence) needs two essential ingredients:
    - Low power microelectronics engineering (i.e. a commercial technology)
    - and imagination (i.e. YOU)
- If you are at this school, you have already developed a sense of gratification and pleasure by ”creating”
  - new systems (for system designers)
  - programs (if you mainly use “computers”)
  - new logic functionality (FPGA designers).
- *ASIC design can add a new dimension of “creativity” to your bag of tools.*