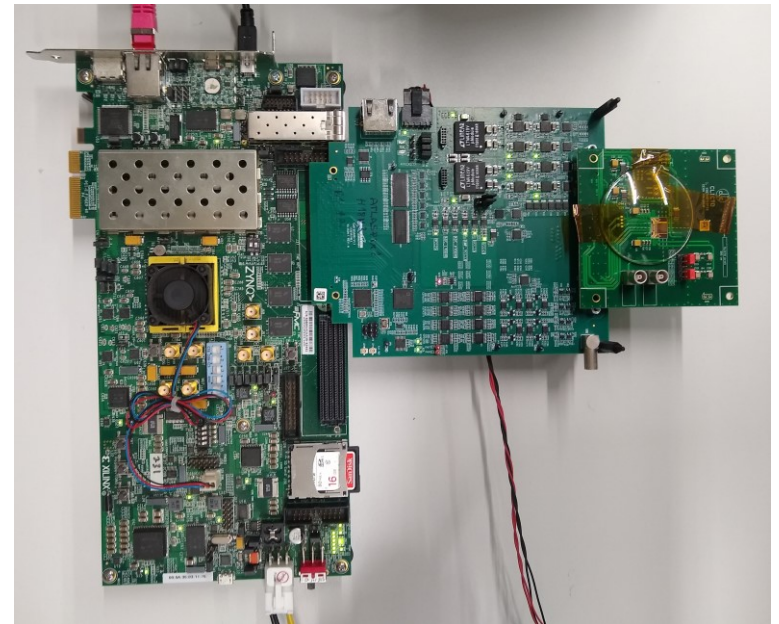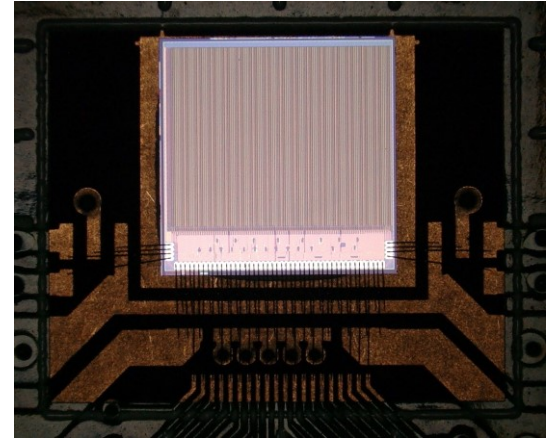# First results from CLICTD lab measurements

CERN, August 2nd 2019

I. Kremastiotis
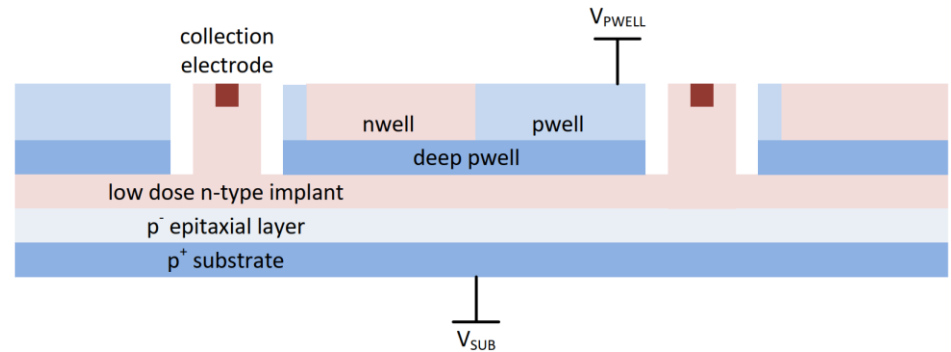
Introduction

- CLICTD chips received: 02 July 2019

- Matrix size: 16 x 128 pixels (4.8 x 3.84 mm^2)

- Chip size: 5 x 5 mm^2

- Wire-bonding:
  - 2 samples from "Rev. A" – continuous N-implant
  - 1 sample from "Rev. B" – gap in N-implant
  - Wire-bonded samples received: 04 July 2019

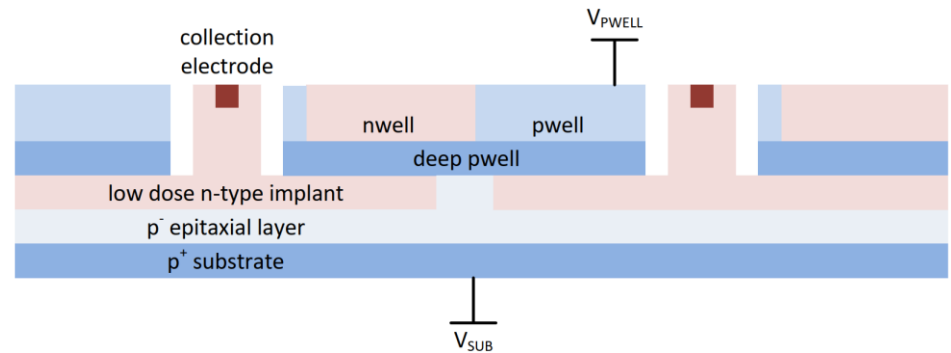- Communication established using CaRIBOu

I-V characteristics
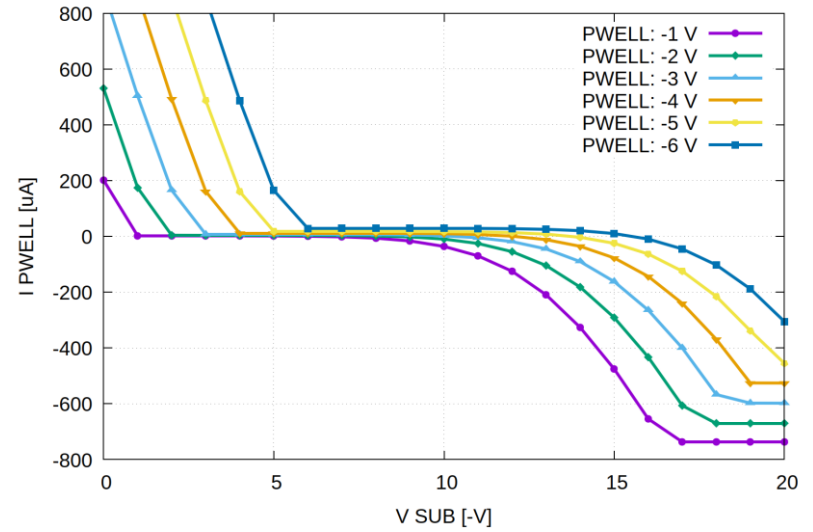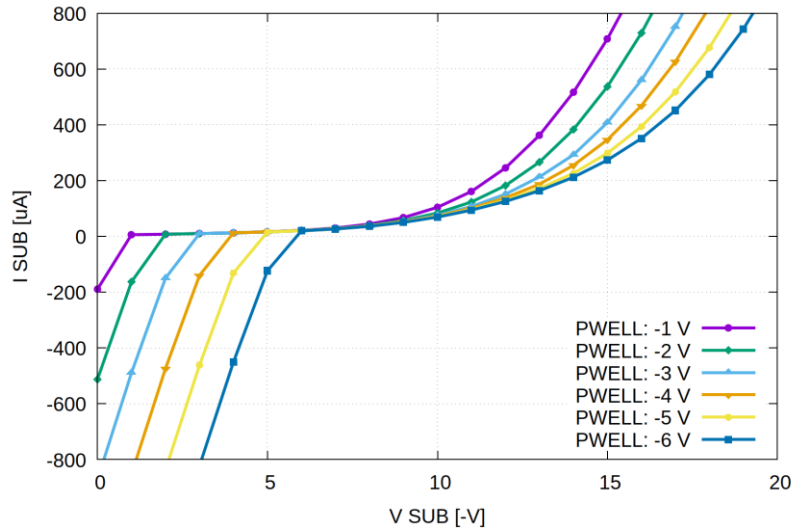
- 1st process split: continuous N-layer

- 2nd process split: gap in N-layer
  (only in the long dimension)

- Sensor I-V measured by scanning the substrate bias, for different values of the deep P-well bias
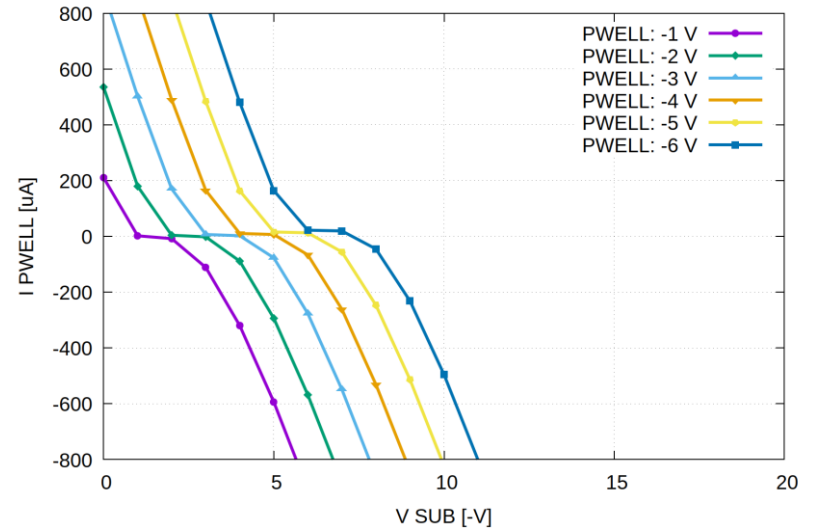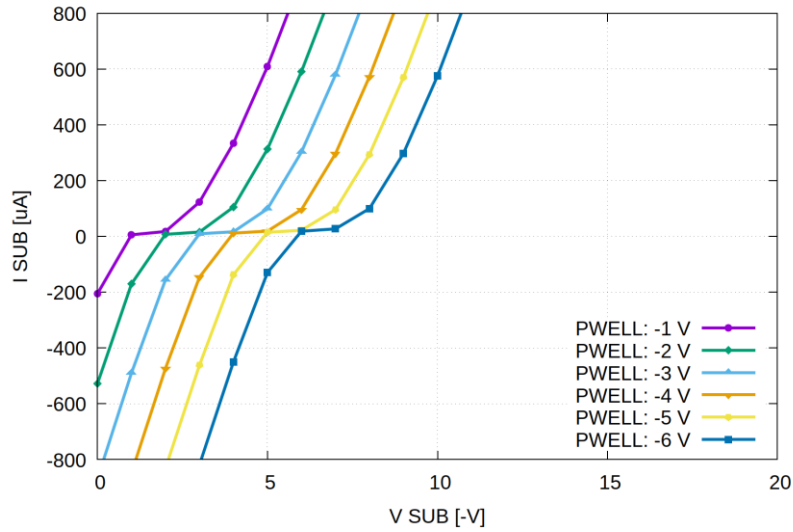- Leakage current was measured at both nodes: SUB and PWELL

I-V characteristics

- 1st process split: continuous N-layer

I-V characteristics

- 2nd process split: gap in N-layer

Slow control

- Slow control performs as expected
  - Reset issues, probably due to the incorrect clock frequency
  - After successful reset, all registers have their expected values.
  - Successful read / write operation to all registers

| Register	I^2C Address	Length	Reset value
globalConfig	0x00	8	0x01
internalStrobes	0x01	8	0x00
externalDACSel	0x02	8	0x00
monitorDACSel	0x03	8	0x00
matrixConfig	0x04	8	0x08
configCtrl	0x05	8	0x00
configData	0x06	16	0x0000
readoutCtrl	0x08	8	0x00
tpulseCtrl	0x0A	16	0xFFFF
VBIASResetTransistor	0x10	8	0x03
VRESET	0x11	8	0x68
VBIASLevelShift	0x12	6	0x09
VANALOG1	0x13	9	0x000
VANALOG2	0x15	8	0x00
VBIASPREAMPN	0x16	6	0x05
VNCASC	0x17	8	0x5B
VPCASC	0x18	8	0x82
VFBK	0x19	8	0x47
VBIASIKRUM	0x1A	6	0x04
VBIASDISCN	0x1B	6	0x08
VBIASDISCP	0x1C	6	0x09
VBIASDAC	0x1D	6	0x07
VTHRESHOLD	0x1E	9	0x09A
VNCASCCOMP	0x20	8	0x76
VBIASLevelShiftstby	0x21	6	0x01
VBIASPREAMPNstby	0x22	6	0x01
VBIASDISCNstby	0x23	6	0x01
VBIASDISCPstby	0x24	6	0x01
VBIASDACstby	0x25	6	0x01
VBIASSlowBuffer	0x26	8	0x0F
AdjustDACRange	0x27	8	0x03
VLVDSD	0x28	4	0x0F

DAC scans

- Current and voltage DACs were scanned, confirming that they operate as expected

- Example current DAC: preamplifier bias current
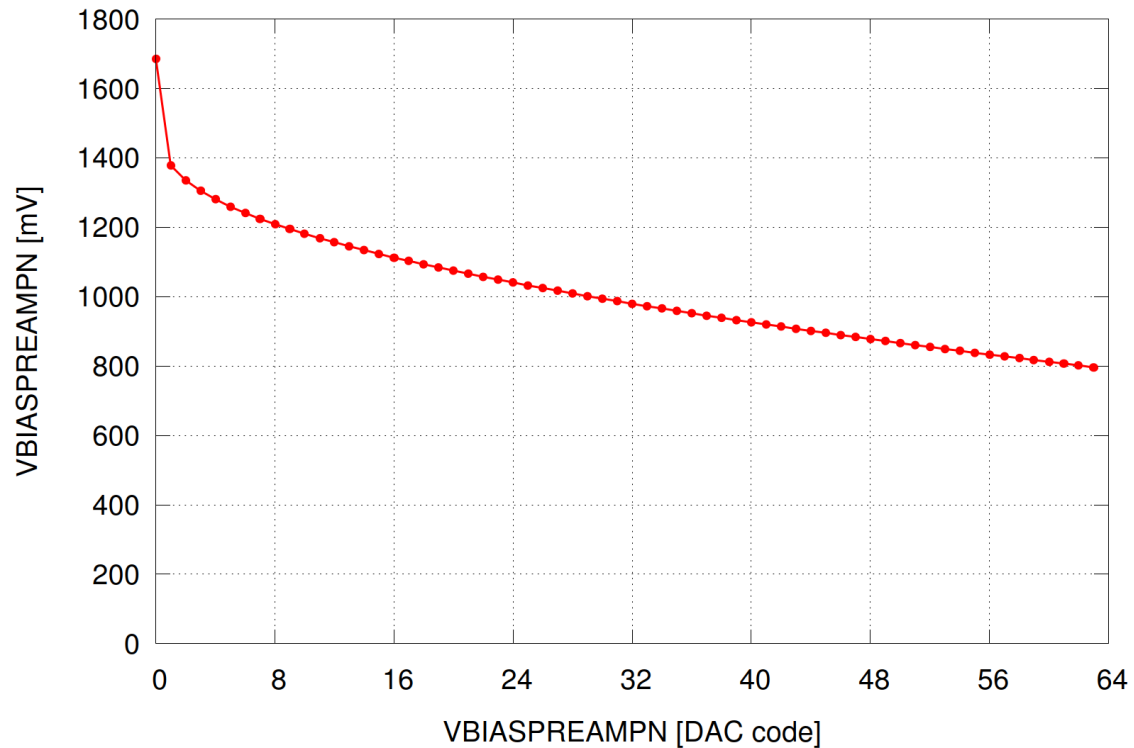
DAC scans

- Example voltage DAC: threshold voltage
- 'AdjustDACrange': register tuning the DAC range, by a set of current mirrors
- Threshold voltage scanned for different values of 'AdjustDACrange'
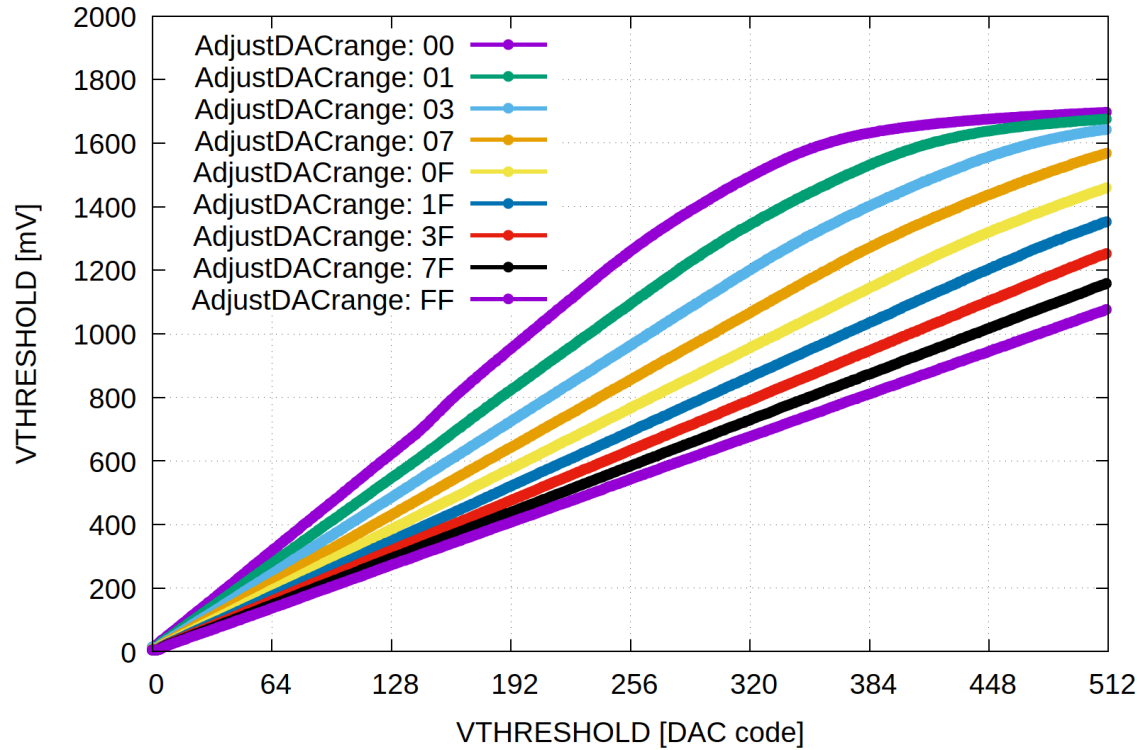
Power consumption

- After reset:
  - Analog power consumption: 40 mW (22 mA @ 1.8 V VDDA) for the full chip
  - After applying power pulsing: power reduced to 9 mW (5 mA)
    - Close to the ~8 mW expected for the analog periphery
  - Power consumption of the analog front-end is configurable by periphery DACs
    - Depends on the operating point
    - Can be further studied after matrix readout

  - Digital power consumption: 29 mW (16 mA @ 1.8 V VDDD) for the full chip
    - Expected:
      - 22 mW LVDS drivers (4 mA per LVDS driver, 1.8 V supply, 3 drivers in chip)
      - 5 mW LVDS receivers (1.5 mA per LVDS receiver, 1.8 V supply, 2 receivers in chip)
    - Dynamic power consumption from clock distribution not captured by the monitoring ADC (conversion time → 100's of µs)

Summary and next steps

- Summary:
  - Sensor I-V characteristics indicate that the sensor can be operated at its nominal bias
  - CLICTD chip periphery performs as expected
    - Slow control
    - DAC scans

- Next steps:
  - Firmware for readout in progress
  - Matrix configuration
  - Reading back configuration
  - Threshold scans
  - Measurements with radiation sources
  - Measurements with test pulses

Additional slides

I-V characteristics

- 1ˢᵗ process split: continuous N-layer (log scale)
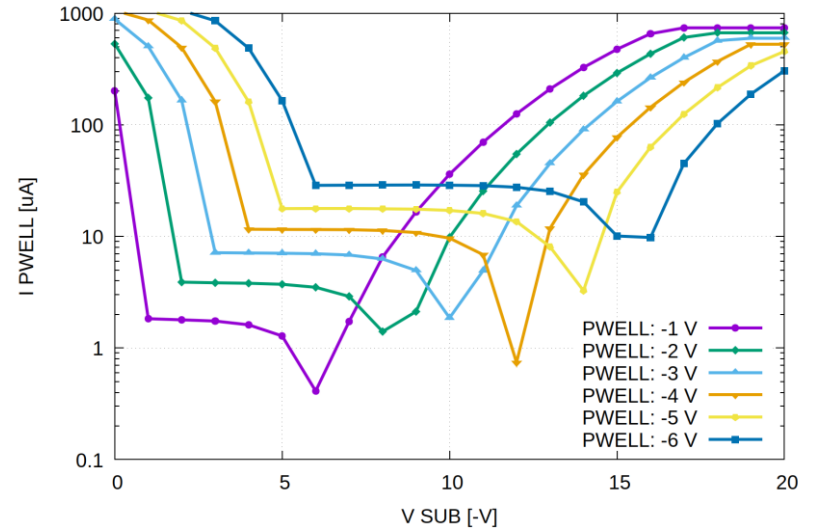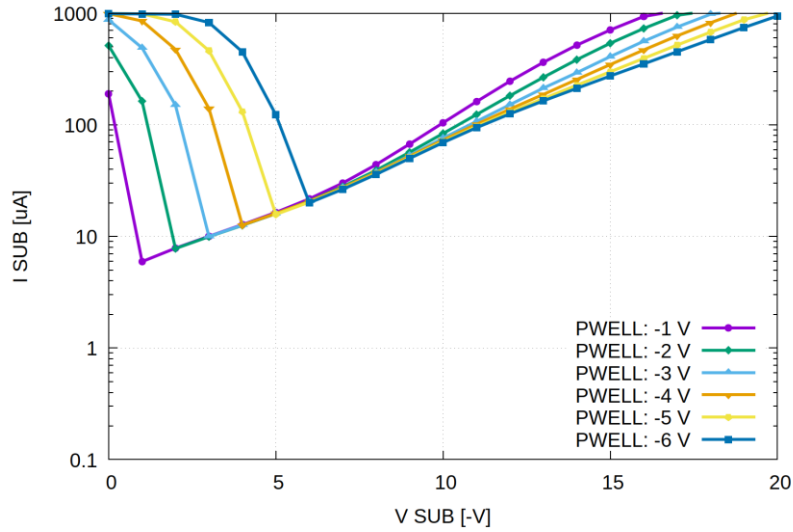
I-V characteristics

- 2nd process split: gap in N-layer (log scale)