Summer Student 2019 Project Report

#### CARIBOU DAQ: OS UPDATE AND SOC BOARD UPGRADE

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# INTRODUCTION TO CARIBOU

- CaRIBOu: versatile data acquisition system to facilitate pixel detector R&D.
- Based on Xilinx Zynq-7000 ZC706 Eval. Kit
- Runs (modified) Poky embedded Linux distro. by the Yocto Project.
  - Currently on version Rocko (2.4.4)
- Additional functionality through 'layers': meta-caribou
  - Linux tools and packages.
  - FPGA firmware.
  - Peary DAQ software.





## PART I: OS & SOFTWARE UPDATE

Motivation

• Poky version Rocko no longer supported.



Objectives

- Update Poky to version Thud (2.6.2, latest supported by Xilinx).
  - ...along with all associated layers (OpenEmbedded, Xilinx, Caribou).
- Refresh/fix kernel patches to suit any changes from Rocko to Thud.
- Test updated OS & patches with ATLASPix & CLICpix2 configuration.



## PROCESS: "BLIND" UPDATE

- Update to Thud and build the image without modifying anything else.
- Expected problems:
  - Kernel patches don't work  $\rightarrow$  kernel files were changed.
  - Peary doesn't work 
    → I2C header file removed/modified in previous Poky update.
- Unexpected problems:
  - prepare\_sd script fails → image boot directory structure changed, not enough sleep.



#### PROCESS: CHANGED FILES

- conf/machine/caribou-zynq7.conf
  - Boot image directory structure.
- [Peary] peary/interfaces/I2C/i2c.cpp
  - New (or rather, old) header file.
- Kernel patches redone on new kernel.
  - Usually they only differ in line number (i.e. other stuff were added or removed in the update).
  - More significant change: drivers/i2c/i2c-core.c split into /drivers/i2c/i2c-corebase.c and several other files.
- Add sleep (delay) action before & after SD card mounting/unmounting.



# VERIFICATION

- Verification using a standard ATLASPix setup.
  - Tests I2C functionality and data acquisition.
  - Initialization, configuration, and trial DAQ run.
- Verification using a standard CLICpix2 setup.
  - Tests both I2C and SPI functionality.
  - Initialization, configuration, and trial DAQ run.
- System manages to work in both cases; updated system verified.



## PART 2: UPGRADE OF SOC BOARD

Motivation

- Modern architecture (UltraScale+), better support.
- More computing power (ARM Cortex-A53 64-bit quad-core proc).
- Can connect 2 boards.
- ZCU102 and UltraScale+ architecture more widely used at CERN.
- All for the same price!





## PART 2: UPGRADE OF SOC BOARD

#### Objectives

- Build embedded Linux project suitable for ZCU102 board (derived form Yocto/Xilinx reference repo).
- Migrate Peary, firmware (Vivado design) as appropriate.
- Add CaRIBOu-specific mods (Peary, firmware, packages through metacaribou).
- Validate on board.





#### **DEV & BUILD PROCESS**

- Uses Yocto layers and project setup supported by Xilinx.
- FPGA firmware developed in Vivado.
- CaRIBOu modifications and Peary added through meta-caribou.
- Build system (bitbake) wraps everything up and generates image.



#### **DEV & BUILD PROCESS**





# RESULTS

- Full Linux boot image with meta-caribou modification, Peary, and a 'hello world' firmware.
- Verification with bare ZCUI02 board (not connected to any detector).

Results

- Boot up successful, with a catch.
  - Ethernet problems (currently slows down boot up).
- Firmware verified.
  - Runs an LED program as set up in the block design.
- Peary runs, but memory addresses weren't set up properly yet.
  - Setup both in firmware (block design) and Peary (hardcoded addresses).



## CONCLUSION

- Successfully updated old CaRIBOu system to the latest OS version, with packages and kernel patches fixed.
  - Update process will be documented in written report for future references.
- Successfully build working boot image (Linux) for new ZCU102 board.
- Verified that meta-caribou functionality works and Peary runs on the new board.
- Firmware (i.e. FPGA part) not yet migrated.



## **FUTURE WORKS**

- Firmware (i.e. FPGA part) not yet migrated, so new board cannot interface with detectors yet.
  - Update IP cores, memory addressing.
- Peary has to be migrated as well.
  - Modify hardcoded memory address according to FPGA block design.
- Development and build process will be documented in written report to help with this process.



# EXTRA NOTES

- UltraScale+ architecture on ZCU102 board has various features that may (or may not) be interesting for future developments.
  - RPU, GPU, ...
- There are plans in the Xilinx community to consolidate Xilinxsupported layers.
  - Currently a mess of several layers: meta-xilinx-bsp, meta-xilinx-contrib, metaxilinx-standalone, meta-xilinx-tools, possibly meta-petalinux).
  - Better? More confusing? Both?

