



Novel Detectors for Tracking and Timing *"satellite view"* Pixel 2022

Frank Hartmann

I prepared an introduction talk - a bit of everything

- **Full credits go to the people doing the real work, i.e. not me**
- I am personally very curious to get the real news in the next days

We are all using Silicon in various configurations

Some of us are also using Germanium, Tellurium, Diamonds

Diamonds – NuPECC; ECFA
LHC, GSI, KEK – *BCM, Lumi, Spectroscopy, timing (ToF)*

Si-Strips – NuPECC; ECFA, ApPEC
LHC, KEK, GSI, ISS, Satellite – *position*

Germanium – NuPECC, ApPEC
 γ Tracking
 $0\nu 2\beta$ decay

MAPS/CMOS – NuPECC; ECFA, ApPEC
LHC, STAR, PSI satellite, CBM, medical – *position, imaging*

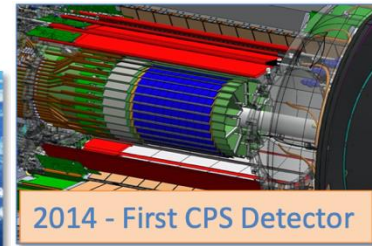
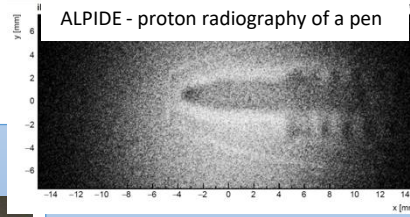
3D silicon – ECFA
Innermost layers - Radiation hard – *position*
ATLAS, CMS, timing

SiPM – NuPECC, ECFA, ApPEC
LHC, GSI, ISS, Satellite, medical (PET, X-ray) – *photons, energy, timing*

Si-Hybrid Pixel – NuPECC; ECFA, ApPEC
LHC, GSI, ISS, Satellite – *position*

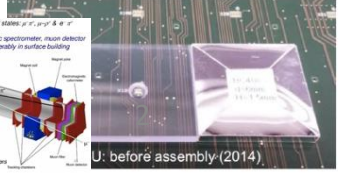
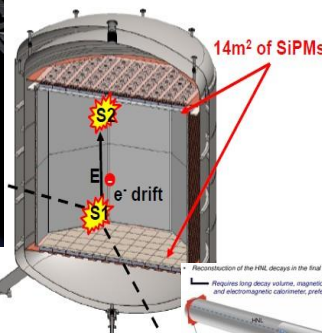
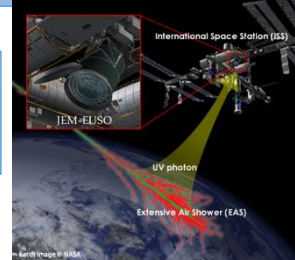
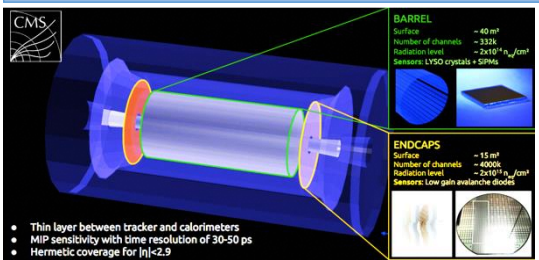
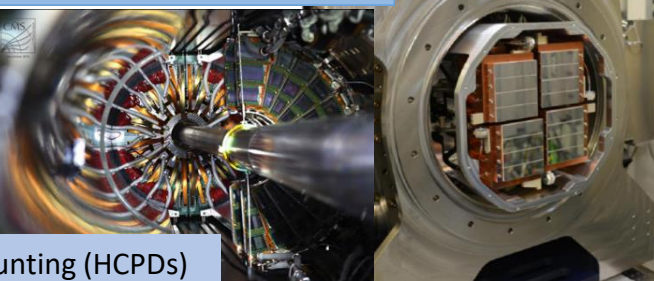
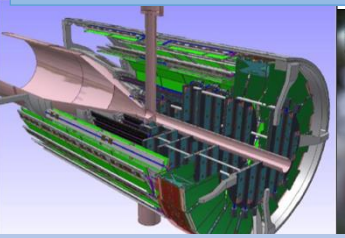
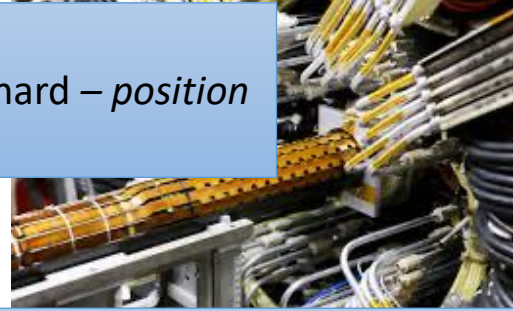
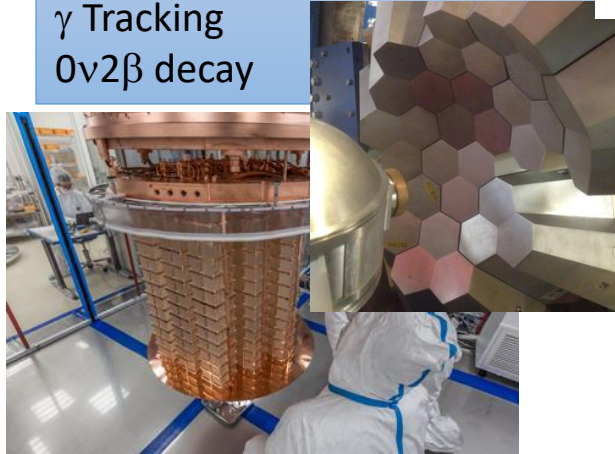
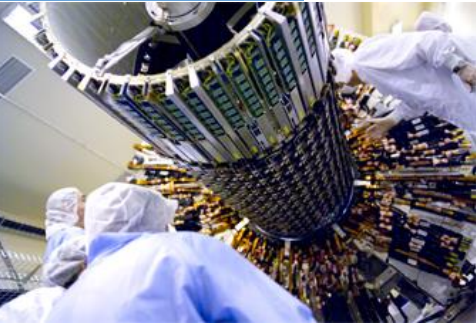
LGADs – ECFA
ATLAS & CMS – *timing, position*

CSES – HEPD2



2014 - First CPS Detector

STAR HFT
0.16 m² – 356 M pixels

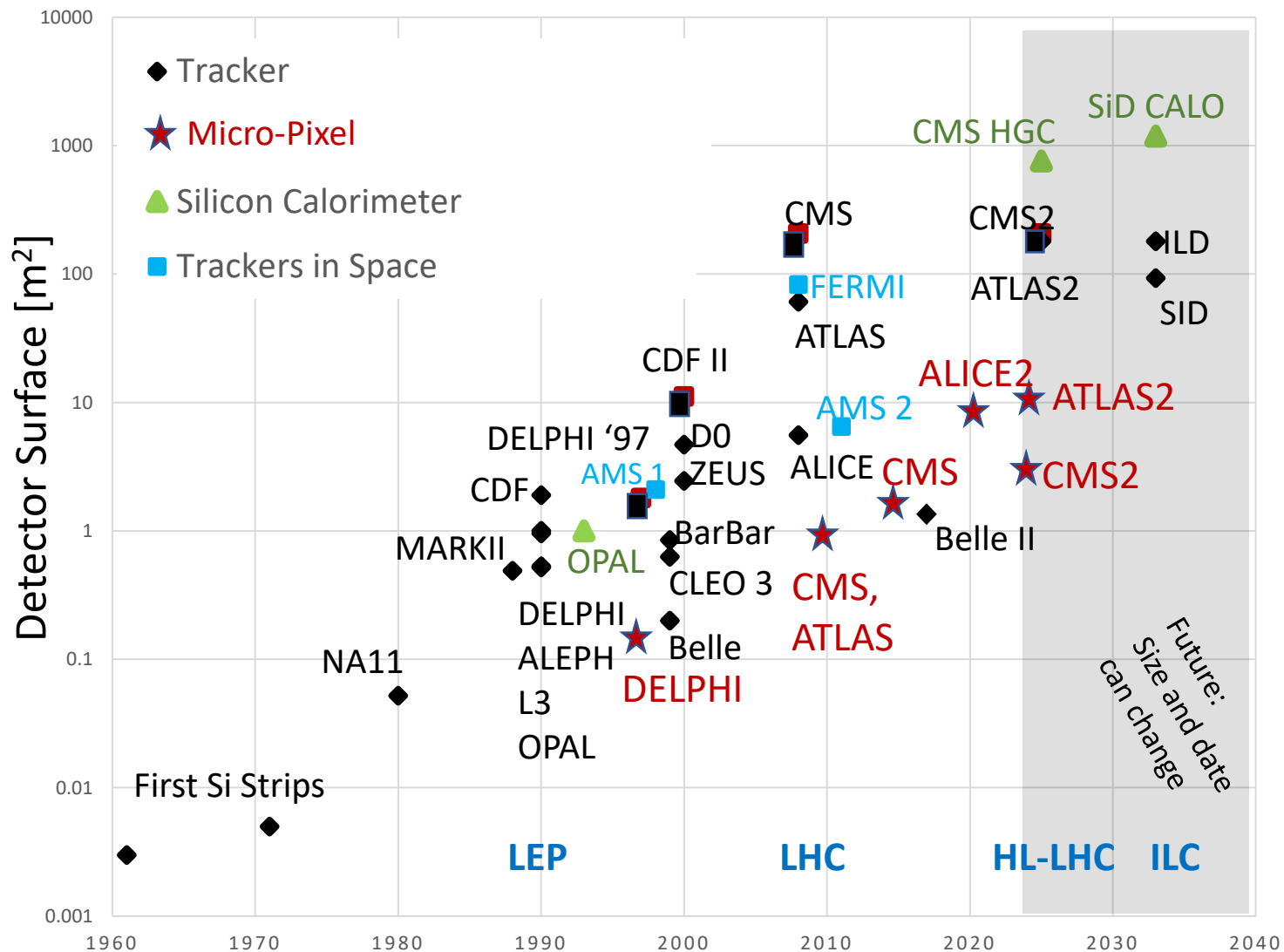


+ synchrotron photon counting (HCPDs)

- Thin layer between tracker and calorimeters
- MIP sensitivity with time resolution of 30-50 ps
- Hermetic coverage for $|\eta| < 2.9$

U: before assembly (2014)

Size matter! Does it?



FCC-h
(no number)

Cell size **goes down significantly**
Cell count **goes up significantly**

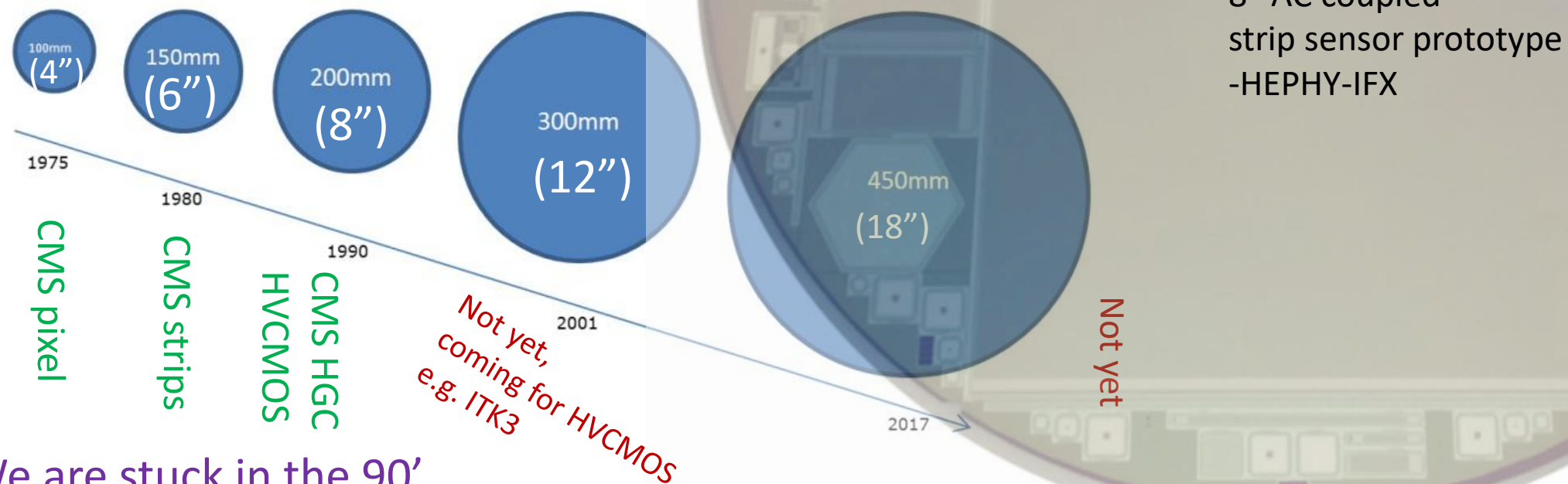
We are counting in GIGA these days

Planar Silicon Sensors - wafer sizes

SILICON DETECTORS WITH 5 μm SPATIAL RESOLUTION FOR HIGH ENERGY PARTICLES

1983! The detectors [2] are made of high-ohmic n-doped silicon single crystal wafers of 2" diameter and 280 μm thickness (fig. 1). Using the planar process [1], p-doped strip diodes, covered by aluminium contacts, are implanted into one side of the wafer. On the other side a

Wafer Areas in Chip industries:



We are stuck in the 90'

I discuss some items, that I consider novel but do not fully fit into the "Pixel" theme and/or are not discussed in later talks this week



Starters

- First 8" sensors for HEP (*for tracking inside a calorimeter and proof of concept for tracker*)
- Passive CMOS – is this a path?
- Level-1 Track and Vertex Trigger – a concept not a sensor, but needs *macro-pixel!*

Main

- Timing detectors and their evolution
 - Planar and 3D – with and without gain
- 3D pixels and their evolution
- HV-CMOS/DMAPS – is this the future?

Dessert

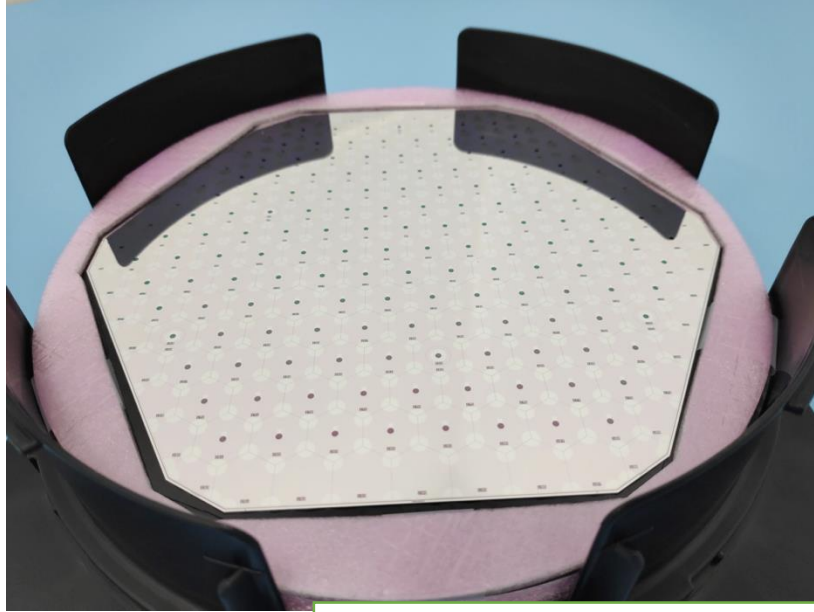
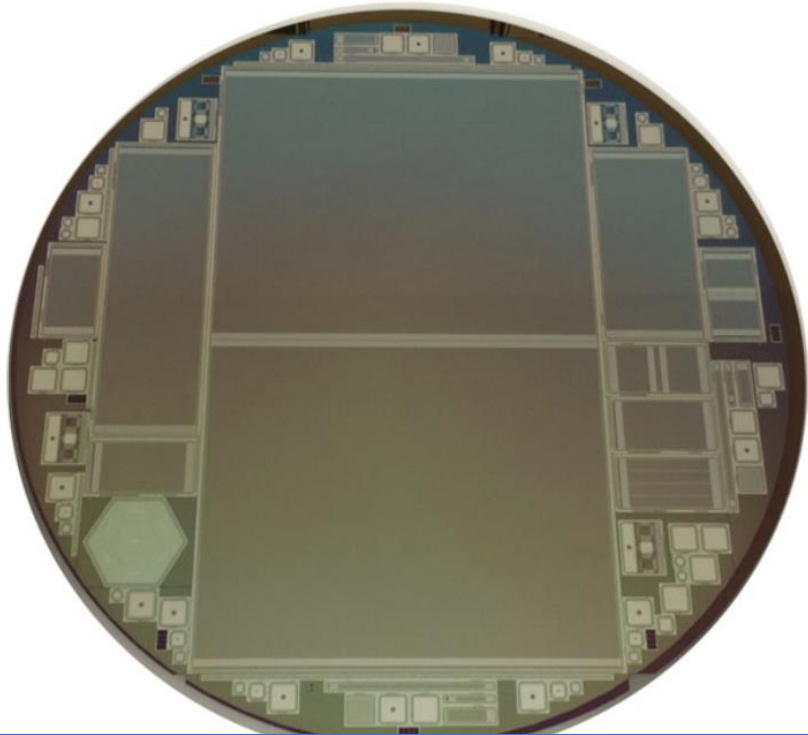
- Coffee Break



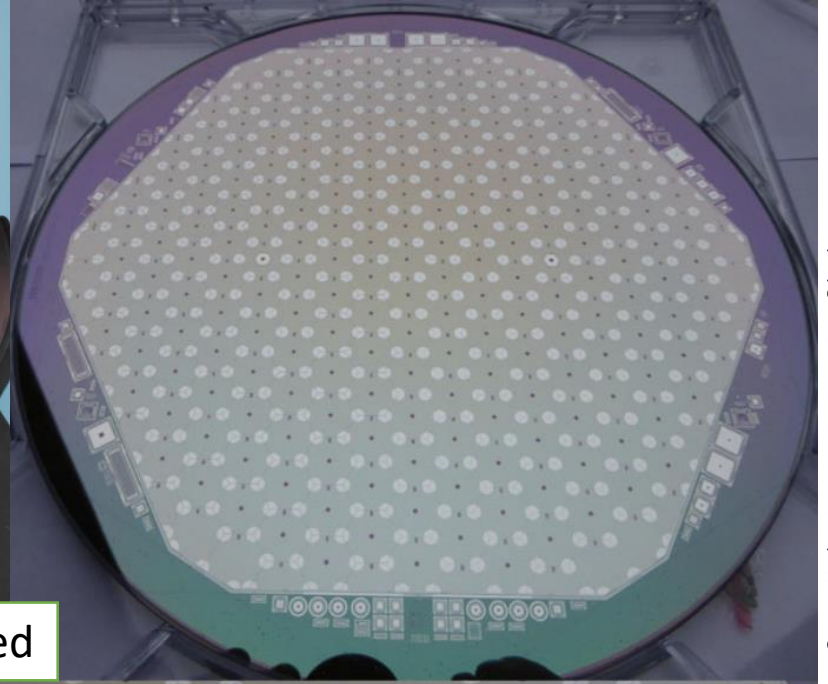
Appetizers

8" wafers – a big and novel step, but not for all!?!?!?

8" n-in-p strips AC-coupled



8" n-in-p pads DC-coupled



8" is a **game changer** for 'really-large-area' detectors, like the CMS forward imaging calorimeters. And, the hexagonal shape pad sensor uses the circular area in an optimal way - ratio of sensor/wafer

8" **not** for **strip** tracker as ratio of sensor/wafer not ideal; and 6" still more mature. *Both ATLAS and CMS are using 6"!* Hybrid pixels would strongly benefit on real estate, and especially on flip-chipping effort/cost.

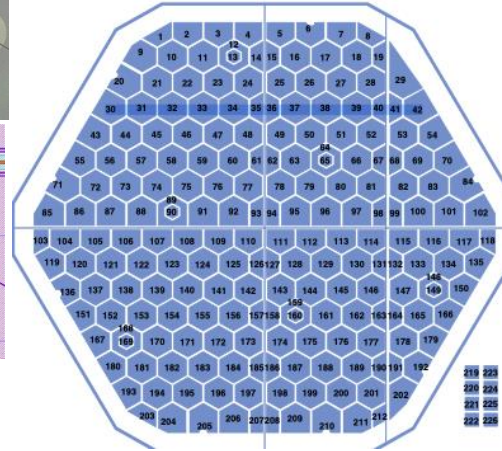
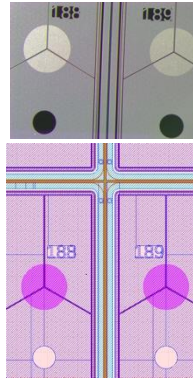
I am also aware of 8" wafers for active* & passive CMOS sensors and LGADs!
At coffee you tell me where else!

* e.g. ALPIDE 8" and ITS targets 12"

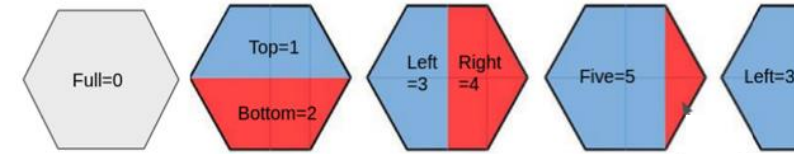
Another cost saving, novel idea – Multi-Geometry Wafer

Use one mask and cut to different geometries

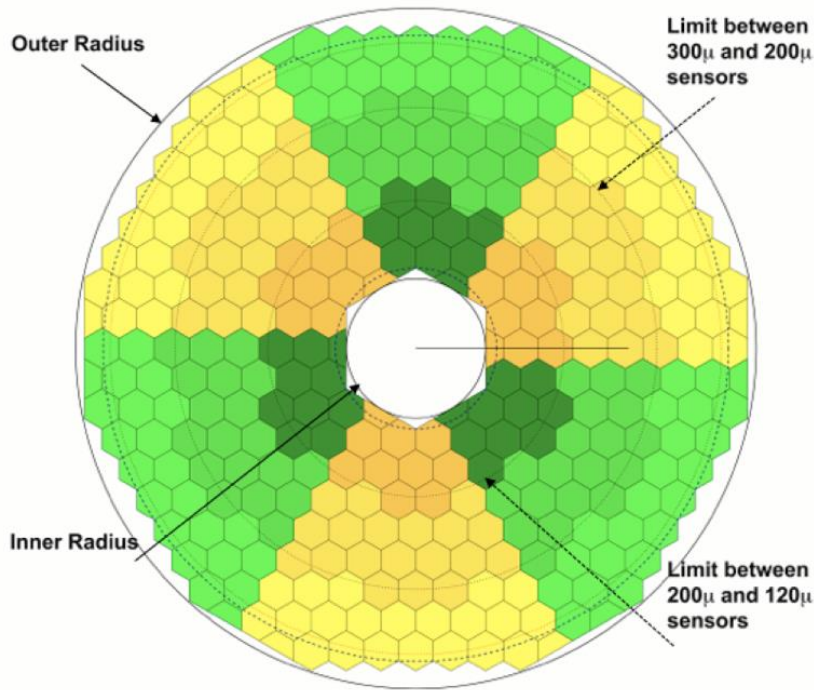
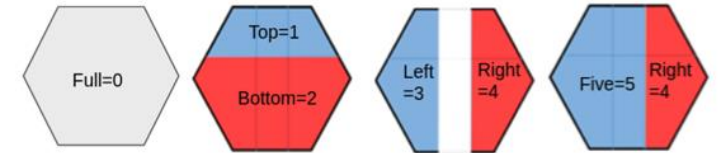
CMS needs many so-called 'partials'



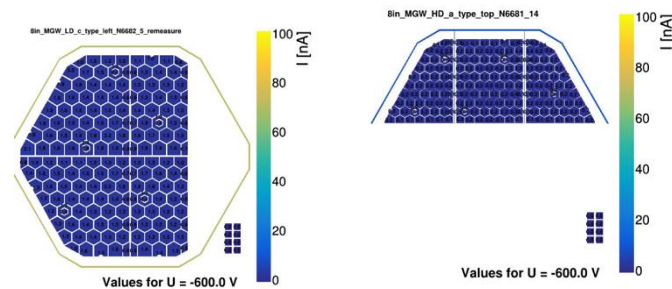
LD partial sensor layout names



HD partial sensor layout names

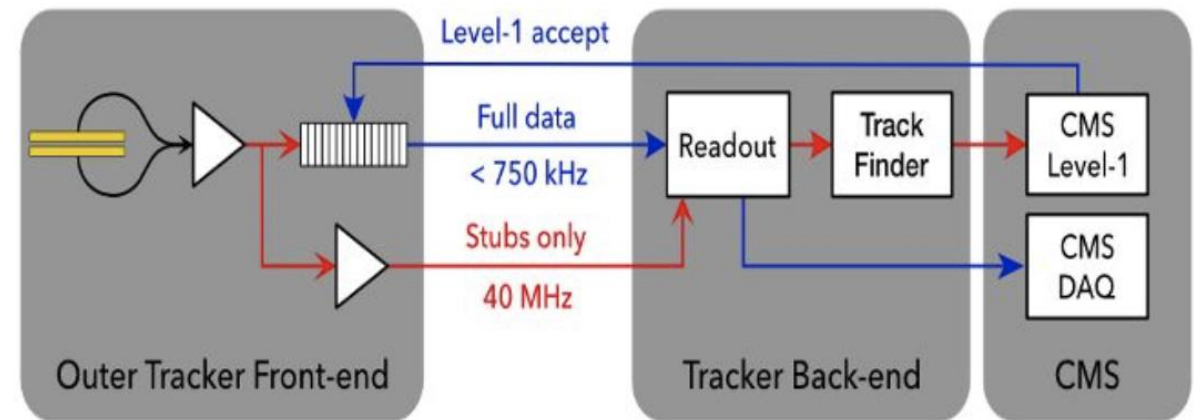
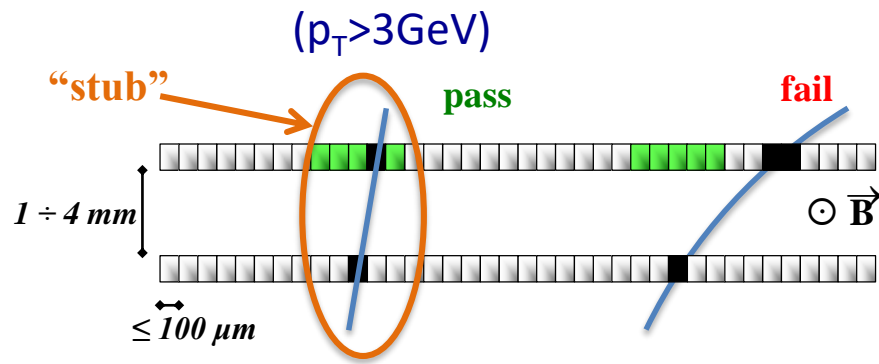


Pay attention to the cutlines, guard and bias lines.
Et Voila it works!



Triggering on tracks at 40 MHz – CMS Phase-2

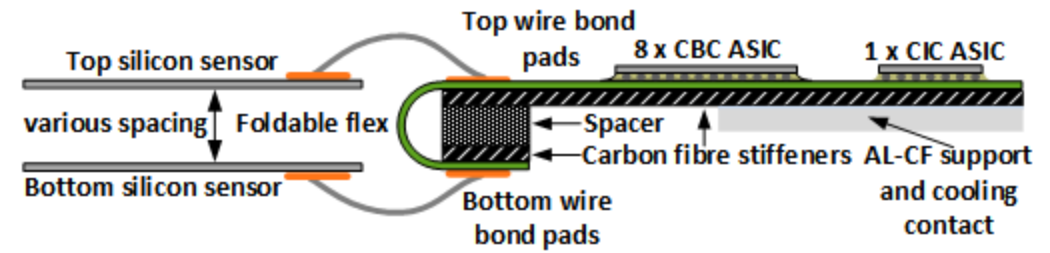
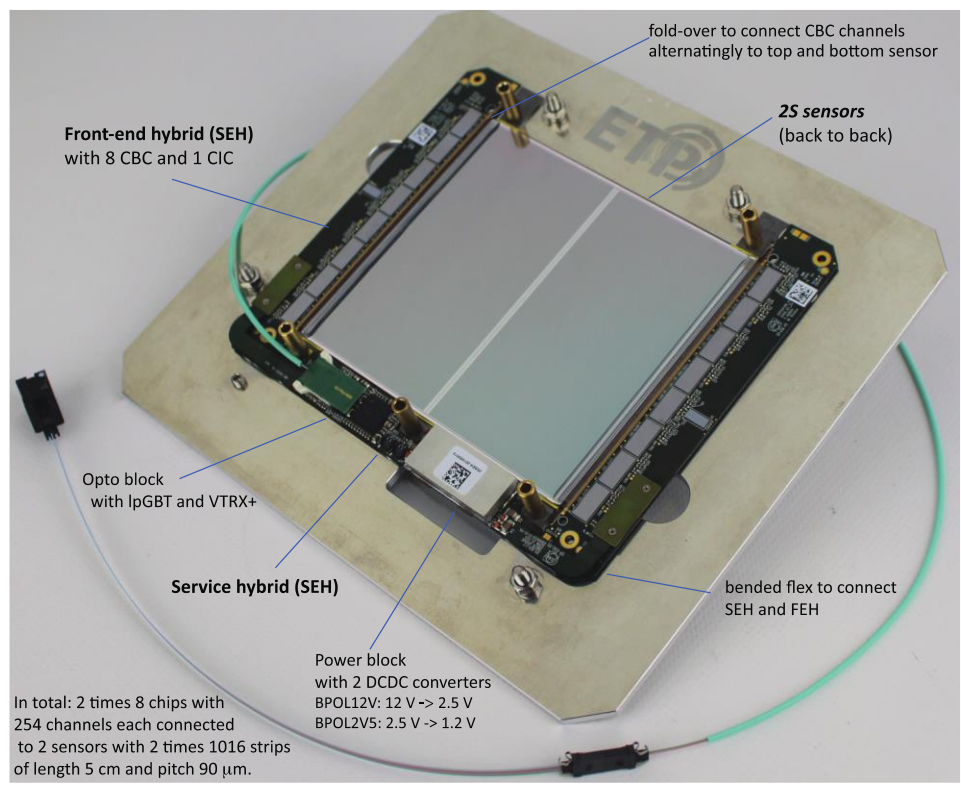
- Traditionally, Trackers cannot be read out at full speed
 - too complex, too much data, not enough bandwidth
 - 'a track' as a trigger object needs information of several layers *but they are not connected*
- Can we connect internally? Yes we can – a bit, very local, on parts of the track!



- But what about the z coordinate?

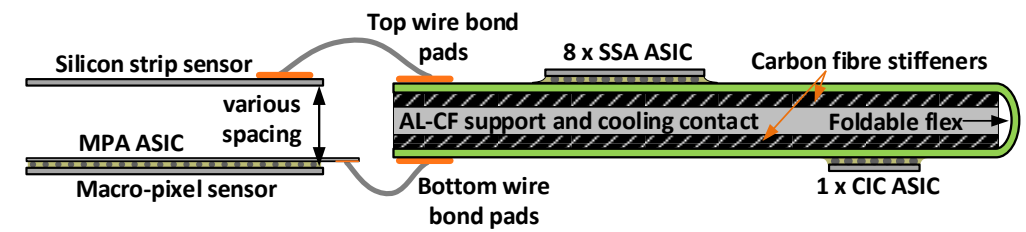
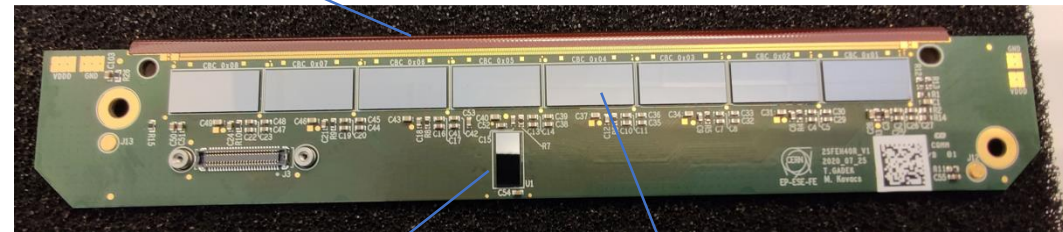
Stub data being sent out at 40 MHz
(data reduction factor 10, still ~ 80% of bandwidth)
Full track reconstruction in backend FPGA (~4 μ s) as trigger objects

How does it work locally? Is there a drawback? Stereo angle? Z-resolution?



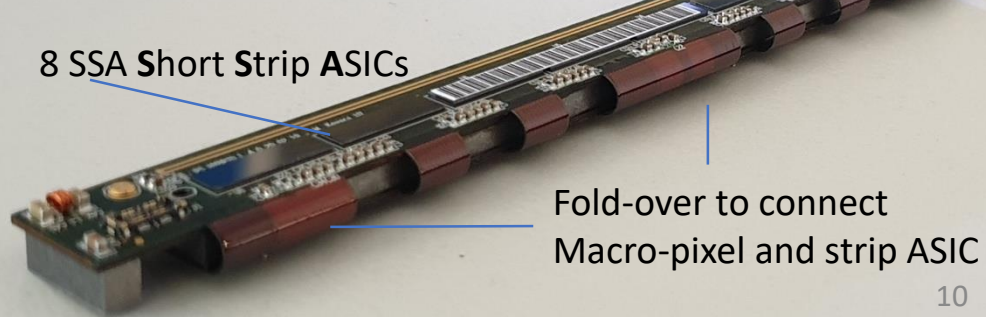
Front-end hybrid (FEH) - 2S module

Fold-over to connect CBCs to both sensors



Front-end hybrid (FEH) - PS module

(left version)

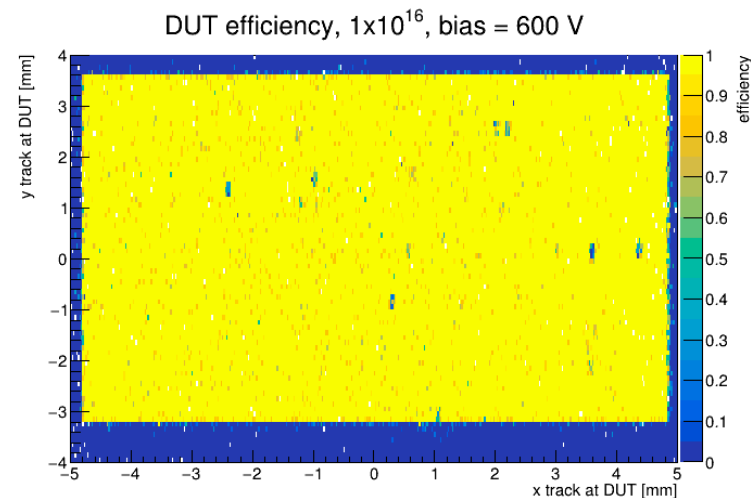


- Bottom and top strips connected to same ASIC via flex fold-over, doing the correlation
 - Strips parallel - stereo angle not possible – no z-resolution only p_T
- 2nd module version with 1.5 mm macro-pixels (and 2.5 cm strips)
 - Strip ASICs provide info to pixel ASIC doing the correlation
 - Unambiguous z-resolution at trigger level (~1mm vertexing possible) - @trigger
 - Results in a 25 m² macro-pixel detector (bump bonded)

Passive CMOS sensors – a cost effective alternative?

- In search of more sensor producers, several groups are evaluating strip and pixel sensors from CMOS companies!
 - Use n-well/p-well/metal/polysilicon layers for sensor implantations, biasing, field shaping
- The process is distinctively different to 'our' standard, mature planar process!
Different = new **complications** and new **opportunities**.
Mask sizes are limited to so-called reticles – same limits as for ASICs
 - Large sensors can only be realised by stitching
 - **Multiple metal layers** allow interesting redistributing schemes, e.g. disentangle electrode implant from readout connection
 - **MIM** (Metal-Insulator-Metal Capacitance) allows AC coupling for small structures (pixels) with decent coupling
 - **HIGH** and **LOW** resistivity **polysilicon layers** allow for bias resistors on small real estate or field shaping structures

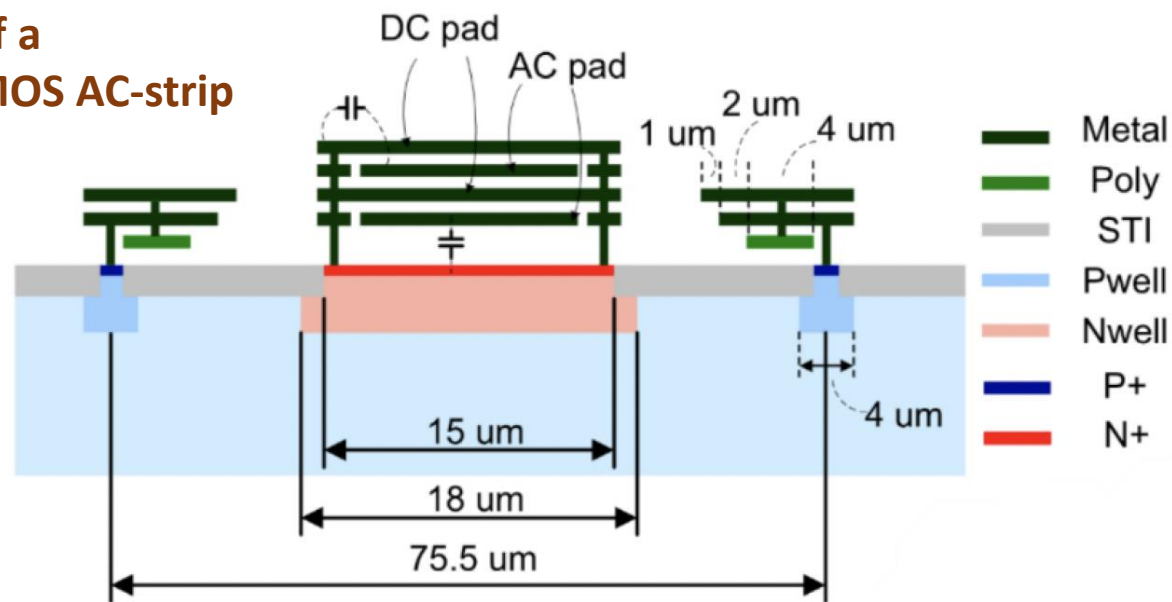
• In a nut-shell it works!



Obviously many features are common to **active** CMOS sensors.

Not our usual Planar Process

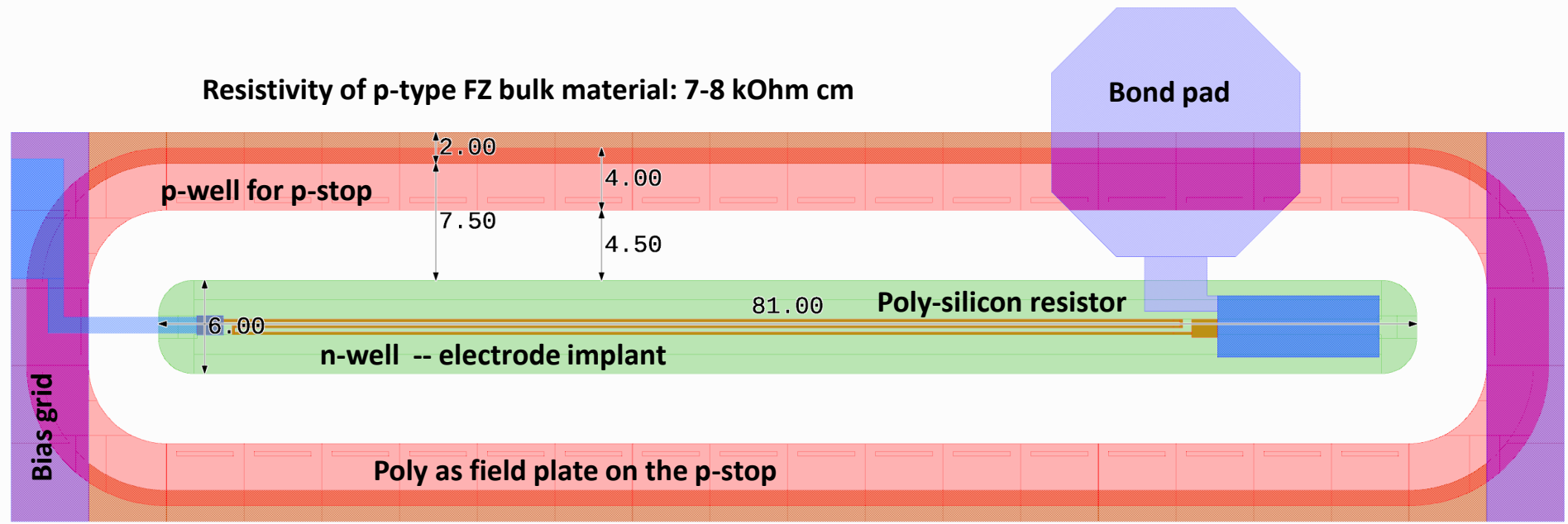
Example of a passive CMOS AC-strip



<https://arxiv.org/abs/2203.11376>; <https://arxiv.org/abs/2111.07797>; <https://arxiv.org/abs/1702.04953>
NIMA 1033 (2022) 166671

Example of a passive CMOS DC-pixel

Resistivity of p-type FZ bulk material: 7-8 kOhm cm

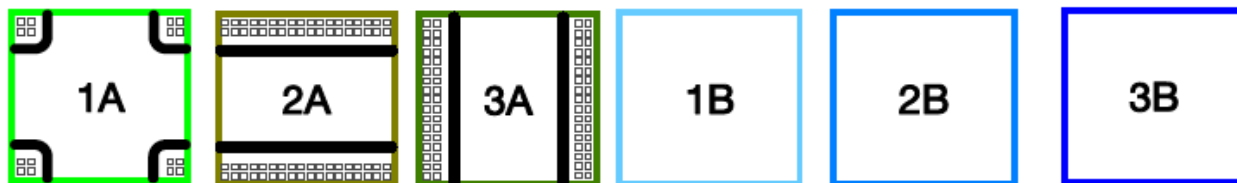


Courtesy CMS Pixel

Reticle stitching

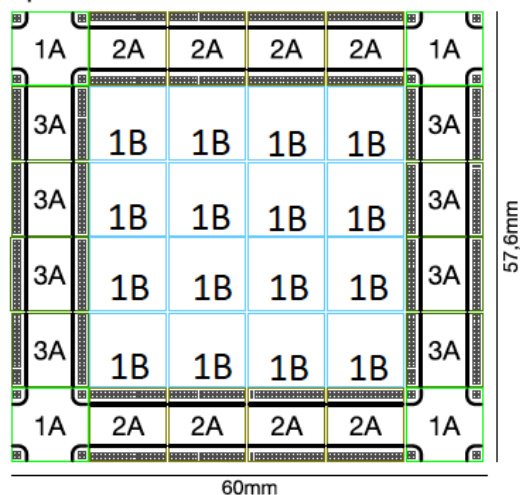
Sensor size > reticle size 26 mm x 32 mm → reticle stitching needed

- Different sub-reticles (~ 1 cm x 1 cm) for edge and active areas:

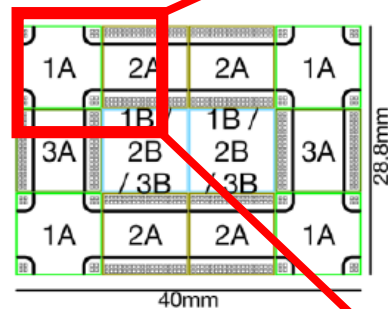


- Repeat them for different designs:

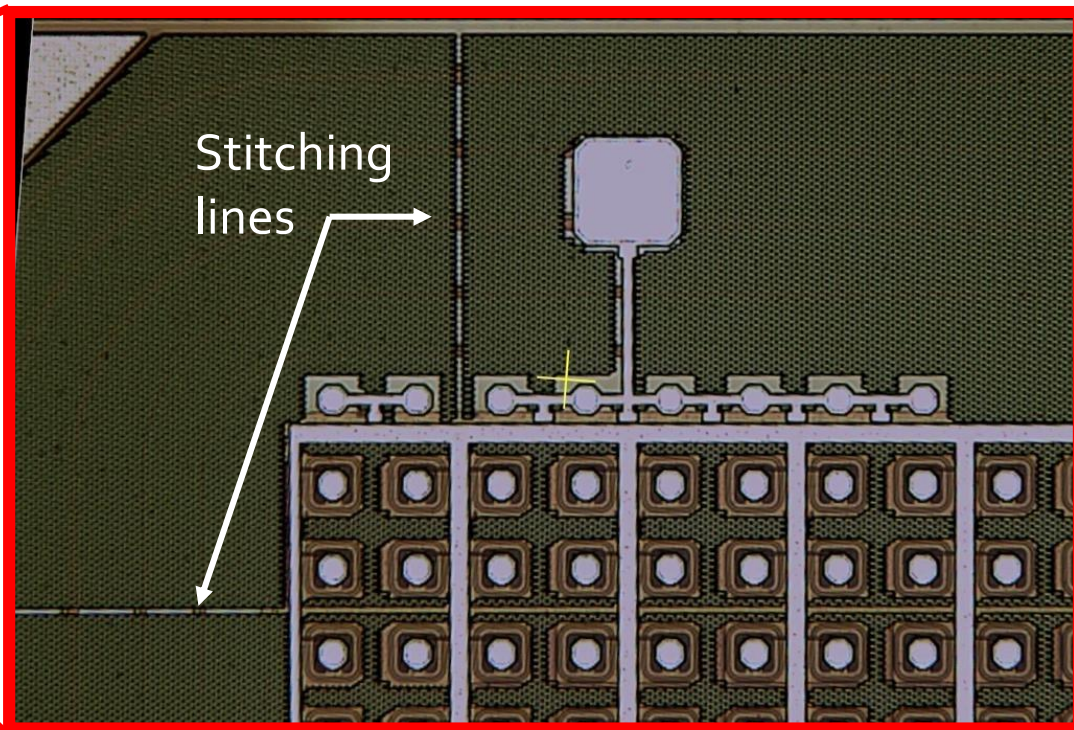
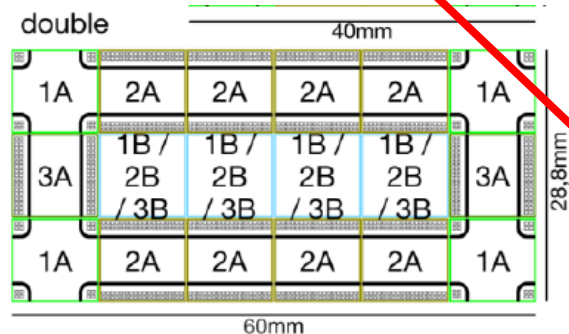
quad



single



double



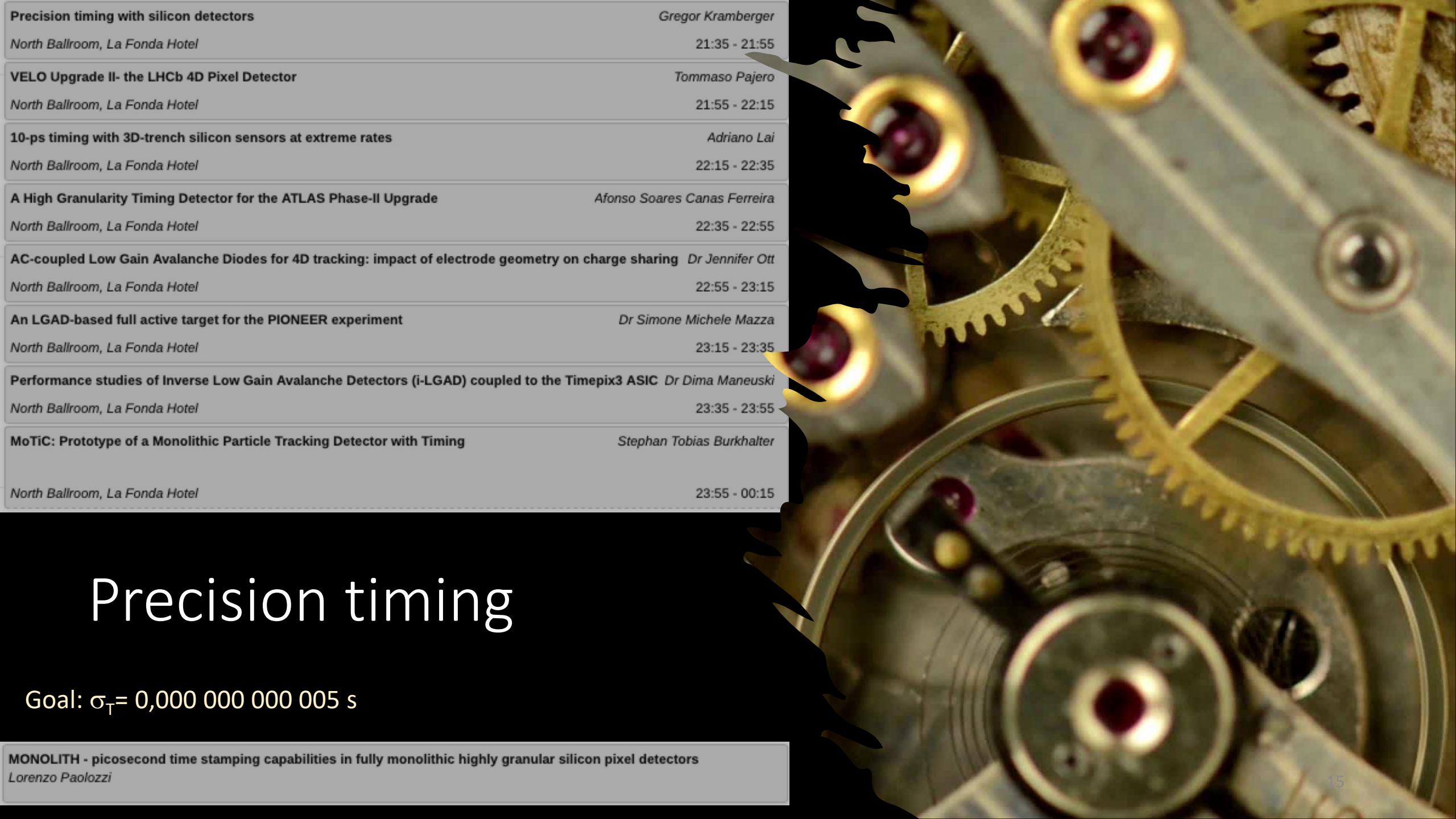


Onto the three main courses

Timing

... 3D

... HV-CMOS



Precision timing with silicon detectors	<i>Gregor Kramberger</i>
<i>North Ballroom, La Fonda Hotel</i>	21:35 - 21:55
VELO Upgrade II- the LHCb 4D Pixel Detector	<i>Tommaso Pajero</i>
<i>North Ballroom, La Fonda Hotel</i>	21:55 - 22:15
10-ps timing with 3D-trench silicon sensors at extreme rates	<i>Adriano Lai</i>
<i>North Ballroom, La Fonda Hotel</i>	22:15 - 22:35
A High Granularity Timing Detector for the ATLAS Phase-II Upgrade	<i>Afonso Soares Canas Ferreira</i>
<i>North Ballroom, La Fonda Hotel</i>	22:35 - 22:55
AC-coupled Low Gain Avalanche Diodes for 4D tracking: impact of electrode geometry on charge sharing	<i>Dr Jennifer Ott</i>
<i>North Ballroom, La Fonda Hotel</i>	22:55 - 23:15
An LGAD-based full active target for the PIONEER experiment	<i>Dr Simone Michele Mazza</i>
<i>North Ballroom, La Fonda Hotel</i>	23:15 - 23:35
Performance studies of Inverse Low Gain Avalanche Detectors (i-LGAD) coupled to the Timepix3 ASIC	<i>Dr Dima Maneuski</i>
<i>North Ballroom, La Fonda Hotel</i>	23:35 - 23:55
MoTiC: Prototype of a Monolithic Particle Tracking Detector with Timing	<i>Stephan Tobias Burkhalter</i>
<i>North Ballroom, La Fonda Hotel</i>	23:55 - 00:15

Precision timing

Goal: $\sigma_T = 0,000\ 000\ 000\ 005\ s$

Precision timing

– WHY, do we need it and *WHAT* and *WHERE*?

Why? Probably by consensus as we all like it :-)

It is new!

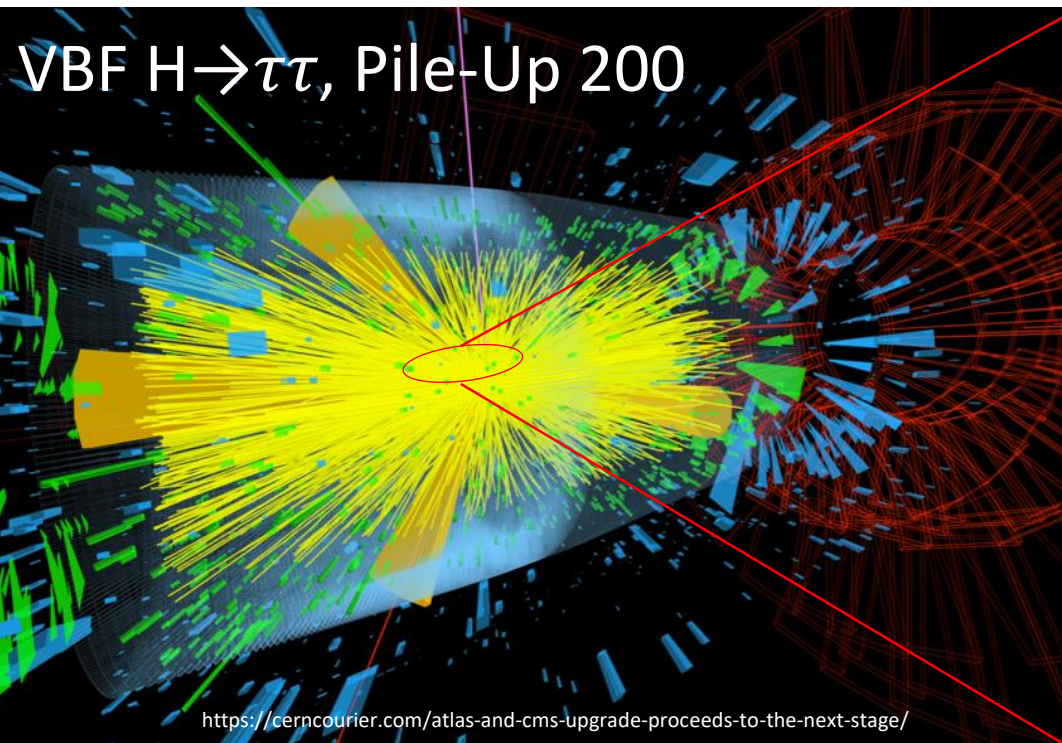
1. Precise timing information of ‘a track’
 - mitigate pile-up, PID in Heavy Ion, increase reach to measure LLP
 - Here **modest spatial information** is OK, good fill factor is a plus – **LGADs and scintillator can do the job**
2. Precise timing information of ‘track points’, or of ‘each track point’
 - all the above plus reduce combinatorics for track finding
 - **Superb spatial information & 100% fill factor** is mandatory – **standard LGADs are probably NOT good enough!**

LHCb 4D Pixel Detector
– by Tommaso

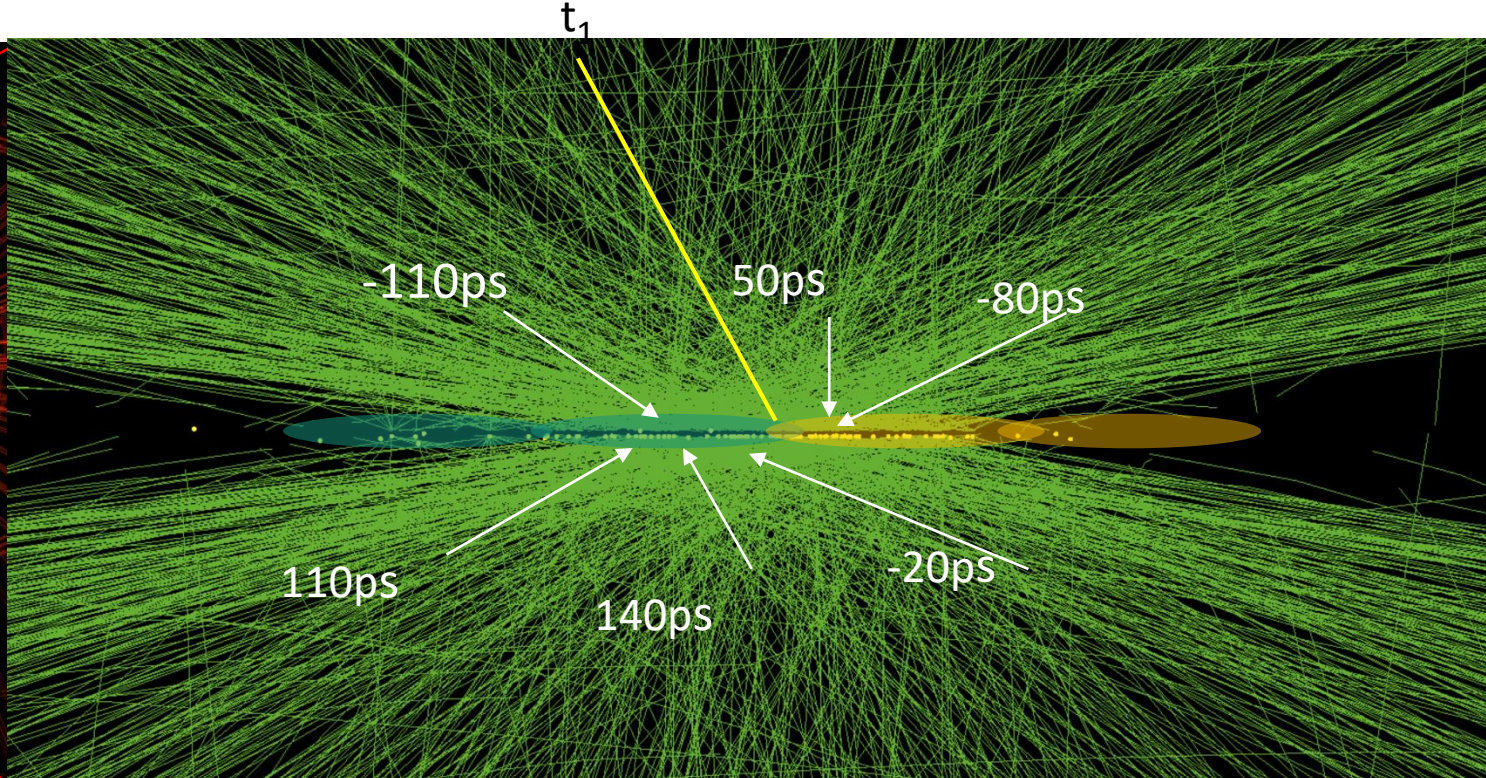
➔ **Ok, we want superb timing and spatial precision with 100% fill factor, (all in **power budget**) in general it must be radiation tolerant and best full-monolithic and with volume suppliers**

I am looking forward to “Precision timing with silicon detectors” – by Gregor

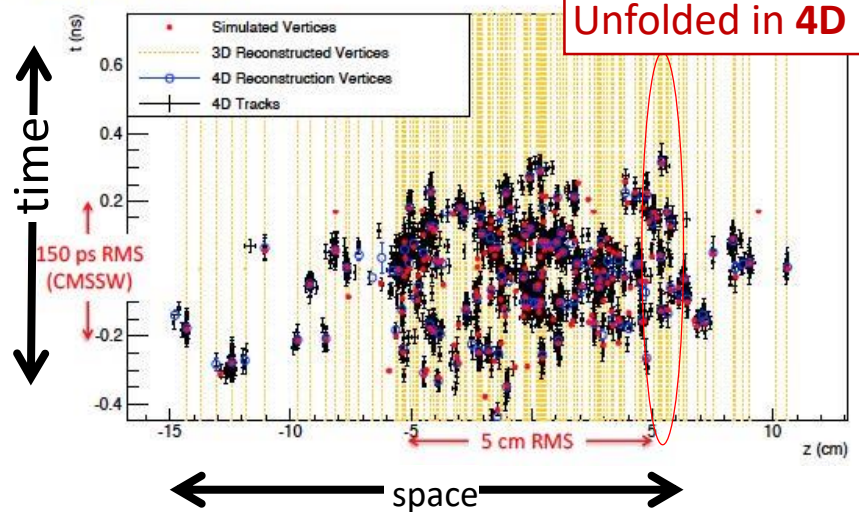
VBF $H \rightarrow \tau\tau$, Pile-Up 200



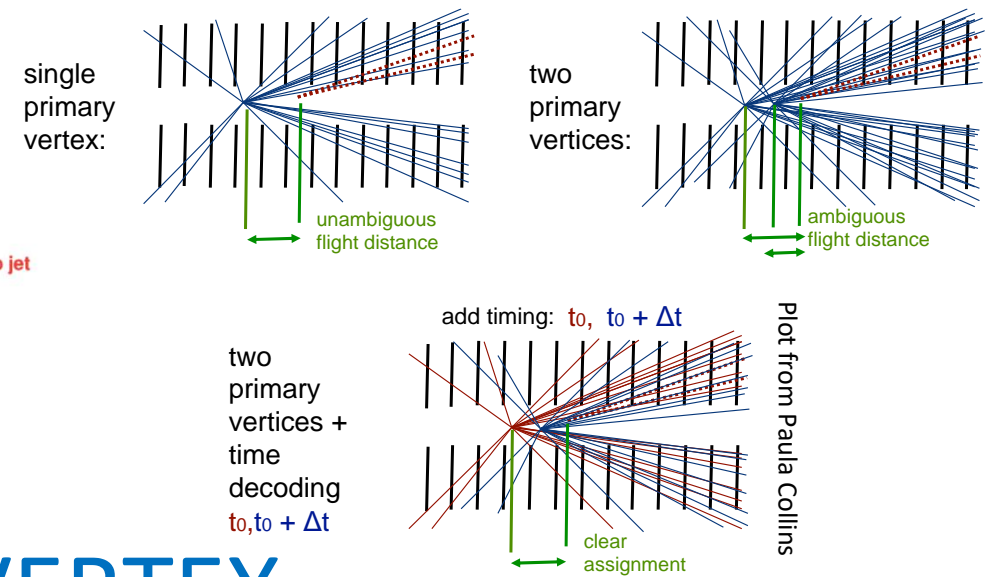
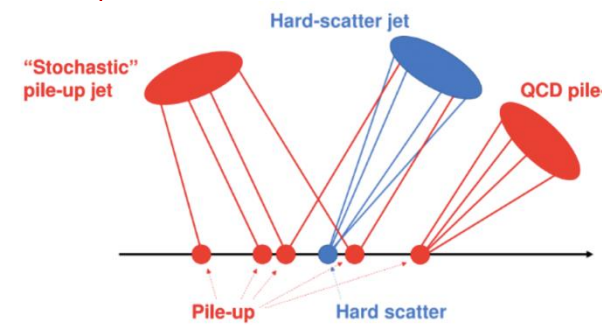
<https://cerncourier.com/atlas-and-cms-upgrade-proceeds-to-the-next-stage/>



200 pileup collisions

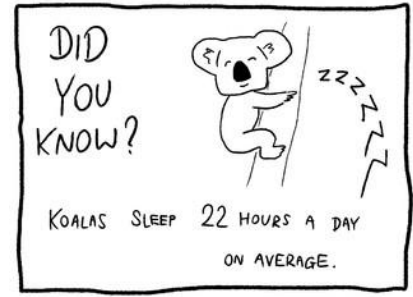


Ambiguous in 3D space
Unfolded in 4D



CLEAN YOUR VERTEX

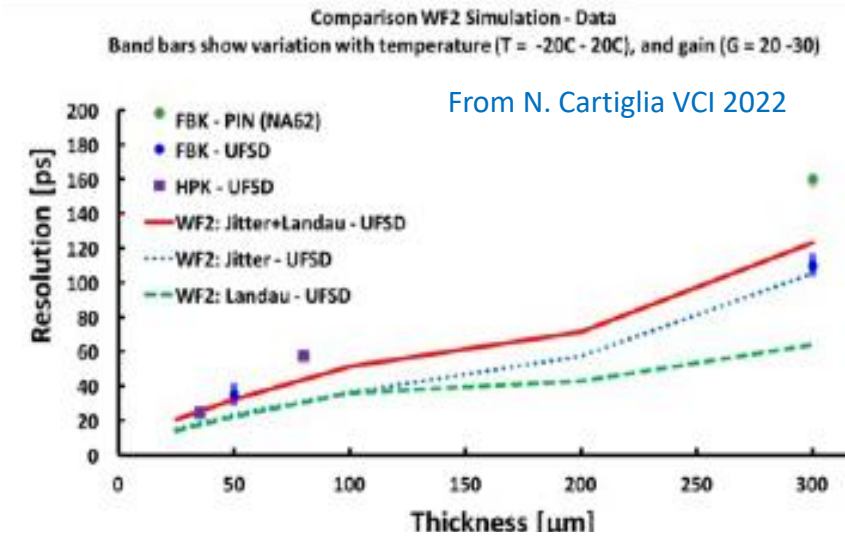
A bit of random wisdom (no no, not from me)



Stock.adobe.com

- Intrinsic timing capability of sensors is basically infinite* (sub ps) – **W. Riegler**
- Landau noise (non-uniform ionization - *spatial*) and electronic noise is the issue – **everybody says this**
 - Decreasing electronic noise ‘costs’ power’, which is ‘limited’ – **I say this but I heard it from somewhere**
 - Decreasing sensor thickness decreases drift length and Landau noise – **from the experts**
- Using signal **gain** beats electronic noise and decreases ‘jitter’, - wait for the electrons to arrive at the gain layer (similar for concentrated weighting fields)
- In “timing circuits”, things can go wrong very rapidly (quote stolen from a chip designer) – **N. Cartiglia**

Landau noise = physical limit of timing precision



$$\sigma_t^2 = \sigma_{\text{Time walk}}^2 + \sigma_{\text{Landau noise}}^2 + \sigma_{\text{jitter}}^2 + \sigma_{\text{Distortion}}^2 + \sigma_{\text{TDC}}^2$$

Compensate in electronics

Go thin

Weighting field

electronics

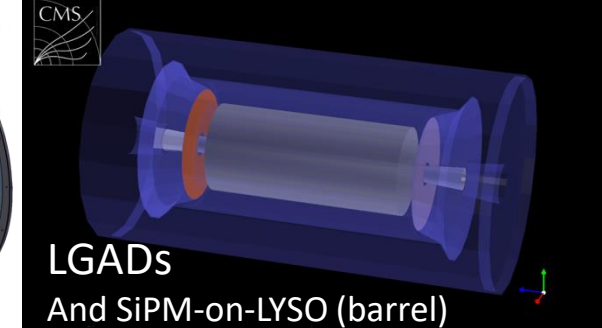
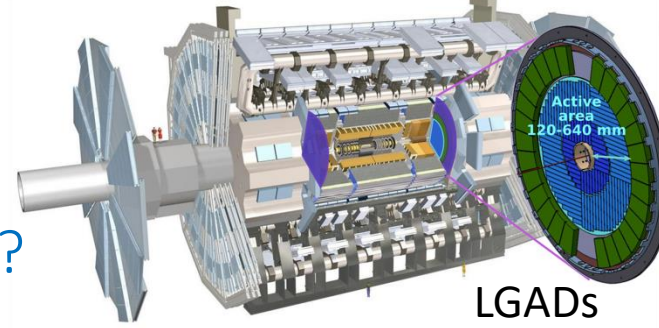
$\sigma_t = \frac{\text{noise}}{dV/dt}$

* acceleration of electrons to 10⁷cm/s in vacuum is 0.14ps & passage of the particle through a 50um sensor takes 0.16ps

Low Gain Avalanche Detector - LGAD

aka the **working horse** for HL-LHC

aka the mature but already obsolete technology??



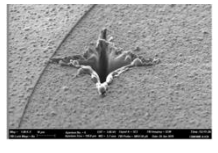
- Timing precision $\sigma_t = <30$ ps
- Fill factor mediocre (~80%)
as inter-pad region = no gain
- Spatial precision ~mm



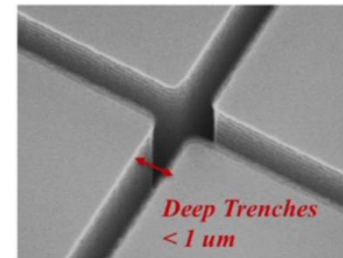
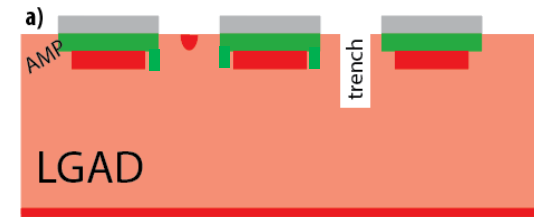
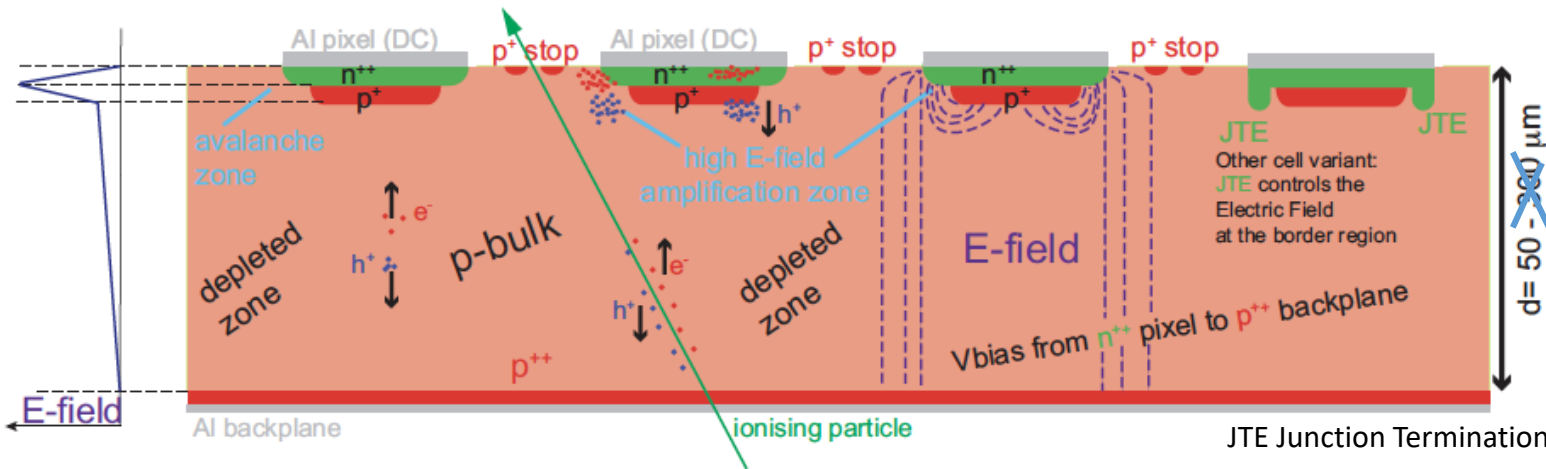
Numerous iterations, testbeams, market survey – several vendors, radiation studies

➔ **Mature technology** $\sim 2 \cdot 10^{15} \text{ MeV}_n/\text{cm}^2$

- E.g. adding of C in gain layer
- Understood single event burnout!
- Lots of effort to increase fill factor, e.g. TI-LGADs Trench Isolation LGADs
 - $\sim 50 \rightarrow 5 \mu\text{m}$ dead zone



From CMS ETL



Single Trench Layout

Double Trenches Layout

From AIDAinova

Function: Signal from electron avalanche – arrival time starts avalanche – gain beats noise/jitter – **limit is Landau noise**

Thinner sensor decreases Landau Noise - shorter drift time (shorter path and higher field) (& no weighting field effect as pads >> thickness)

And, the LGAD concept
is not brand new

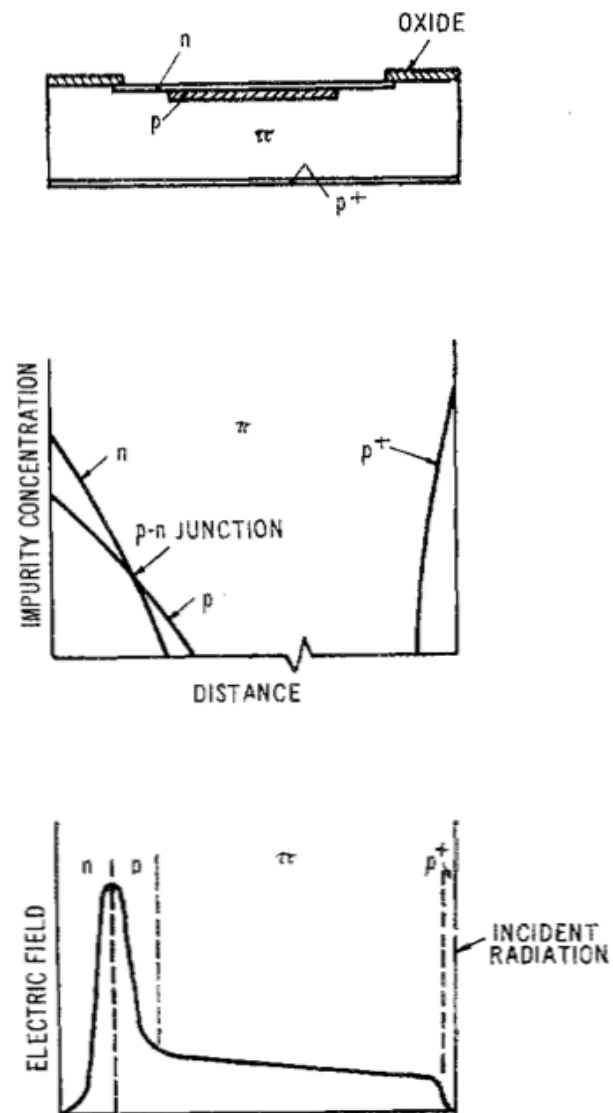


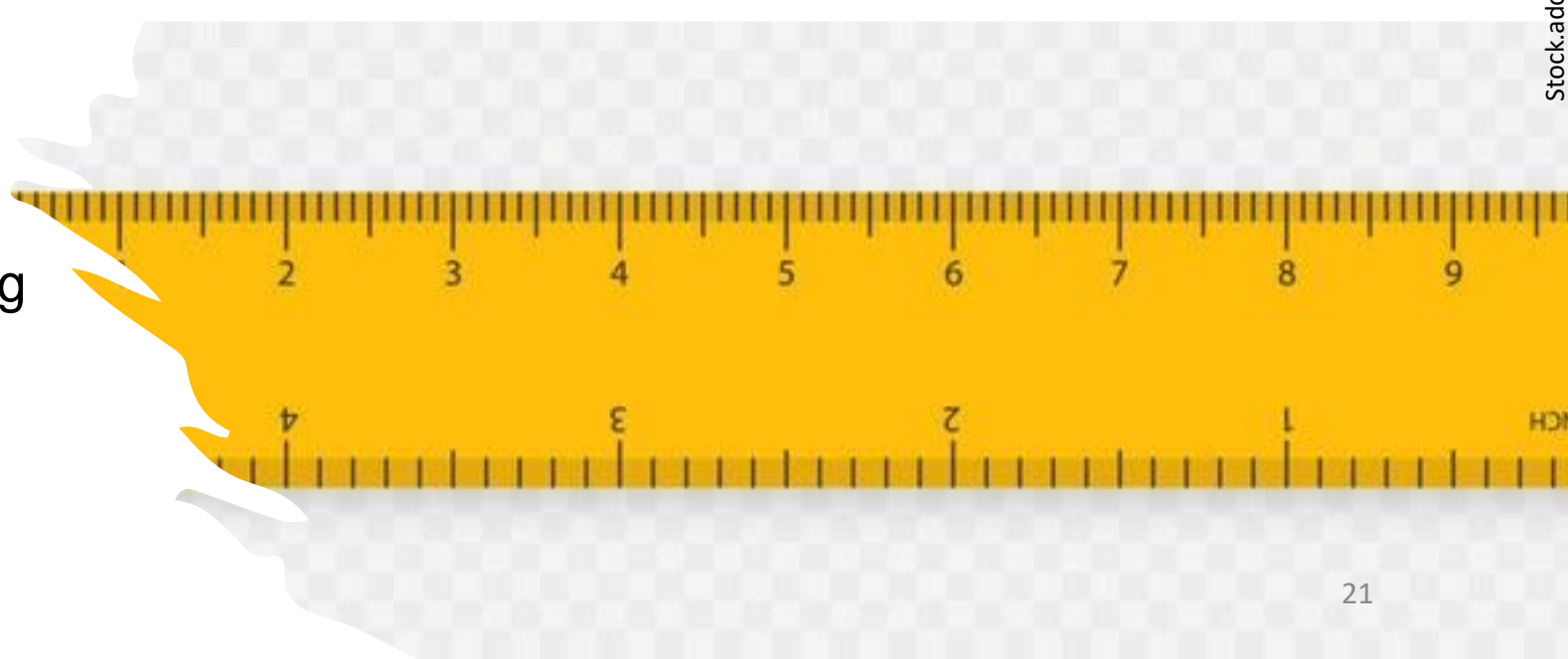
Fig. 1. Sketches of reach-through avalanche-diode structure, impurity-concentration profile, and electric-field distribution.

From Abe Seiden, Hartmut Sadrozinski and Nicolo Cartiglia pioneers on LGADs:

I'm wondering if we can do both measurements (space and time) in one object, a silicon detector with very good timing resolution.

We thought it was a dumb question...but over lunch, we jotted down some numbers.

... The main question is understanding the gain in silicon sensors

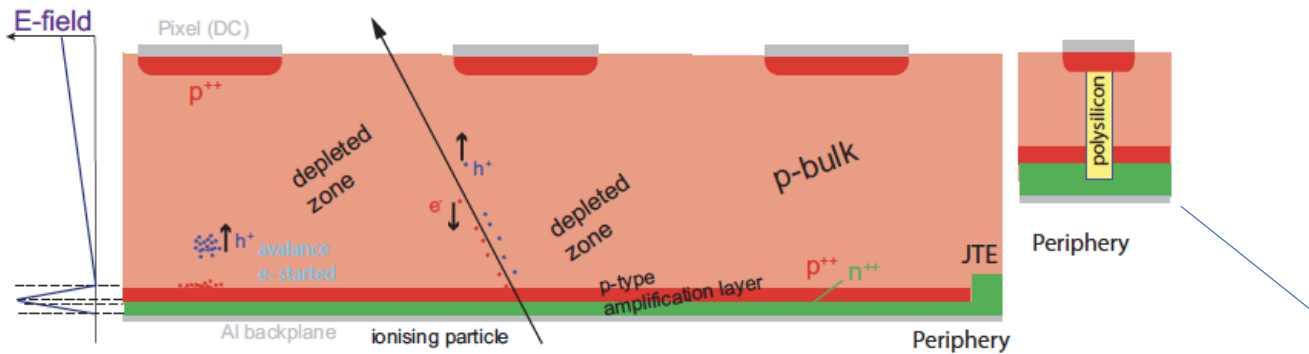



Ok, we achieved precision timing

Now let's think about fill factor and spatial resolution!

MOVE the amplification layer - Disentangle amplification and readout electrodes

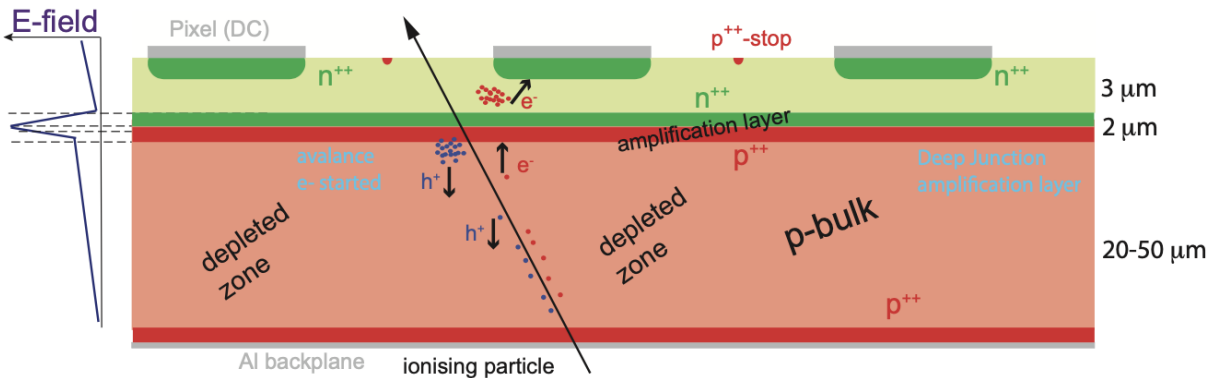
• Inverse LGADs




- Fill factor 100% 
- Spatial resolution – good
- Timing limited to ~100 ps
 - Thickness ~ 300 μm
 - JTE at back ask for **double** sided process
 - hole collection
- New version using 3D technology
 - Thin and slim edge & **single** sided process

Performance studies of Inverse Low Gain Avalanche Detectors (i-LGAD) coupled to the Timepix3 ASIC – by Dima

• Deep Junction LGADs – DJ-LGADs



- Fill factor 100% 
- Spatial resolution – good
- Timing good < 30 ps
- How easy to build?? Finetuning??

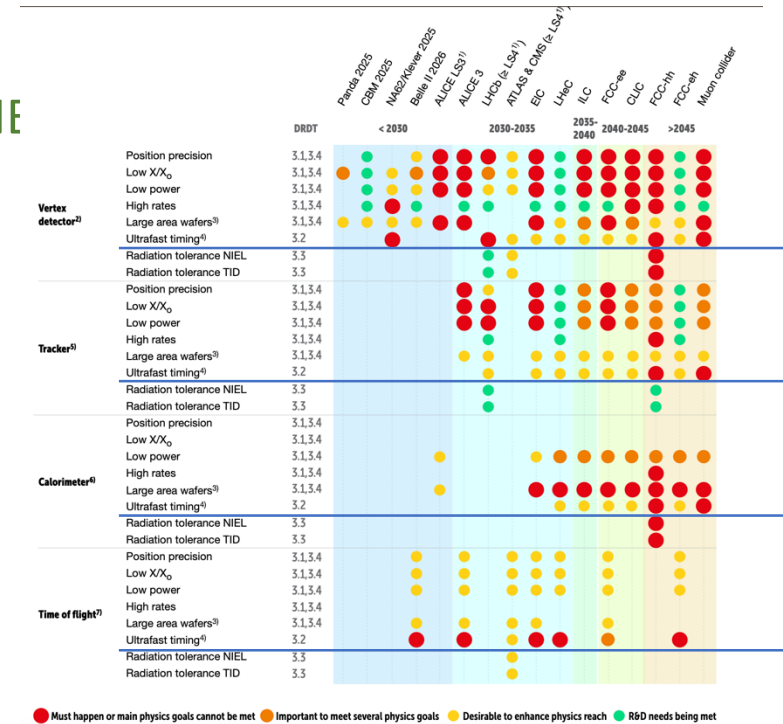
Same function, advantages and limitation of standard LGADs on timing (signal starts at arrival)

– limit is Landau noise

Timing, *same* reason for everybody??

(see DOE Basic Research Needs for High Energy Physics Detector Research and Development Report, ECFA roadmap, Snowmass)

- HL-LHC (mitigate pile-up, PID in Heavy Ion, increase reach to measure LLP) - 30 ps – DONE
- Future e+e- colliders (Higgs Factories):
 - Spatial Resolution ~3 μm
 - Time resolution - would enhance **particle identification** and reconstruction
- Future Hadron collider **Pileup** (~1000; 4THz of tracks) and radiation levels up to 8×10^{17} n/cm²
 - Track resolution < 10 μm per layer
 - Time resolution 5 – 10 ps
- Muon Collider - for **BIB background** rejection
 - Track and time resolution 20 – 30 ps
- Electron-Ion Collider (EIC) Time of Flight (ToF):
 - fine time and space resolution needed for **PID** π/K/p separation at low/medium momentum
 - 20 – 30 ps timing per hit
- Very Forward Physics **PPS** at the (HL-)LHC and future hadron colliders:
 - fine time and space resolution needed for precise proton momentum reconstruction and **association to correct vertex**
 - 5 ps timing to suppress pileup (needs many timing layers), 5 μm tracker resolution
 - Greatly reduced to 20 ps in case 4π timing detector in the central region

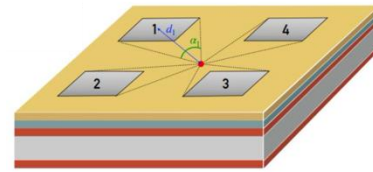
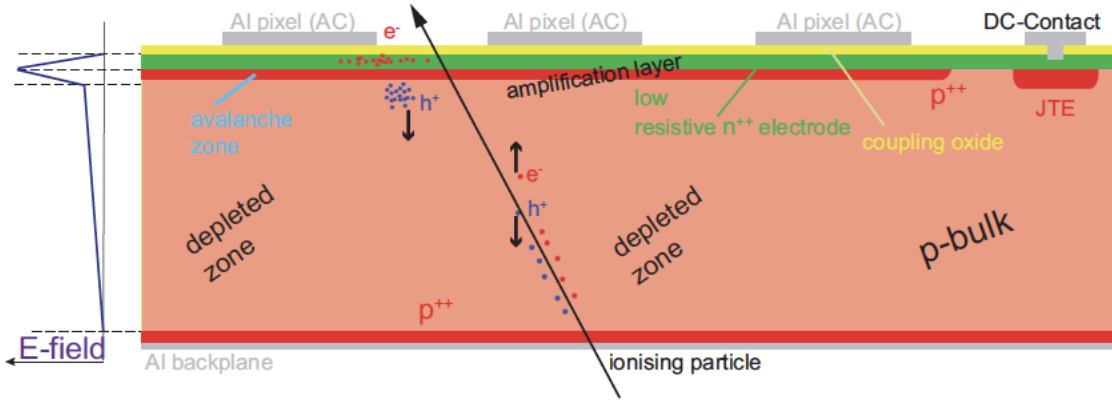


➔ 20 – 30 ps seem OK **but** for FCC-hh

Evolving further

– and apologies for all developments I overlooked

• AC-LGADs or Resistive Silicon Sensors RSD



- Timing ~ 30 ps  
- 100% fill factor
- $\sim 5 \mu\text{m}$ spatial resolution with $150 \mu\text{m}$ pitch



- Excellent ratio
- Due to charge distribution and sharing in intrinsic low resistivity n^{++} layer with ~ 4 AC pads as smallest impedance to ground

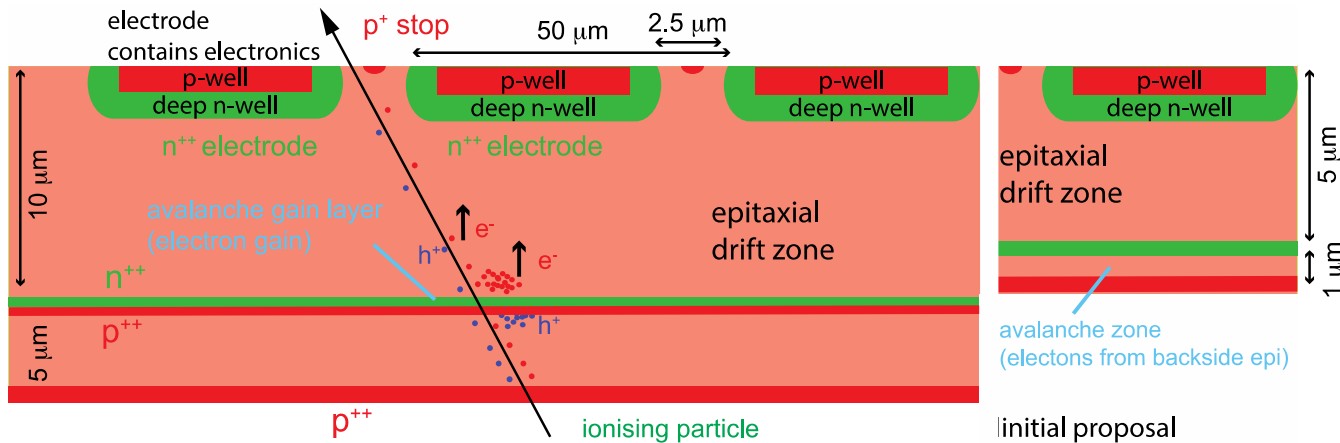
$\rightarrow 11\text{m}^2$ TOF for EiC ?






• Fresh idea; do DC-RSD

AC-coupled Low Gain Avalanche Diodes for 4D tracking: impact of electrode geometry on charge sharing – by Jennifer

• Monolith

M. Tornago et al., RD50 Workshop (2020)



- Timing goal $< 10\text{ps}$
 - Beats Landau Noise due to ultra-thin amplification zone  
- 100% fill factor,  
- $\sim 10 \mu\text{m}$ spatial resolution (small pixel)
- Fully monolithic device 
- Radiation tolerance?

First results very encouraging (IMHO great)

Btw. with this THIN thickness, one could also think about 3D connections??

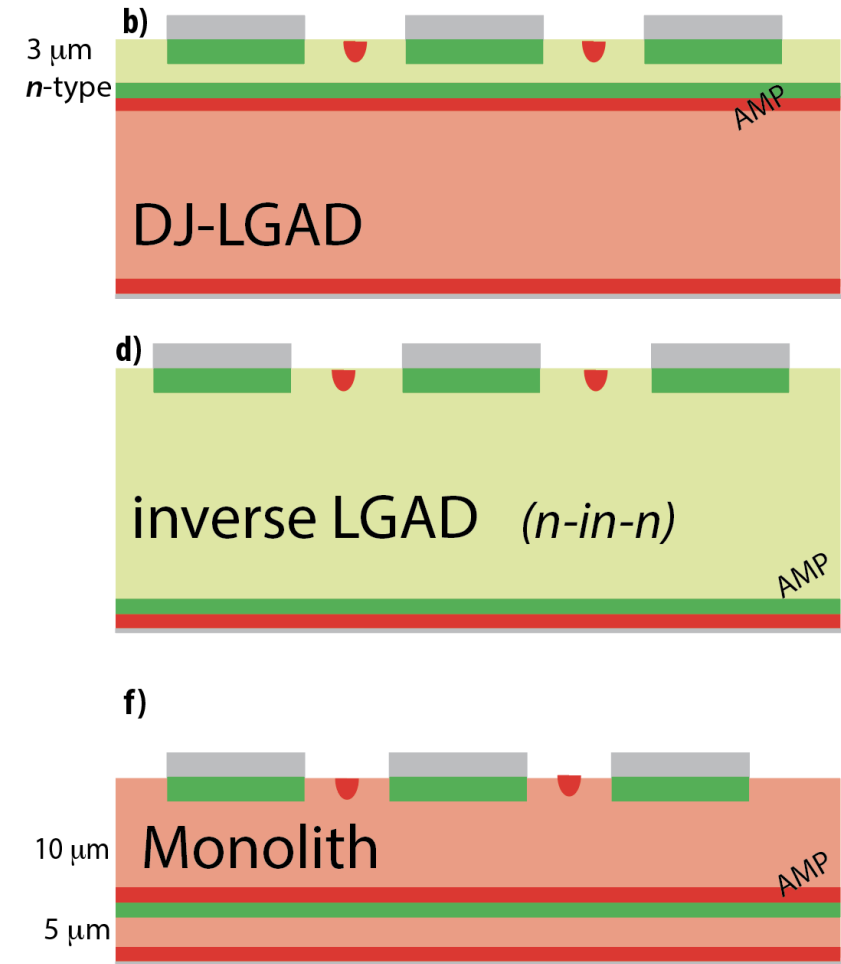
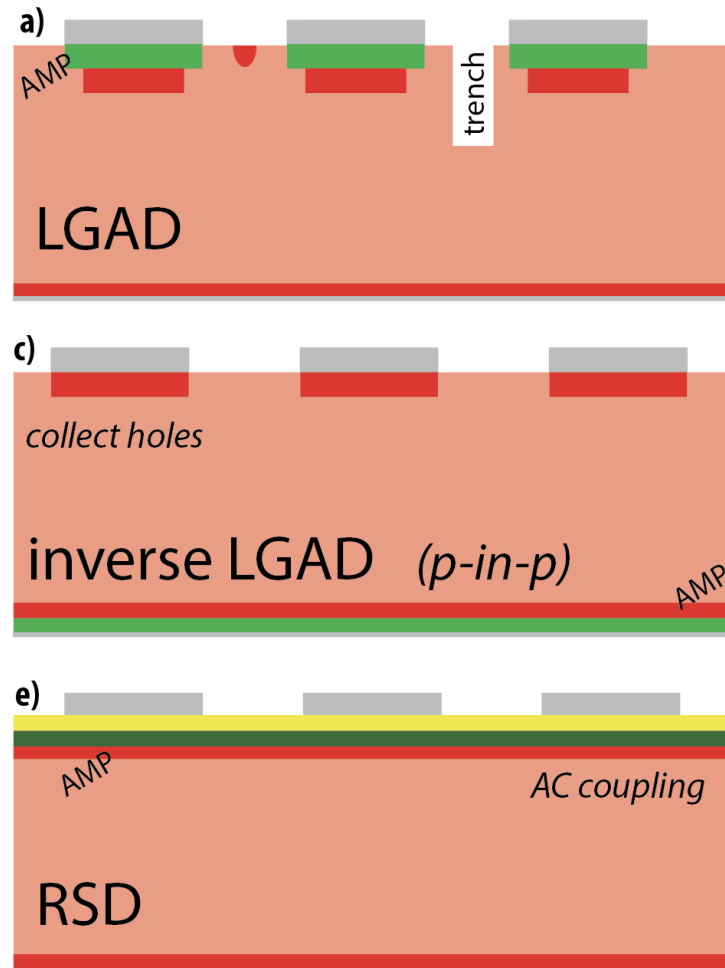


MONOLITH - picosecond time stamping capabilities in fully monolithic highly granular silicon pixel detectors – by Lorenzo

In summary, I present THE ZOO

Anybody up for a bet?

And, not to forget HV-CMOS achieving $\sigma_T = 100 - 200$ ps



or the new DC-RSD

Or the other ‘working’ philosophy

– precision timing without gain layer – 3D trenches

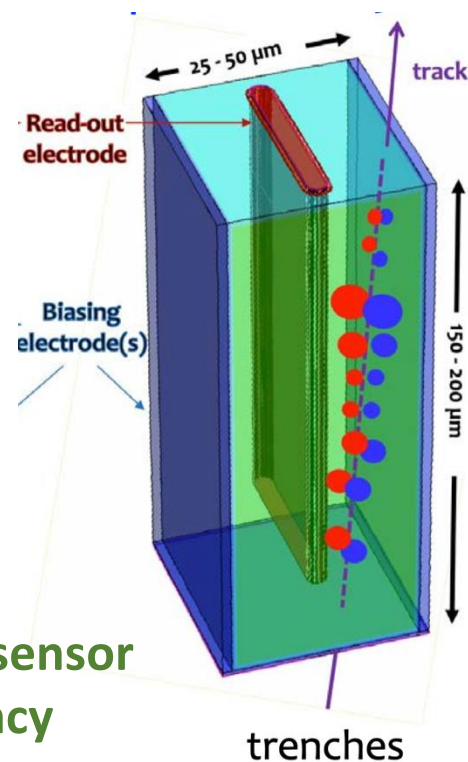
- **Simply great concept** - ‘box’ signals (perpendicular track) from electrons and holes (induction) – good amount of charge (‘thick’) – no weightfield distortion – ‘no’ landau noise

- For sure radiation tolerant

$$\sigma_t^2 = \sigma_{Time\ walk}^2 + \sigma_{Landau\ noise}^2 + \sigma_{jitter}^2 + \sigma_{Distortion}^2 + \sigma_{TDC}^2$$

Compensate in electronics electronics

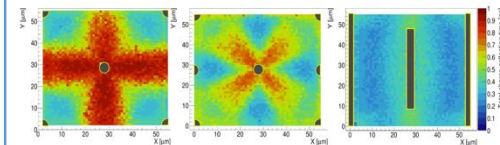
- 3D-trench
- 5x40x135μm³ trench
- 150 μm pixel depth



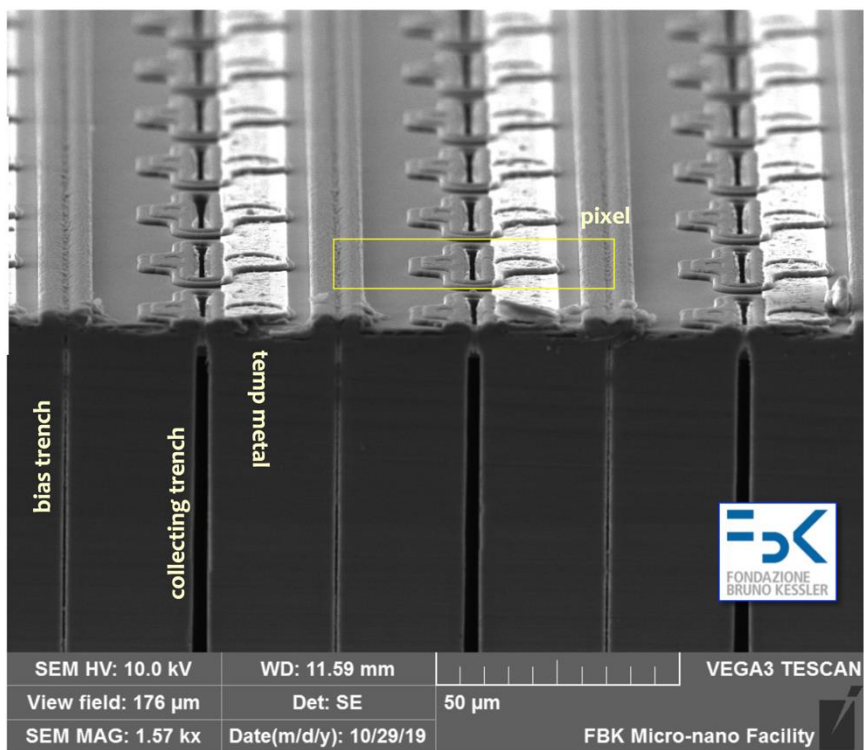
≈ 10 ps & 10 μm at sensor level at 99% efficiency
 >> 10¹⁶ neq/cm²

Adriano will probably tell us more on

- how tilting helps
- other 3D geometries



- 3D diamond
- 28nm TIMESPOT ASIC
- power and cooling challenges





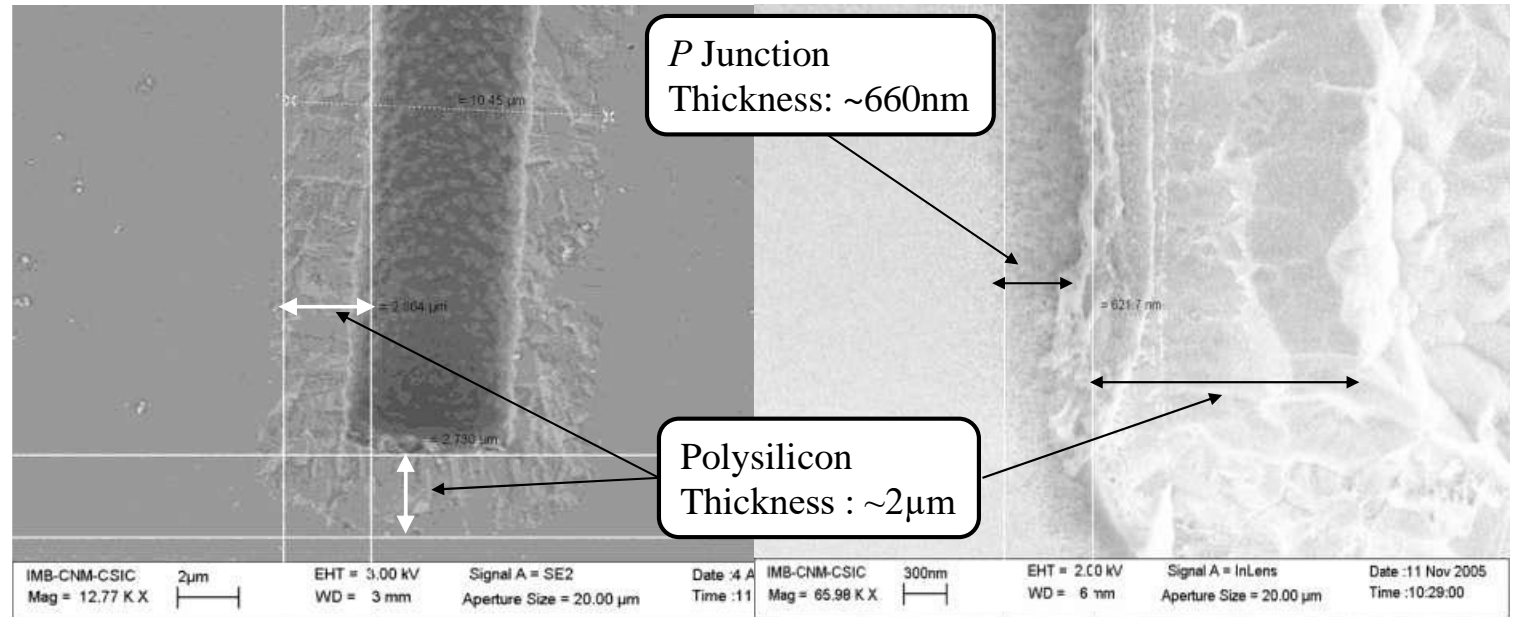
Last words on timing detectors

- Many thought, the development of silicon sensors will not see many surprises anymore
- Well, it is so good to see all these innovative ideas and their incredibly fast implementations into real devices
- **Homework:**
 - $< 5 \mu\text{m}$ spatial
 - $< 20 \text{ ps}$ (eventually 5 ps) timing
 - Monolithic
 - **Low power** ←
 - Even more for gas cooled systems
 - Radiation tolerant
 - (low cost)

3D
 Only small number
 of dedicated talks
 in this conference!
Is it a done deal?

Qualification of the first preproduction 3D FBK sensors with ITkPixV1 Martina Ressegotti
 North Ballroom, La Fonda Hotel 09:10 - 09:30

Results on 3D pixel sensors for the CMS upgrade at the HL-LHC Rudy Ceccarelli
 North Ballroom, La Fonda Hotel 17:50 - 18:10



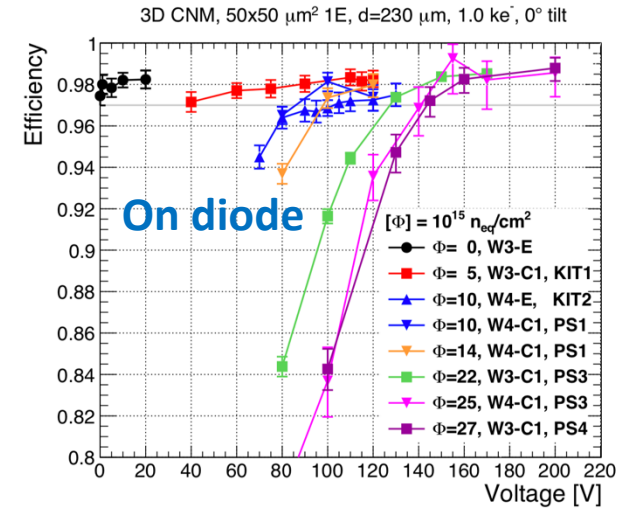
Courtesy CNM

Preaching to the Choir

preach to the choir
to speak for or against something to people who
already agree with one's opinions
www.merriam-webster.com/

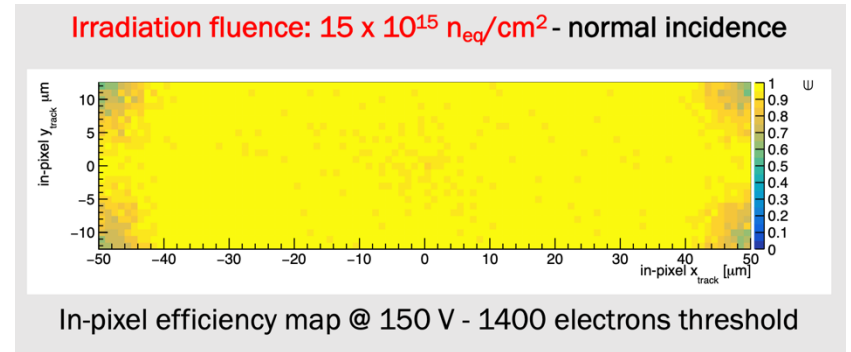
3D – facts we all know

- 3D sensors are radiation tolerant!
 - Short drift path – less trapping
 - Full thickness for signal
 - Lower depletion voltage – lower power
 - Can do slim (active) edge
- Higher Capacity
- Lower yield



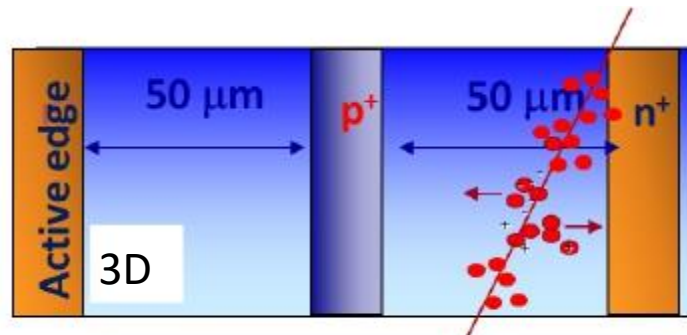
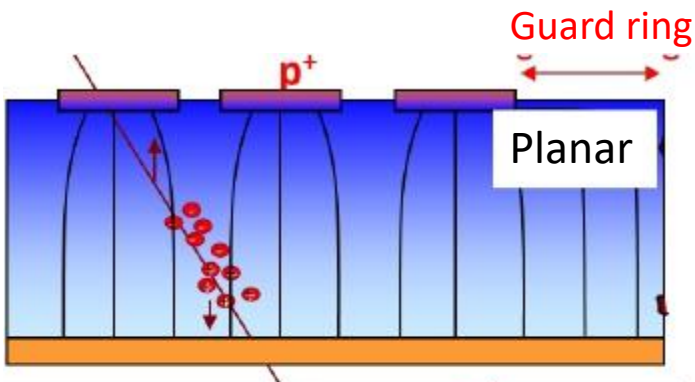
J. Lange et al 2018 JINST 13 P09009

Technology works after $3 \cdot 10^{16} n_{eq}/cm^2$

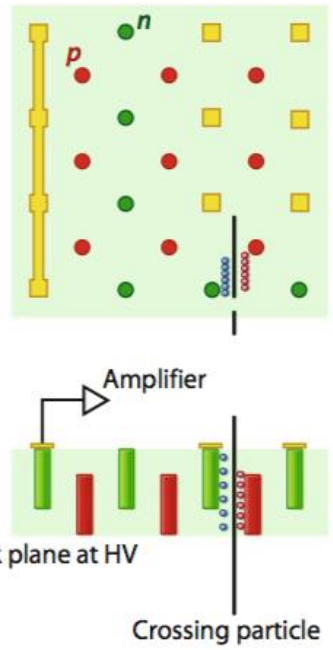
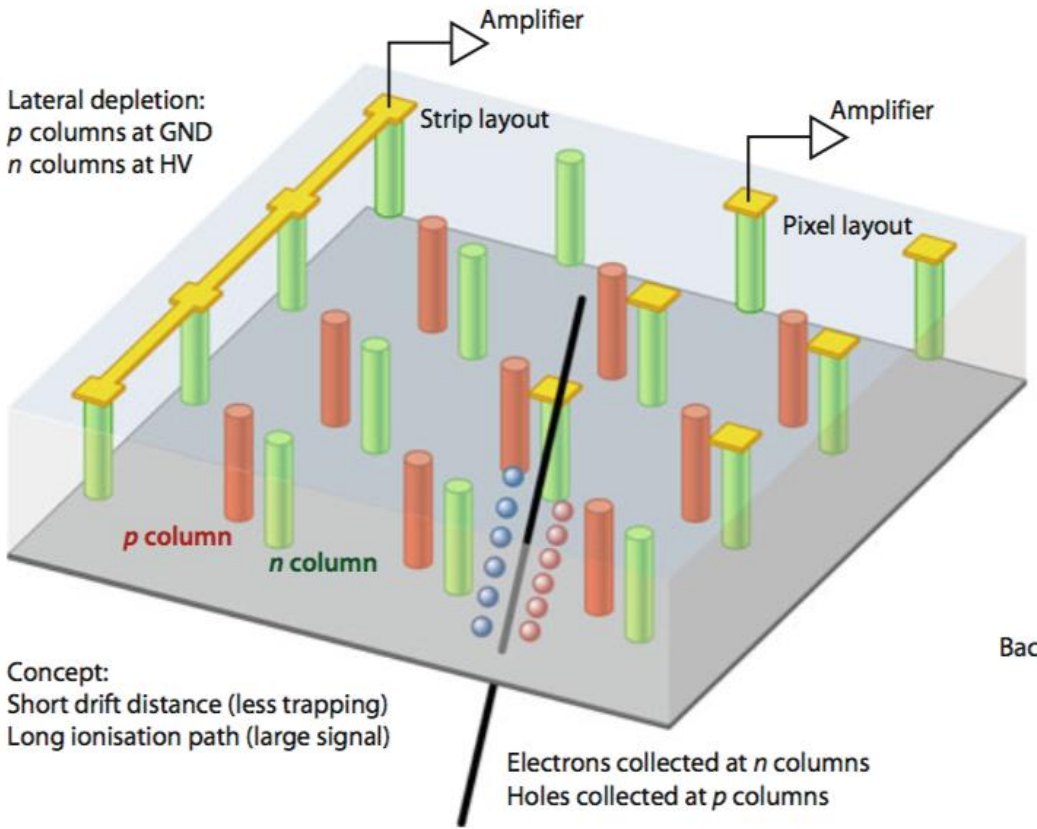


Davide Zuolo - VICI2022

- and are efficient,
and have good resolution

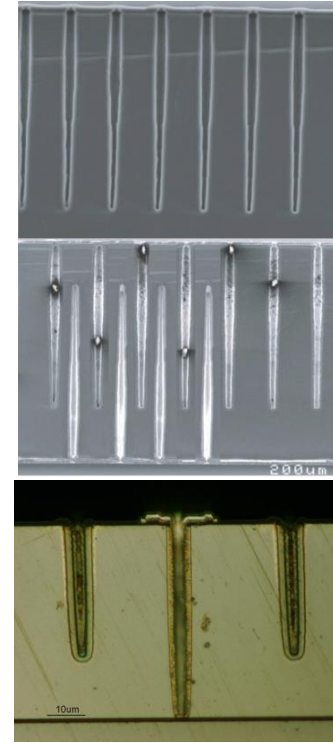


The evolution of 3D sensors



- Double or single type?
- Double or single sided?
- Full 3D-pass-through?
- Thin or thick?

- For HL-LHC we need small pixel cells - $25 \times 100 \mu\text{m}^2$
 - We need narrow columns, thus good column depth/width
 - & **medium** thickness



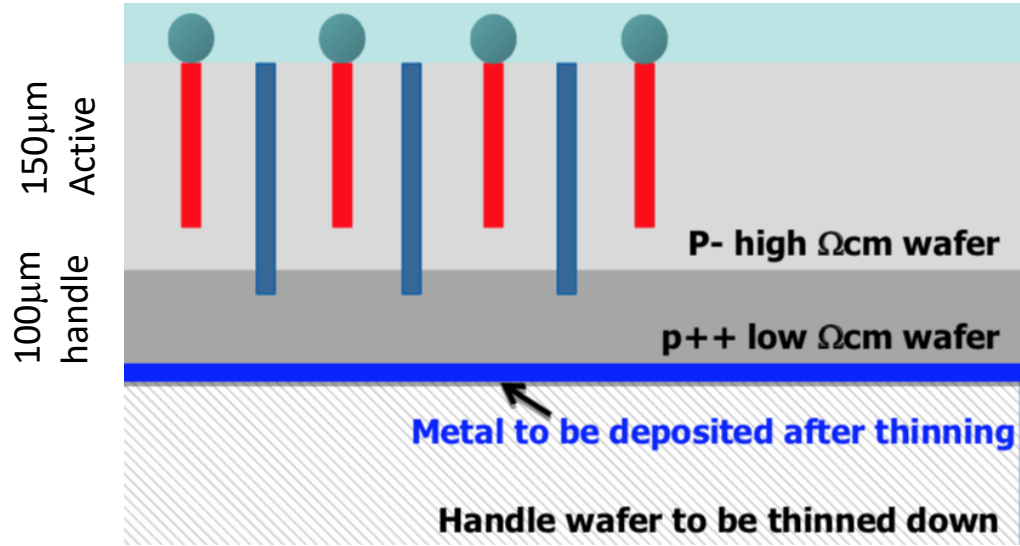
Courtesy CNM

Example double sided, double type

Tell me, but I assume nobody considers 3D for strips ...
 ... it was useful for early testing.

• What do we want later??

3D Silicon Sensors for HL-LHC – yes, we chose



Made possible by Direct Wafer Bonding (Si-Si-DWB)

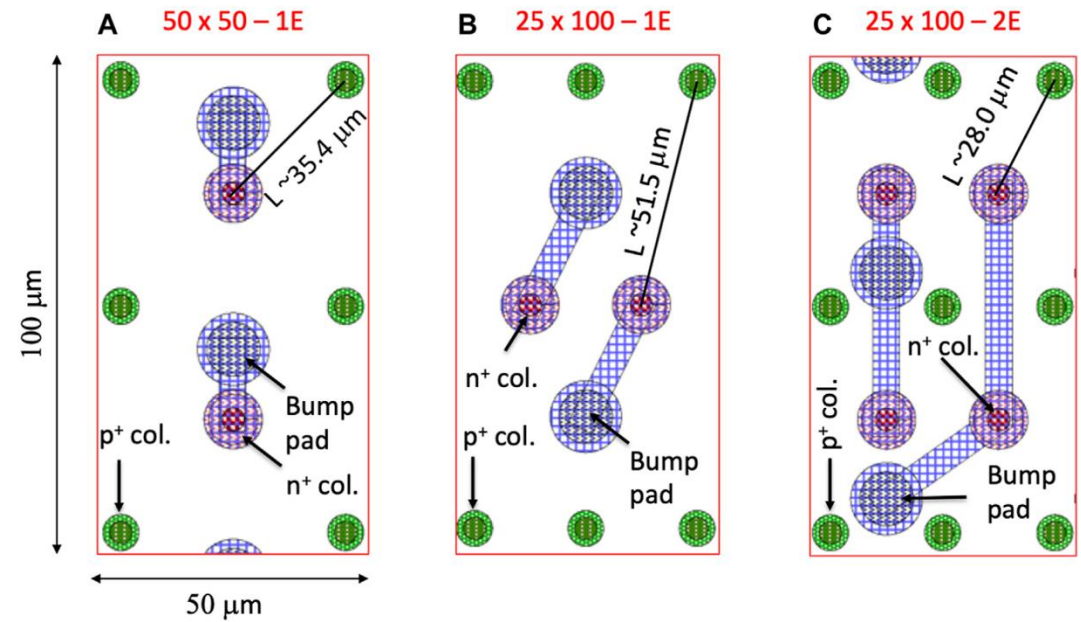


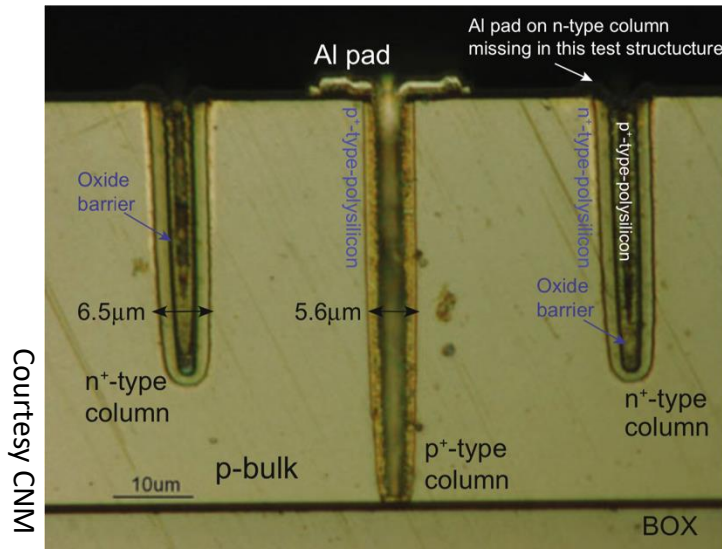
FIGURE 2 | Layouts of two adjacent small-pitch 3D pixels of different geometry for the ATLAS and CMS upgrades at HL-LHC: 50 μm × 50 μm-1E (A), 25 μm × 100 μm-1E (B) and 25 μm × 100 μm-2E (C).

Technology, thickness and cells chosen!

We are quarrelling a bit with noise these days at $\Phi > E16$ and higher voltages

For the future we might like smaller cell sizes (e.g. 25x25 mm²):

- Even shorter drift paths – even more radiation tolerant?
- Higher occupancy
- Tune charge multiplication, already at lower voltages?



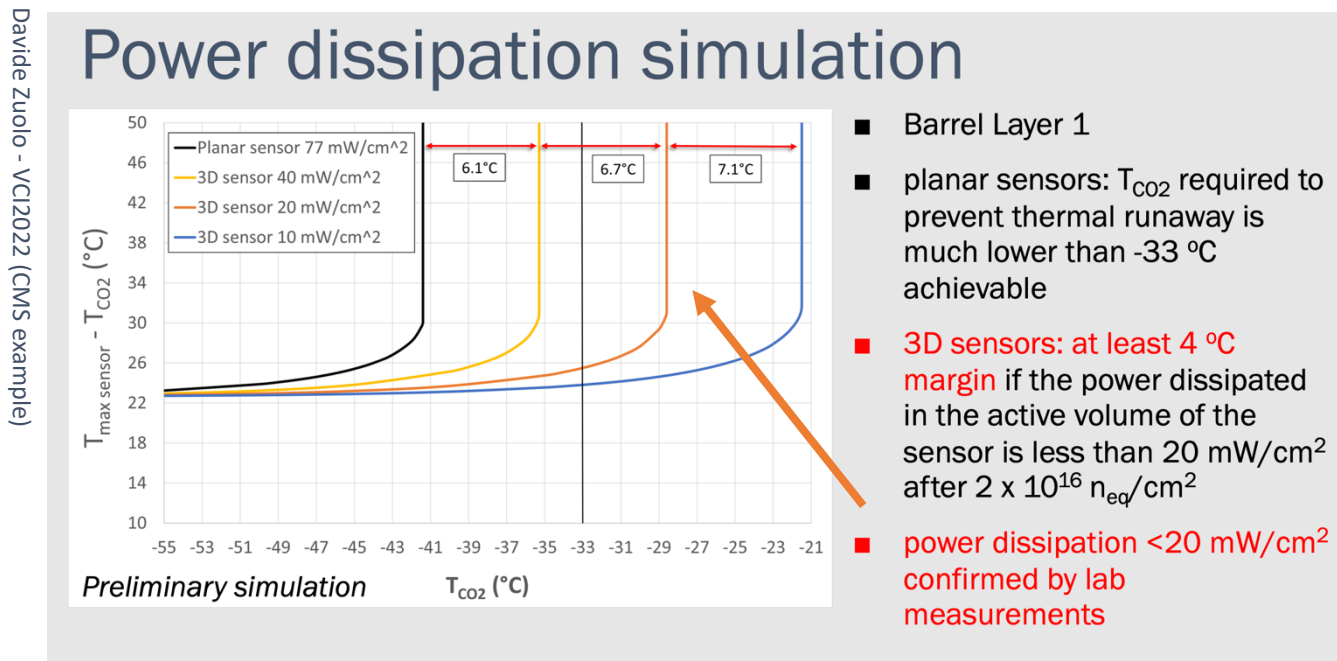
Courtesy CNM

Close to this one...

3D, in the end, do we do it for the radiation tolerance?

(used in ATLAS IBL, AFP, CMS PPS; to be used Phase-2 ATLAS & CMS inner layer)

- The goal of radiation tolerance is around $1-2 \cdot 10^{16} \text{ 1MeV}_{\text{eq}}/\text{cm}^2$
- In principle planar pixels can do this ...
 - Resolutions $\sim 5 \mu\text{m}$ and efficiencies (98-99%) are very similar (*probably equal*)
- I guess, we do it due to power and to prevent corresponding thermal runaway (at minimal cooling contact)
 - Depletes at much lower voltage



More in

Qualification of the first preproduction 3D FBK sensors with ITkPixV1
– by Martina

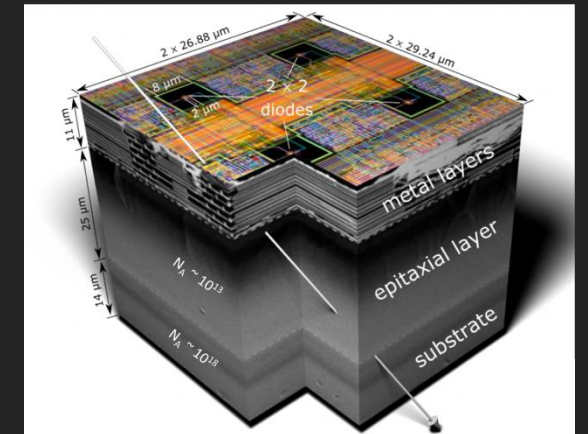
Results on 3D pixel sensors for the CMS upgrade at the HL-LHC
– by Rudy

Monolithic CMOS

some call it
HV-CMOS or HR-CMOS
some call it DMAPS
I call it exciting!

And in my very **personal** humble
opinion it must be fully **monolithic***

And getting all logic in and cope
with high rates will be a challenge --
experiencing the struggle to get all
ATLAS and CMS needs into the
65nm pure pixel ASIC (RD53)



CMOS Sensors for the Subaru Telescope North Ballroom, La Fonda Hotel	Satoshi Miyazaki 17:15 - 17:35
X-ray polarization measurements with CMOS for satellites North Ballroom, La Fonda Hotel	Hirokazu Odaka 17:35 - 17:55
CMOS pixel sensors for ULTRASAT North Ballroom, La Fonda Hotel	Steven Worm 17:55 - 18:15
AstropPix: Status and Outlook of Monolithic Active Pixel Sensors for Future Gamma-ray Telescopes North Ballroom, La Fonda Hotel	Dr Regina Caputo 18:15 - 18:35
Extremely high density and position resolution digital pixel sensors North Ballroom, La Fonda Hotel	Gianluigi Casse 18:50 - 19:10
Pixel detector developments for future lepton colliders North Ballroom, La Fonda Hotel	Domink Dannheim 19:10 - 19:30
ATLASPIX3 modules for experiments at electron-positron colliders North Ballroom, La Fonda Hotel	Prof. Attilio Andreazza 19:30 - 19:50
T3-MALTA North Ballroom, La Fonda Hotel	Valerio Dao 19:50 - 20:10
LF-Monopix2 North Ballroom, La Fonda Hotel	Patrick Breugnot 20:10 - 20:30
Depleted monolithic active pixels sensor in 180nm TowerJazz CMOS technology with column drain readout architecture Christian Bespin	
A derivation of the electric field inside MAPS detectors from beam-test data and limited TCAD simulations North Ballroom, La Fonda Hotel	Arka Santra 14:10 - 14:30
From vertex detectors to applications in ion detection and spectrometry: a glimpse of MAPS R&D in Strasbourg Jerome Baudot	
Optimization of a 65 nm CMOS imaging technology for monolithic sensors for high energy physics North Ballroom, La Fonda Hotel	Walter Snoeys 14:50 - 15:10

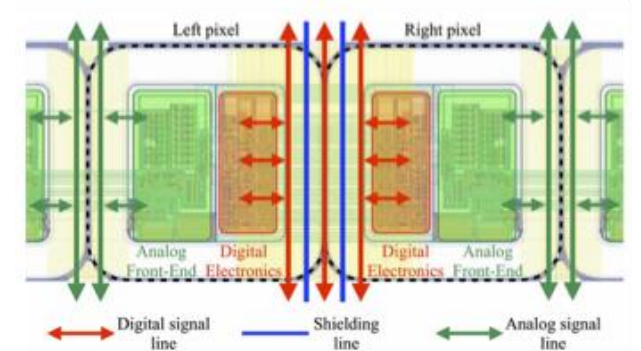
Stating the Obvious

What we all know – Advantages of HV-CMOS



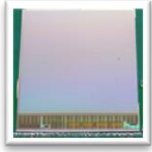
Stock.adobe.com

- Thin
 - Low material budget: $X/X_0 \sim 0.05\%$
 - Radiation tolerant (also 'collects' electrons): $\Phi > 10^{15} \text{ MeV}_{\text{eq}}/\text{cm}^2$
- Low power
- No bump bonding – cost saving, easier logistics
- In-cell processing – monolithic
- Small cells ($10 \times 10 \mu\text{m}^2$) – high resolution $\sim 3 \mu\text{m}$
- Challenges:
 - Stitching
 - How much digital parts features fit in a pixel (and how much in chip periphery)?
 - timing, buffering, L1, data handling - state machine

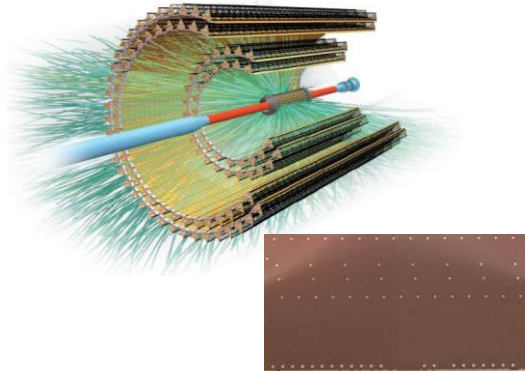


From RD50 talk

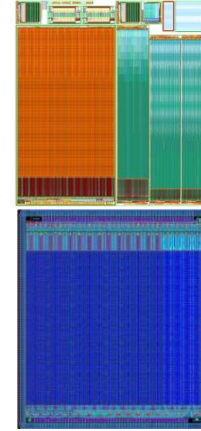
MAPS Monolithic Active Pixel Sensors



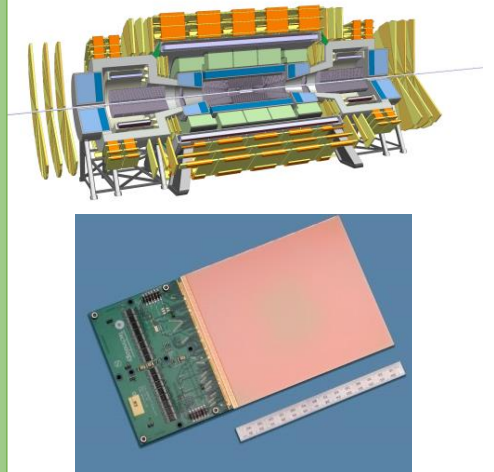
ULTIMATE in STAR
First HEP MAPS
system



ALPIDE in ALICE
First MAPS with sparse
readout similar to hybrid
sensors
Chip-to-chip
communication for data
aggregation



Recent developments
(ATLAS, ALICE, MU3e, etc.)
Depleted radiation hard
MAPS with:
'high' voltage
Sparse readout
Chip-to-chip communication
Serial power



FCC, e⁺e⁻ collider, ...
Large stitched fast
radiation hard MAPS with:
Sparse readout
Chip-to-chip communication
Serial power, timing
... many more
12", <65nm?,
new read-out schemes?

Many more in between, some to be discussed this week

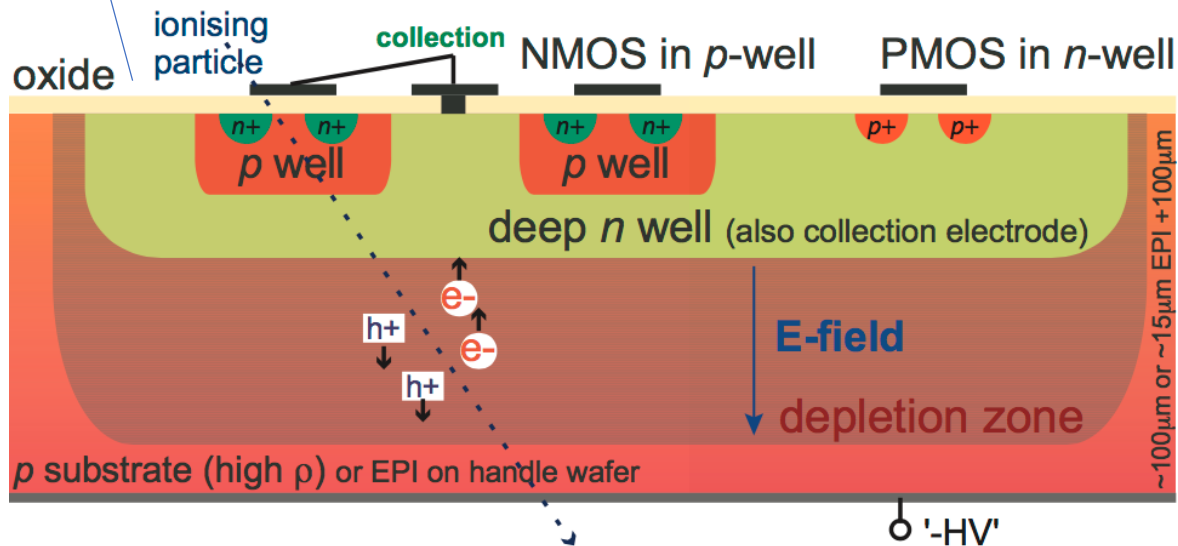
Important steps in
every iteration

Many uses: STAR, ALICE, CBM, NICA MPD, sPHENIX, Mu3e, CSES – HEPD2, Medical, ...
candidates for LHCb, PANDA, BELLE-2, EiC ... ~ well everybody

Nodes being used: 180, 150 and 65 nm technology and 130 nm SiGe BiCMOS

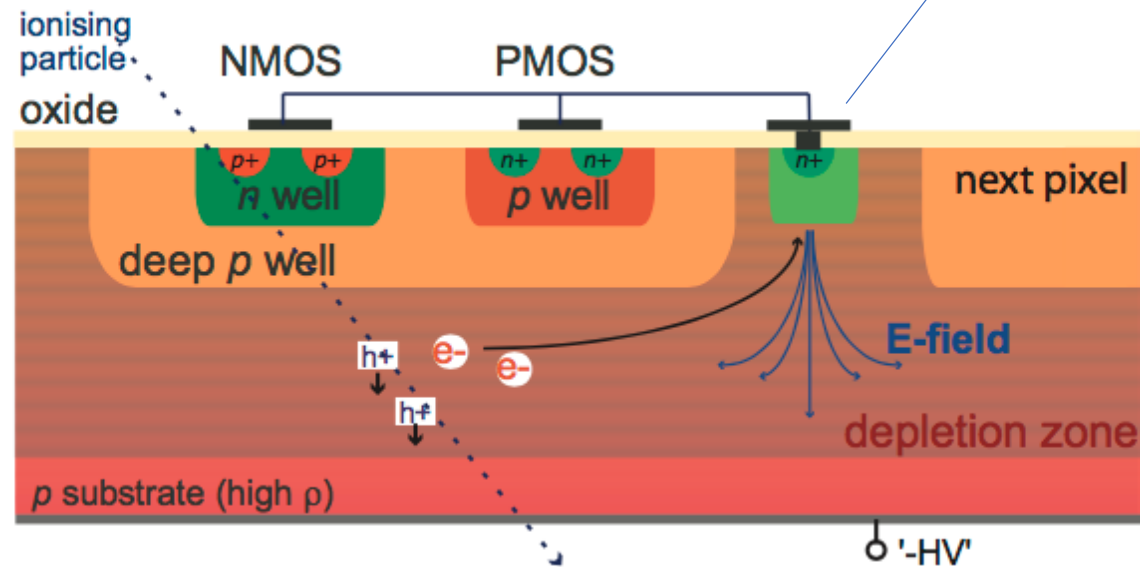
LARGE or SMALL electrode??

e.g. 50-60 μm (for RD50)



- Short drift path (faster 'collection')
- High C - higher noise $O(100 e^-)$
- Homogeneous weighting field
- High homogeneous electrical field
- E.g. MUIPX, RD50, MONOLITH, LF-MONOPIX, ATLASPIX

e.g. 3 μm (for Malta)



- Long drift path
- Very low C - reduced noise ($\sim 10 e^-$ & low power)
- δ weighting field – arrival
- Some adaptations help further
- E.g. ALPIDE, MALTA, TJ-MONOPIX. CLICTD, FASTPIX

LF-Monopix2 – by Patrick

Where can we have more real estate for CMOS circuitry?
 Radiation tolerance – we are around $> 10^{15} \text{ MeV}_{\text{eq}}/\text{cm}^2$ — is LARGE better?

TJ-MALTA - by Valerio

SMALL CELL HV-CMOS EVOLUTION

To overcome:

- Lateral depletion
- Direct drift to to small electrode
 - Mind δ weighing field

Achievements

- Thresholds $\sim 100 e^-$
- Noise $\sim 10 e^-$

TJ-MALTA - by Valerio

E.g. ALPIDE, MALTA, MONOPIX, CLICTD, FASTPIX

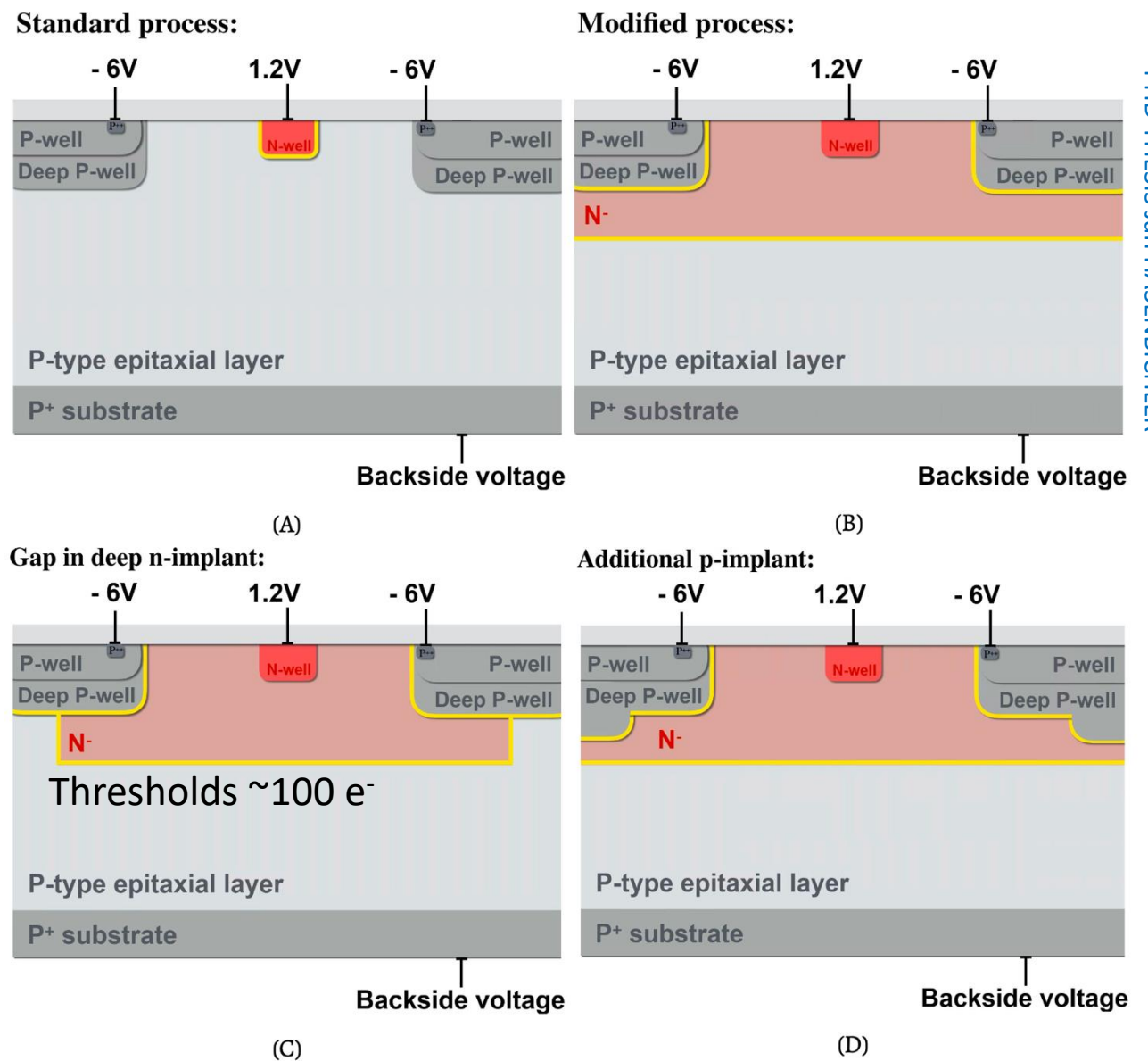
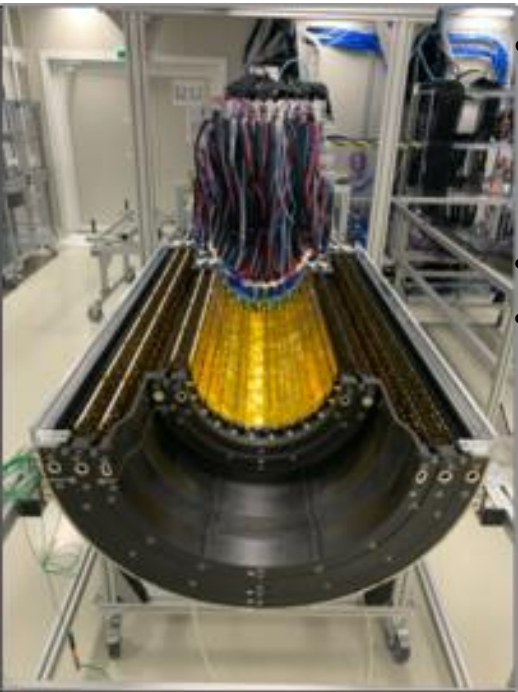


FIGURE 9.1: Four different pixel flavours are shown [119]. (A) shows the standard flavour which was used in ALPIDE. (B) shows the modified flavour which features a blanket deep n-implant. (C) shows the gap flavour which leaves a gap in the deep n-implant. (D) shows the extra-p flavour which features an extra deep p-implant. The junction is represented in yellow. The voltages are the ones used in this chapter. All the drawings are not to scale.

The 'big' Small Cell example of MAPS - ALICE

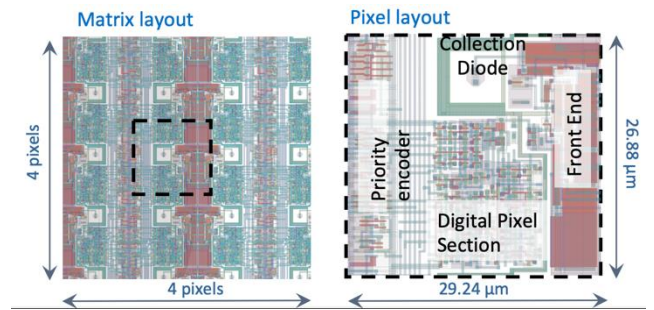
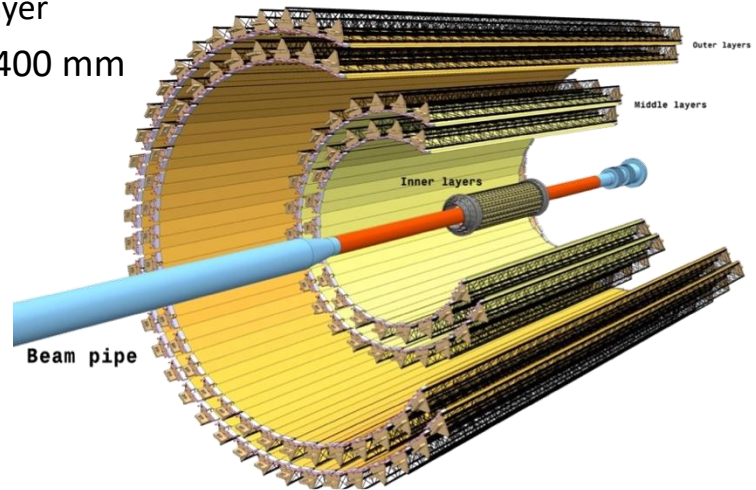


LS2: 3+4 layers of MAPS (CMOS) ~10m²

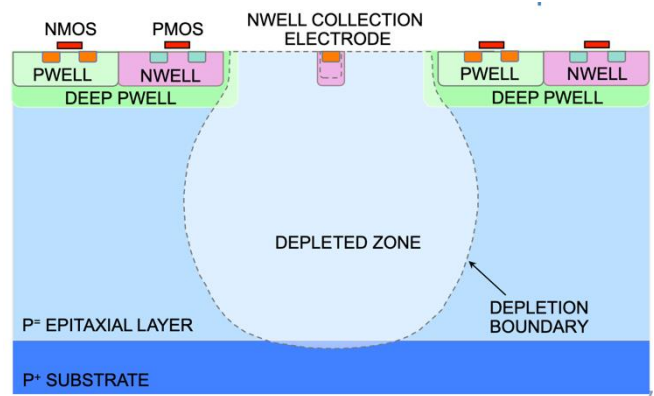
- 27x29 μm² pixels - **12.5 G-pixels**
- MAPS thinned to 50 μm
 - ~0.3 % X₀ per layer

Radial coverage R= **21** - 400 mm

Limited voltage ~3V



ALICE ITS Upgrade TDR CERN-LHCC-2013-024

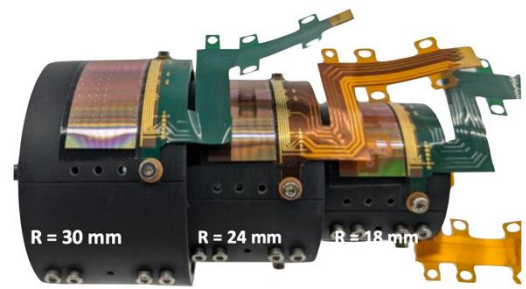


MAPS

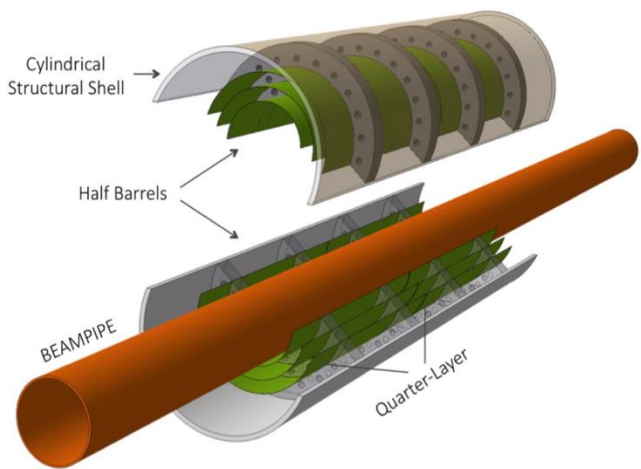
Future: ALICE upgrade (ITS3) – HR/HV CMOS

- Push technology further: **thinner**, large sensors through stitching
- Faster signal, more radiation hard
- Pixel sizes 10x10μm² → 3μm position resolution
- X/X₀ per layer 0.05%
- **CURVED**

In test beam
Bent ALPIDE



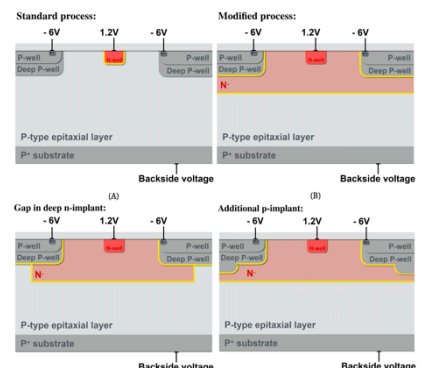
Vertex 2022 Lukas Lautner



Truly cylindrical vertex detector

ALICE-PUBLIC-2018-013

Let's see, which option they will chose?



DMAPS

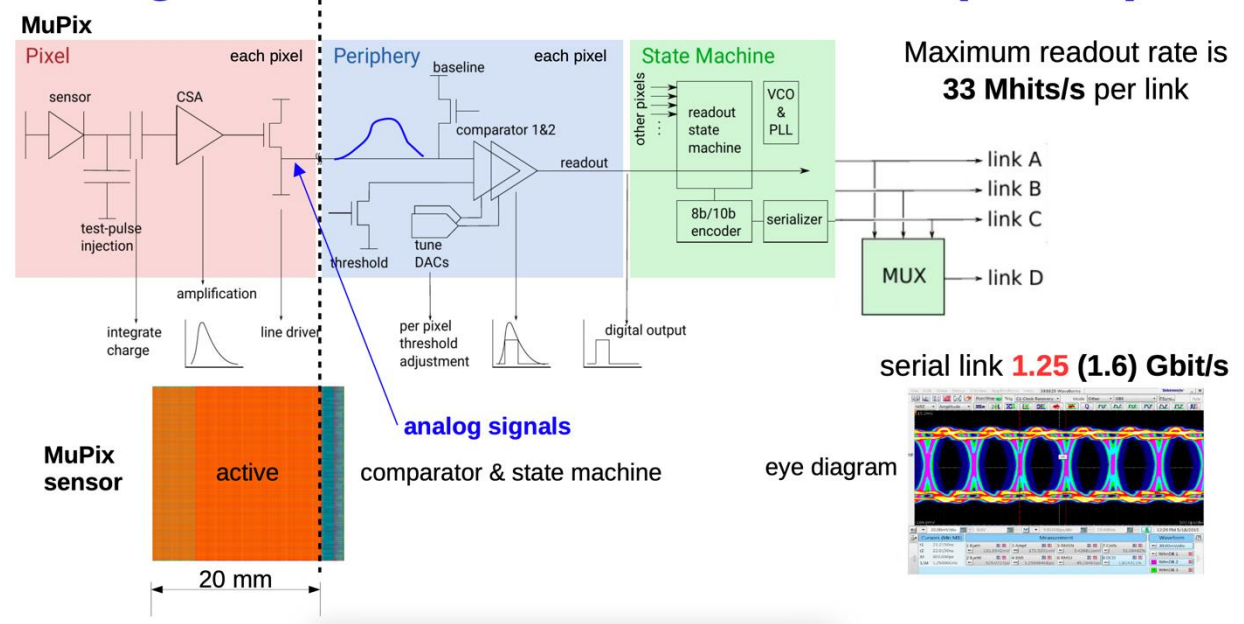
Mu3e – Another wonderful example on HV-CMOS

Big Cell approach - MUIPIX

$x/X_0 = 0.0005$ per layers

Mupix10 mockup with O(100) sensors installed in integration run at PSI (2021)

High Rate & Continuous Readout (MuPix)



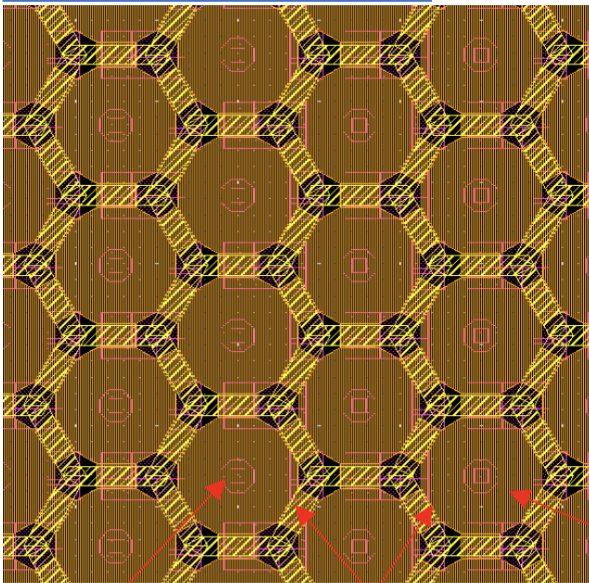
Full monolithic – great example!

- Phase-1: 6 layers (50mm thin and cooled by gaseous helium (up to 400 mW/cm²))

HEP starts to like hexagonal structures – approximate circle!

- Collection electrodes on hexagonal grid
- Charge sharing in the corners between 3 pixels instead of 4
 - Smaller cluster sizes, increase of seed signal -> more margin
- Electrode distance to edges similar boarder improves time resolution - Homogeneous drift field
- Reduce breakdown (minimise edge effects)

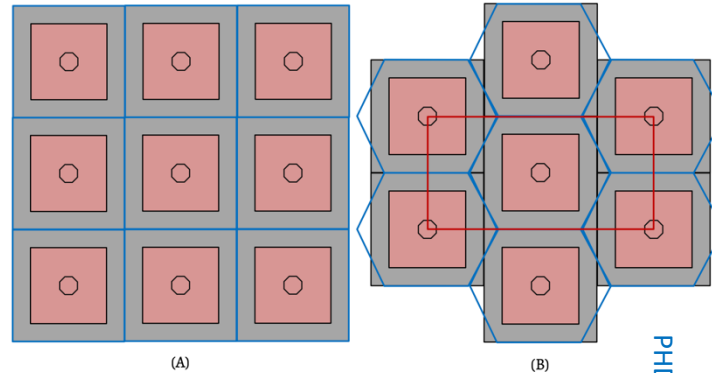
FASTPIX (small cell)



n-well
electrode

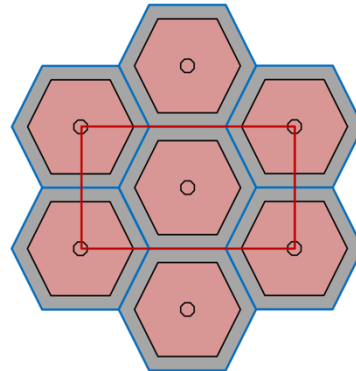
extra p-type
implant

low-dose
n-type
implant



(A)

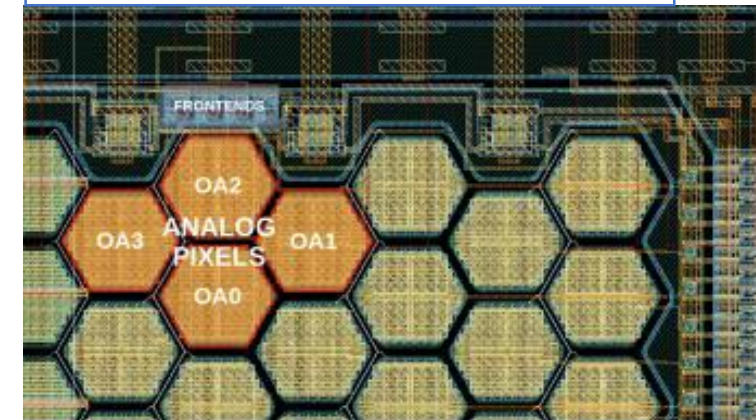
(B)



(C)

PHD THESIS Jan HASENBICHLER

PICOAD/MONOLITH (large cell)

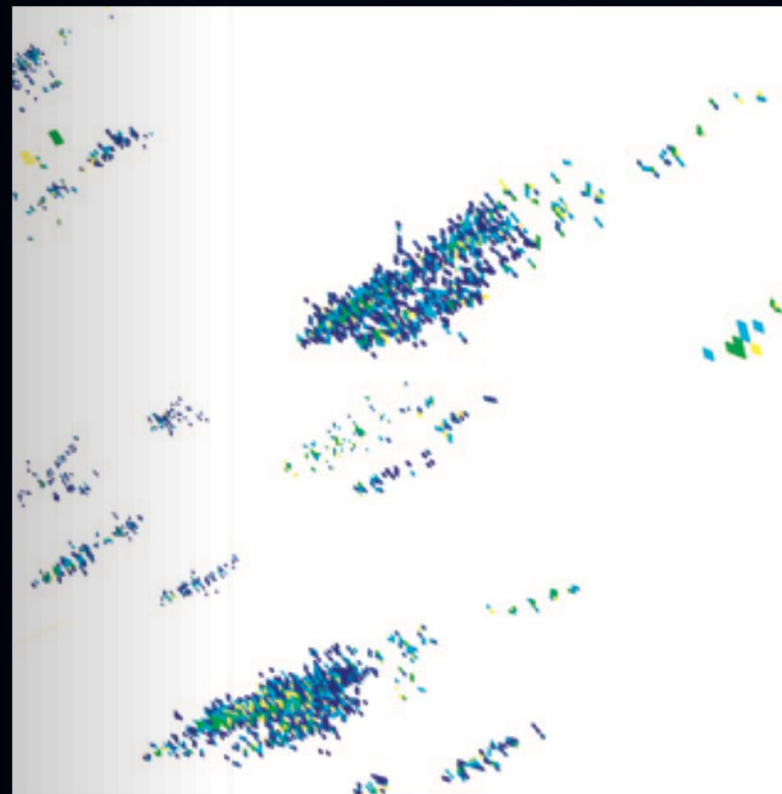
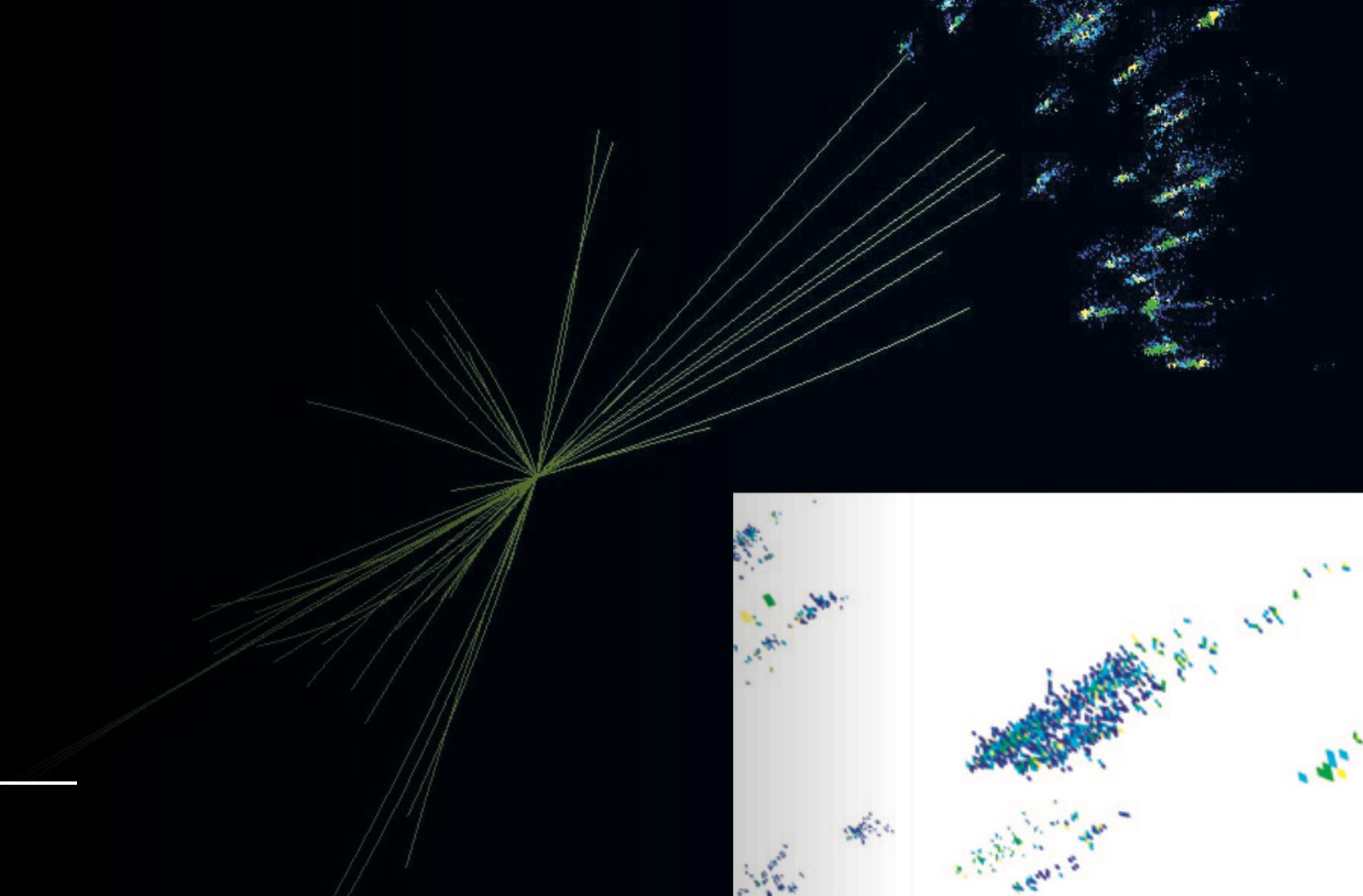


MONOLITH



That's it

Soon, we also 'track' inside calorimeters

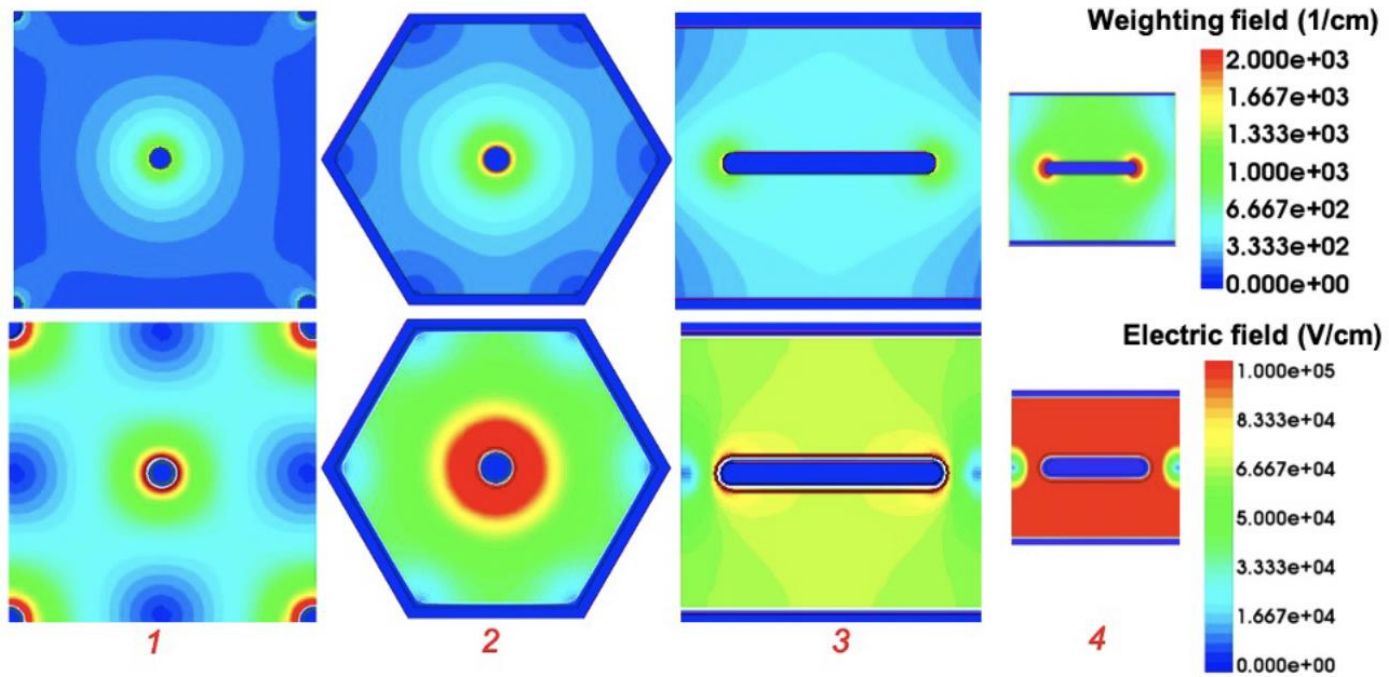


I love this incredibly lively field of sensor and detector system development.

And, it will be a great pleasure to talk to you later

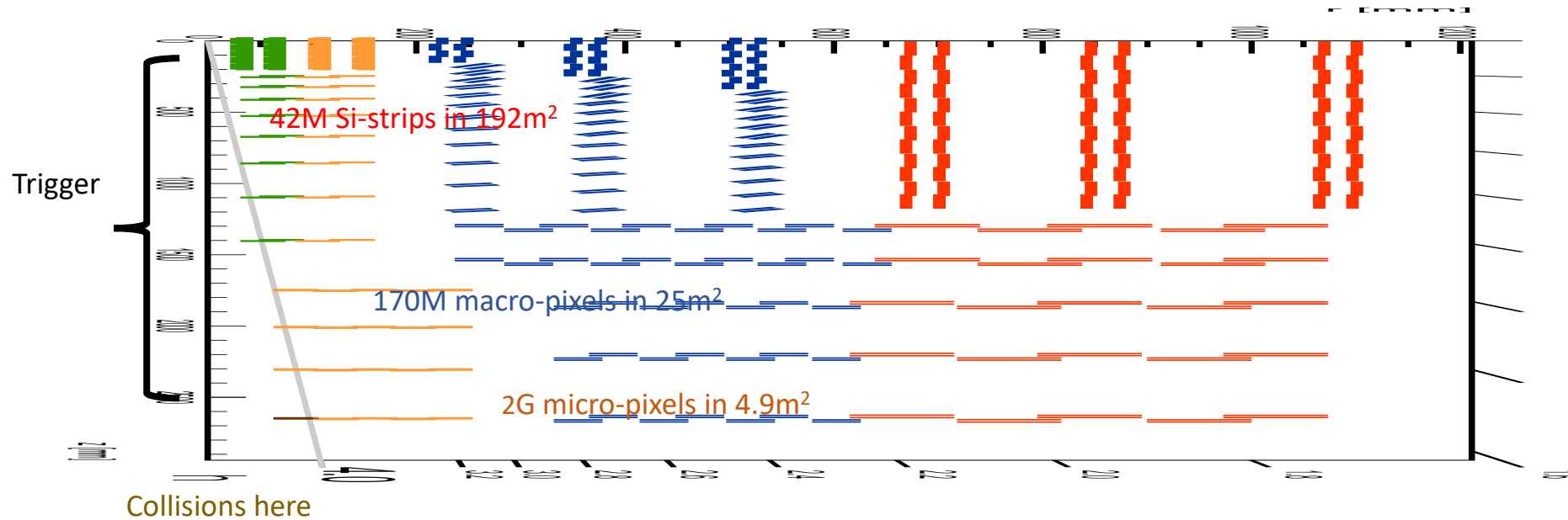
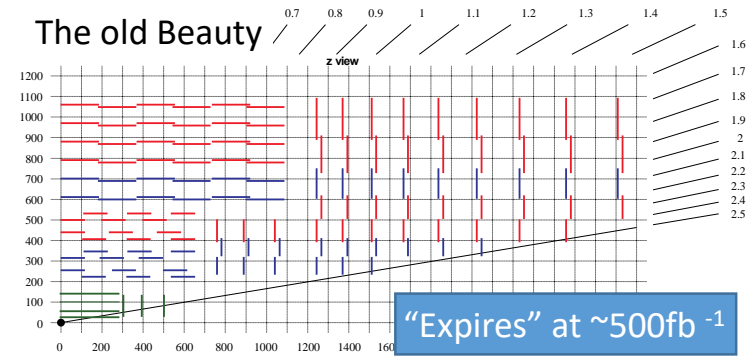
Only problem, such meetings animate me to stop doing managerial work and to go back having fun in the lab.

BACKUP



The new Beauty

- Outer Tracker design driven by ability to provide tracks at 40 MHz to L1-trigger ($p_T > 3\text{GeV}$)
 - World's first
- Tilted modules in three OT layers
- Inner Tracker (pixel) extend coverage to $\eta \approx 3.8$



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