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Precision timing with silicon detectors

G. KRAMBERGER

JOZEF STEFAN INSTITUTE, LJUBLJANA

thanks to the input from many colleagues who filled my knowledge gaps …

Much of the material was already shown by Frank, but some repetition doesn’t hurt

Timing detectors

- T. Pajero VELO Upgrade II- the LHCb 4D Pixel Detector

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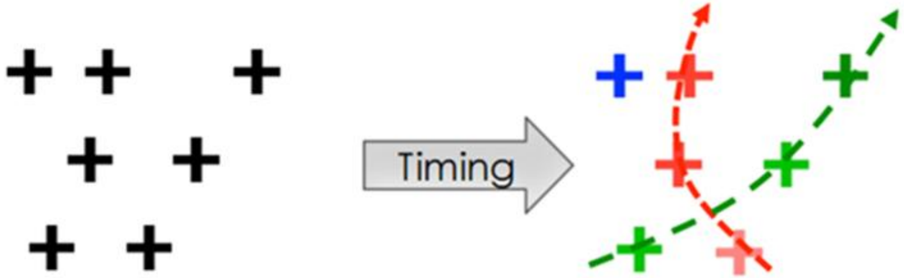
Timing with silicon detectors:

- Track timing (near future: HGTD, ETL) – assign the “time stamp” to the track – no need for superb spatial resolution.
- 4D tracking (more distant future) where each hit has superb position (~few μm) and time resolution (~30 ps)



better reconstruction, less CPU, effectively more luminosity

Particle physics is the key driver in designing and developing those technologies, but there are applications outside HEP:

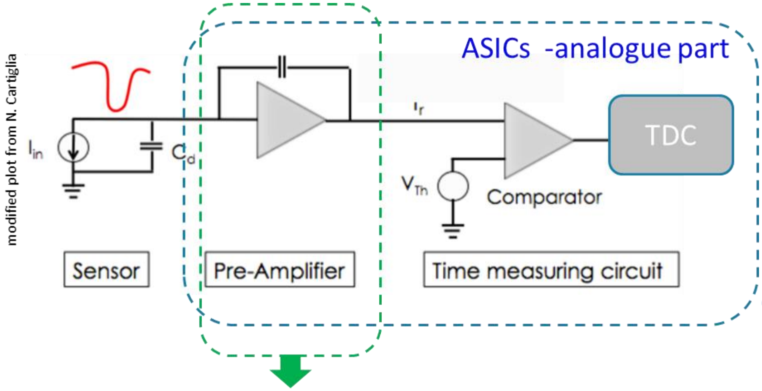
- Medical imaging (proton – CT)
- Therapy monitoring (determination of proton range during therapies)
- Particle counting beam monitors in cancer therapies

Post LS3 LHC ($\Phi_{eq}>10^{16}$ cm^{-2})

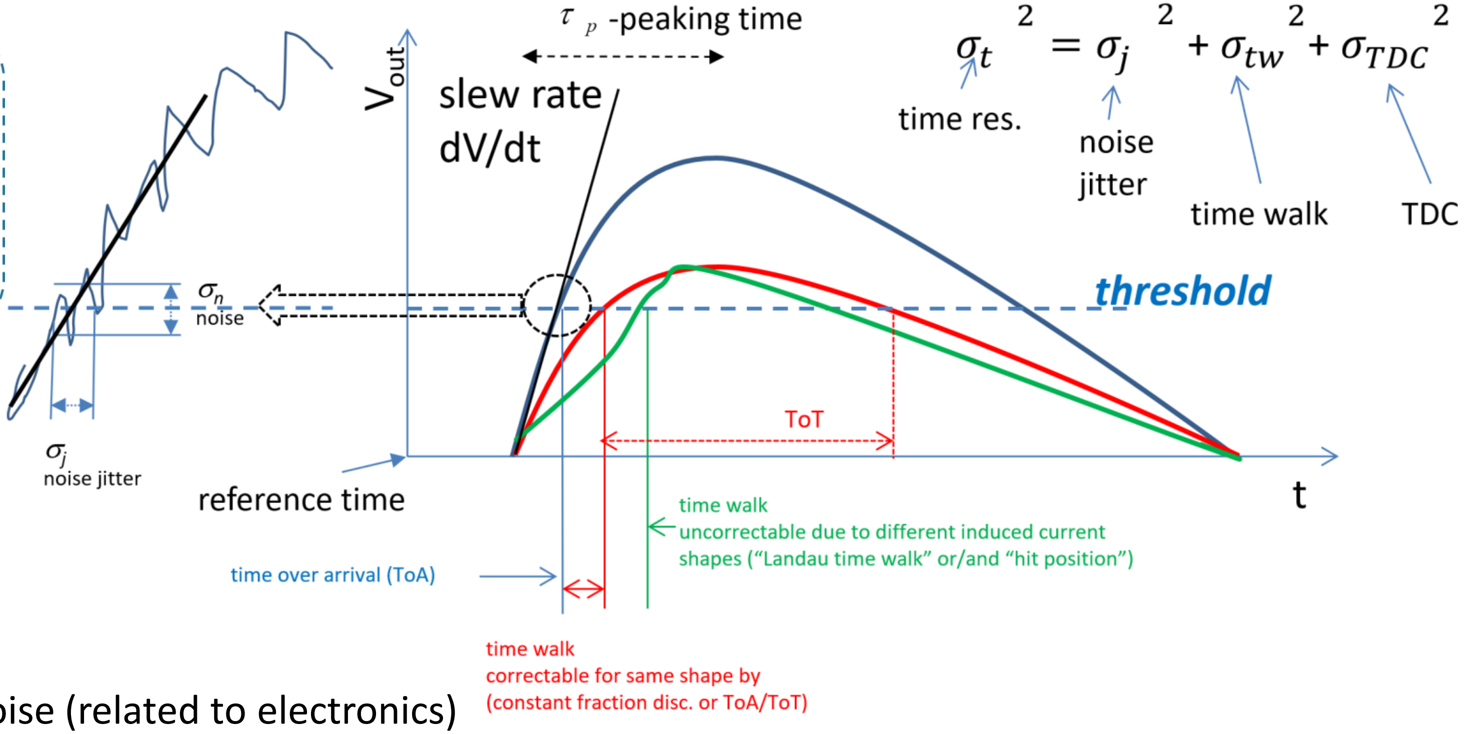
- LHC-B Velo II upgrade (>LS4)
- CMS – Forward Pixel (LS >4,5)
- ATLAS - HGTD/Pixel (LS >4,5)

FCC-hh – with really demanding challenge of track time resolution of ~5 ps

Time resolution



$$\sigma_j = \frac{\sigma_n}{\left|\frac{dV}{dt}\right|} \approx \frac{\sigma_n}{\left|\frac{S}{\tau_p}\right|} = \frac{\tau_p}{S/N}$$



$$\sigma_t^2 = \sigma_j^2 + \sigma_{tw}^2 + \sigma_{TDC}^2$$

- σ_j -jitter – fast rise time and high signal/noise (related to electronics)
- σ_{TDC} – vey good granularity is a challenge for ASIC

σ_{tw}-time walk component includes σ_{wf} , σ_{lf} , σ_{Q}, :

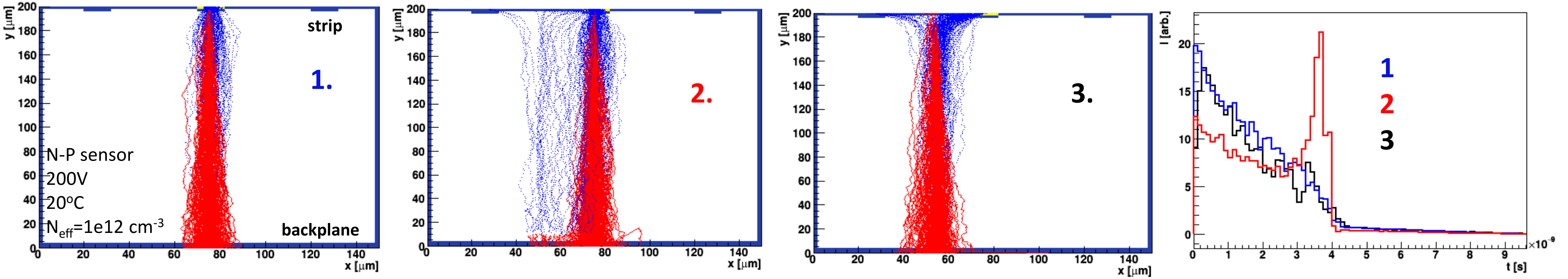
$$\boxed{\sigma_{tw}^2 \approx \sigma_{wf}^2 + \sigma_{lf}^2} + \xcancel{\sigma_Q^2}$$

- σ_Q - fluctuations in amount of deposited charge –> correctable with ToA-ToT or CFD (not trivial !)
- σ_{lf} - Landau fluctuations in shape of the signal -> depends on **hit position** (segmented devices)
- σ_{wf} / σ_{un} – weighting/electric field contribution (distortion component/un-perfection) -> depends on **hit position** in segmented devices

Time resolution

Example of 3 tracks hitting the same pixel/strips and depositing the same amount of charge, but with different induced currents!

(non-correctable time walk – will determine the limits of time resolution)



Landau fluctuations

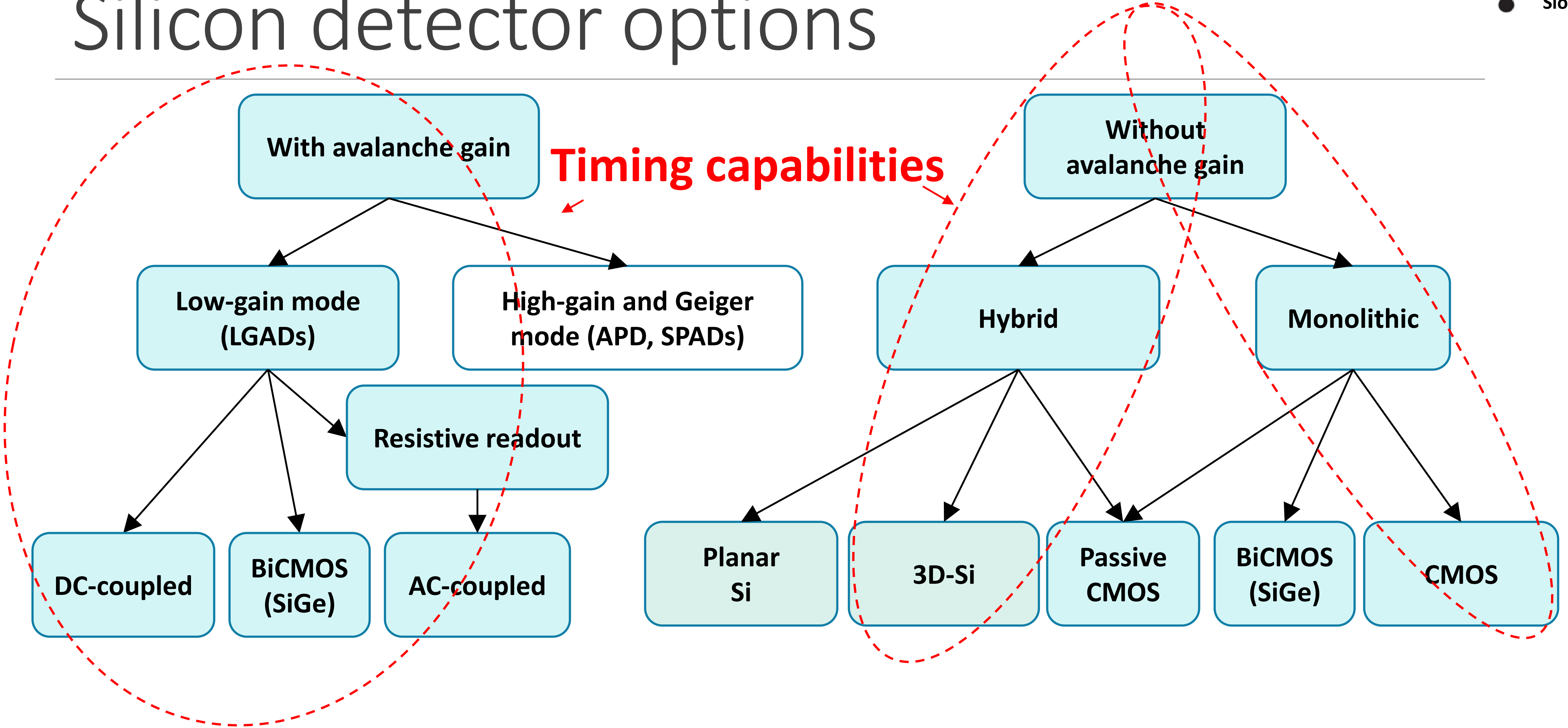
Distortion due to E_w

“Ideal” timing detector:

- Huge signal (small jitter)
- No gain (small σ_{lf})
- Simple electrode geometry (small σ_{wf})
- Short collection distance (small jitter, σ_{tw})
- Low capacitance (jitter/noise and power)

These requirements are mutually excluding, therefore any design should be tailor to the application. There is no one type-fit-all sensor.

Silicon detector options



The 2021 ECFA detector research and development roadmap

http://cds.cern.ch/record/2784893/files/Synopsis%20of%20the%20ECFA%20Detector%20R%26D%20Roadmap.pdf?version=1

Link to the CERN council approved implementation plan for detector R&D roadmap.

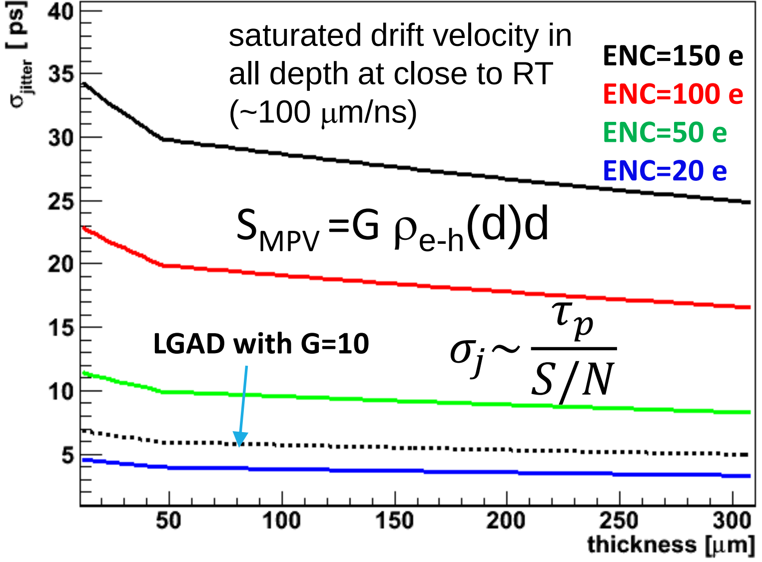
https://indico.cern.ch/event/1197445/contributions/5034860/attachments/2517863/4329123/spc-e-1190-c-e-3679-Implementation_Detector_Roadmap.pdf

Limits for planar sensors

**NA62, NIM A958 (2020) 162127*
***ATLAS HGTD TDR*
**** UCSC data*

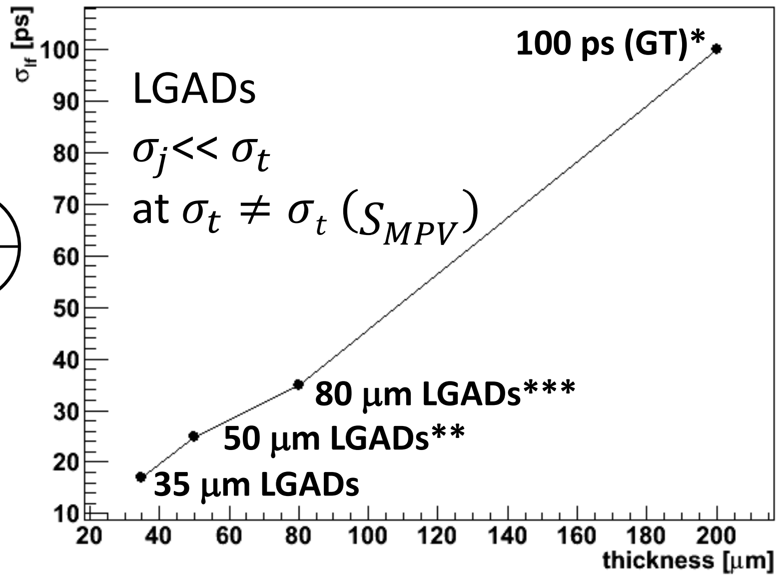
Planar sensors: NA62 giga-tracker (200 μm, p-n, TDCPix, 300x300 μm^2)*: σ_j~80 ps, σ_{wf}~ 80 ps , σ_{lf}~ 100 ps : σ_t~140 ps
This represents roughly the limits achievable with conventional planar detectors of that thickness.

σ_j - Jitter (τ_p= $t_{collection}$)



$\oplus$

σ_{lf} - Landau fluctuations



$\oplus$ **σ_{wf}** (segmentation pitch/thickness) $\approx$ **~10 ps** is (almost?) impossible in Si planar technology

For planar detectors there are two ways of design to improve timing resolution (may not always be the main driver for the choice):

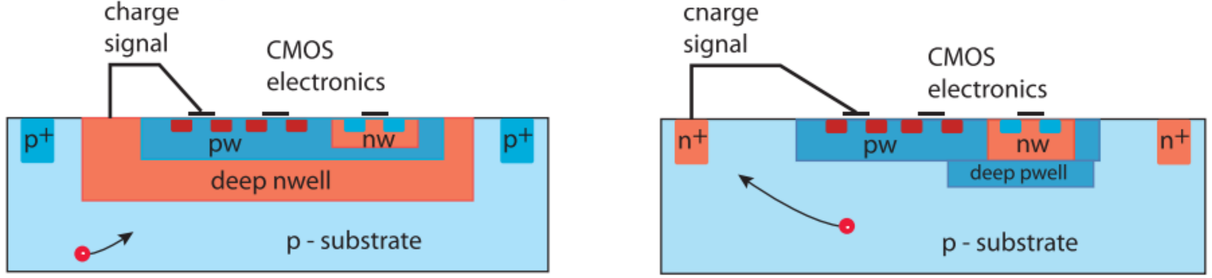
- DMAPS (reduce the noise, deplete larger volume)
- Low Gain Avalanche Detectors – mainly improve the signal and allow for thin sensors

Depleted MAPS - planar

- **S. Buhalter, MoTiC: Prototype of a Monolithic Particle Tracking Detector with Timing**
- **L. Paolozzi, MONOLITH - picosecond time stamping capabilities in fully monolithic highly granular silicon pixel detectors**

Depleted MAPS/HVCMOS offer an alternative to hybrid sensors as timing detectors – aiming for better S/N

$\tau \propto \frac{C}{g_m}$, $ENC_{\mathrm{thermal}} \propto \frac{kTC}{g_m}$ compensated by power (g_m)



taken from N. Wermes

- Large electrode: $C \approx 300\,\mathrm{fF}$
- Strong drift field, short drift paths, large depletion depth
- Higher power, slower
- Threshold $\sim 2000\,\mathrm{e}^-$

σ_{wf} - small, σ_{j}, σ_{lf} - large

- Small electrode: $C \approx 3\,\mathrm{fF}$
- Low analogue power
- Faster at given power
- Difficult lateral depletion, process modifications for radiation hardness
- Threshold $\sim 300\,\mathrm{e}^-$

σ_{wf} - large, σ_{j}, σ_{lf} - small

The limits set for the planar detector are still valid:
CACTUS D-MAPS *(Y. Degerlia et al. JINST 15 (2020) P06011)*

LFoundry-150 nm, high resistivity substrate
thickness=100 μm-> ~7500 e for m.i.p.
simulated channel noise ENC~ 300 e
τ_r~1 ns -> σ_j ~ 50 ps
σ_{wf}~0 (pixel of 1x1 mm^2)
σ_{lf}~20 ps

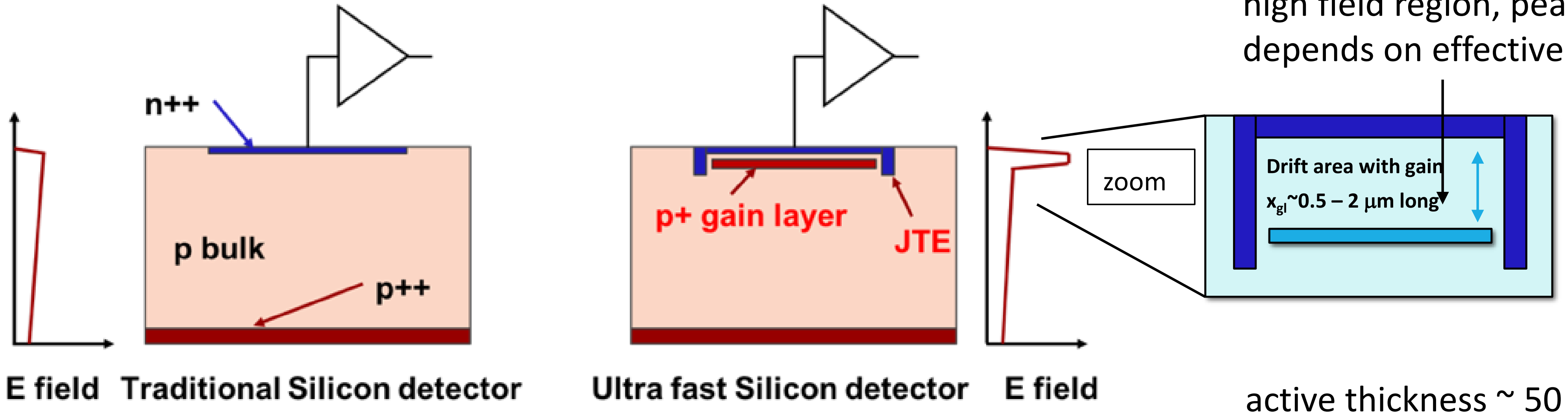
σ_t~55 ps -> 60 ps aimed also by the designers

have a look in CMOS session at Pixel 2022

Devices with Gain - LGADs

G. Pellegrini et al., NIM A765 (2014) p12.
Hartmut F-W Sadrozinski et al 2018 Rep. Prog. Phys. 81 026101
**G. Kramberger et. al., JINST 10 (2015), P07006.*
**M. Ferrero, NIM A919 (2019) p16*

high field region, peak field depends on effective doping level



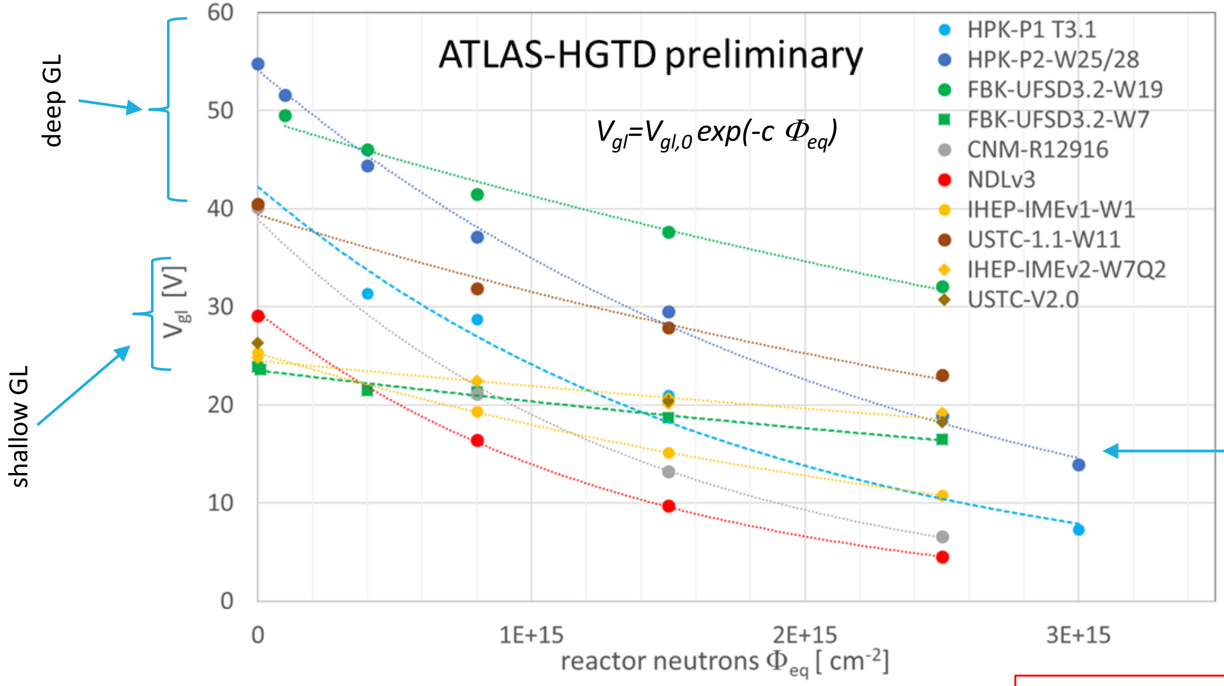
active thickness ~ 50 μm

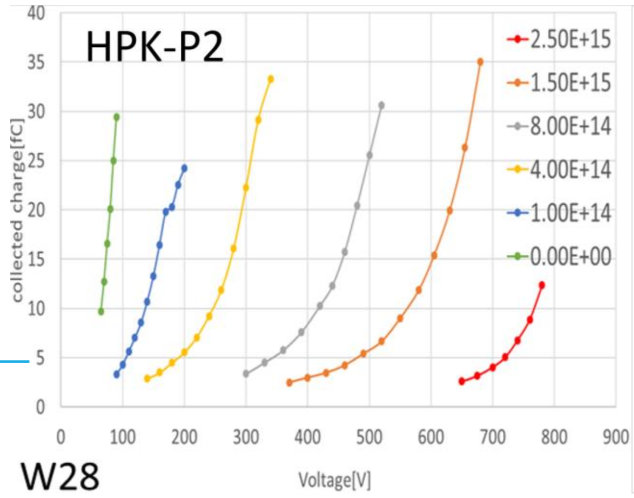
Conventional LGADs (mature enough for experiments) have two main limitations:

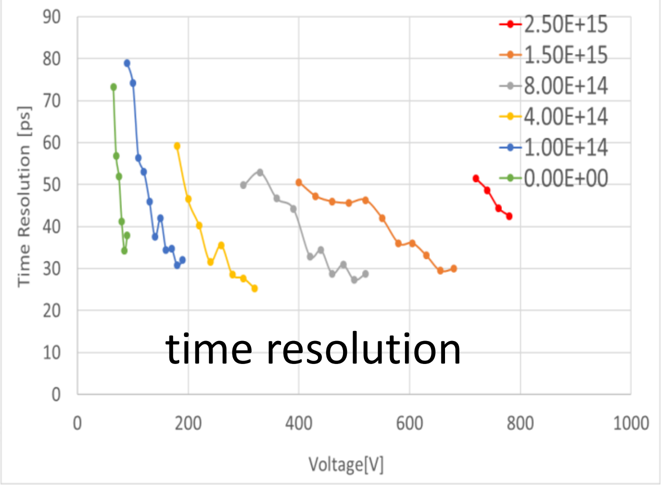
- Radiations hardness *
  - a lot of effort went in recent years to design the gain layer that is radiation hard (radiation induced interstitial Si atoms displace substitutional boron and reduced doping level)
  - **enrichment of the GL with Carbon** seem to give the best results (several fabrication sites master it, IME even in 8”process)
- Active area – fill factor problem (Junction Termination Extension region has no gain)

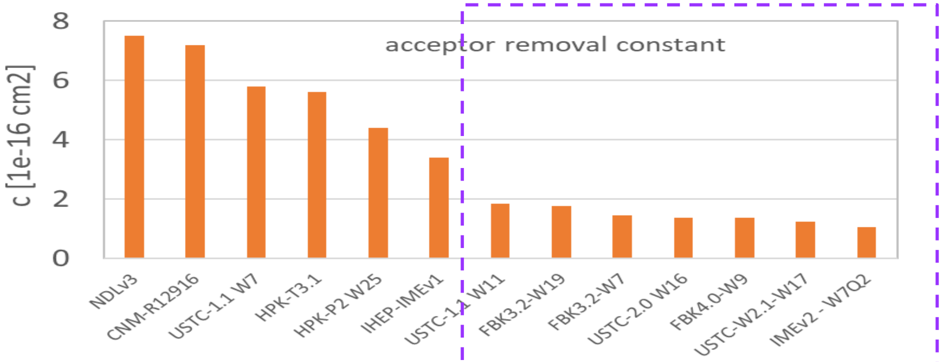
Radiation hardness problem

- **Afonso Ferreira, A High Granularity Timing Detector for the ATLAS Phase-II Upgrade**









$$\Delta V_Q \approx -\frac{D\,\Delta V_{gl}}{x_{gl}}$$

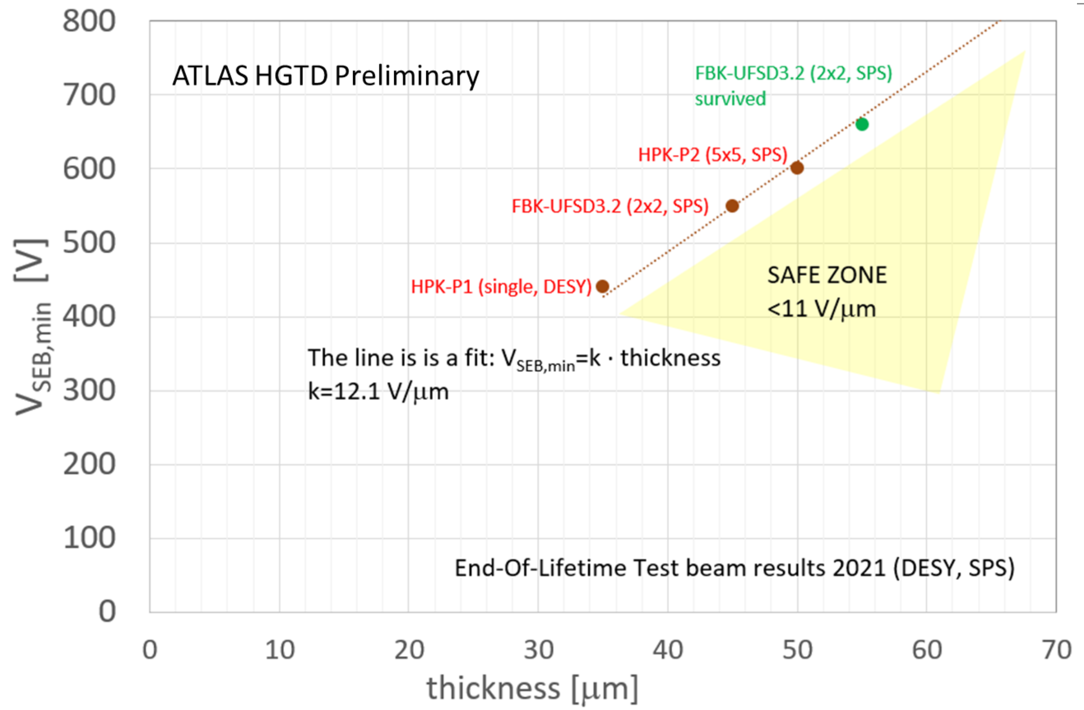
huge improvement for the C-enriched GL

Time resolution is for highly over-depleted LGADs becomes the function of collected charge and thickness only.

charged hadrons are more damaging at the same equivalent fluence!

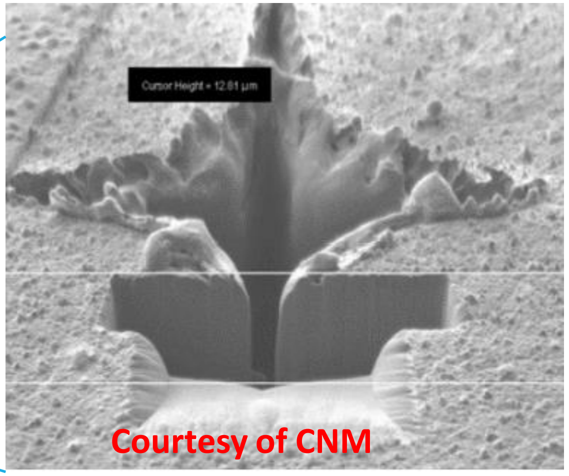
Single Event Burnout

G. Medin et al., NIMA 1041, 167321
R.Heller, 38th RD50 workshop
ATLAS-HGTD EoL TB in preparation



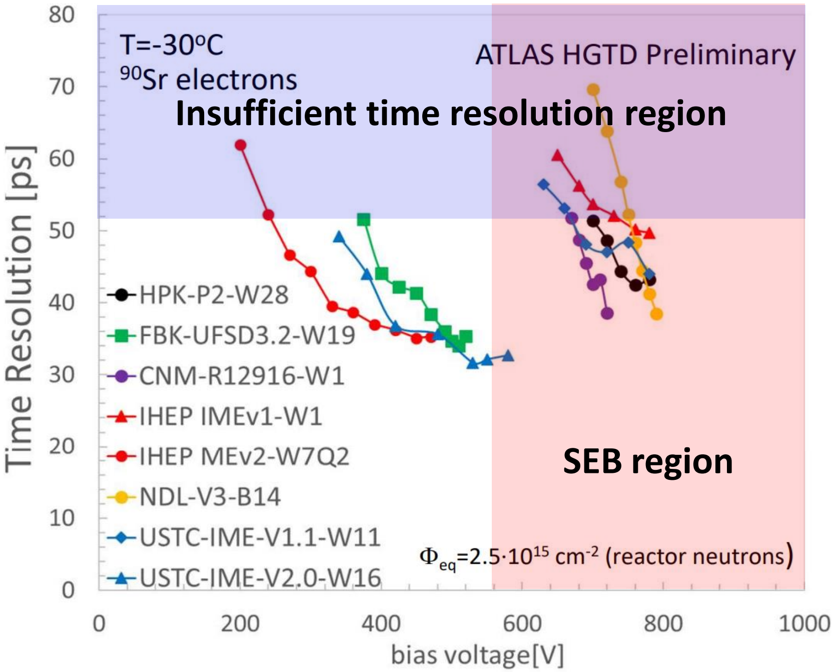
- **a single particle which deposits enough energy** (~tens MeV) causes it – conductive path which leads to destructive breakdown
- it depends **on average field only** (**initial gain, resistivity, fluence, process**…don't matter)
- several TB campaigns of CMS-ETL and ATLAS-HGTD (~100 sensors), also dedicated and fs laser testing confirmed the SEB and helped to understand it

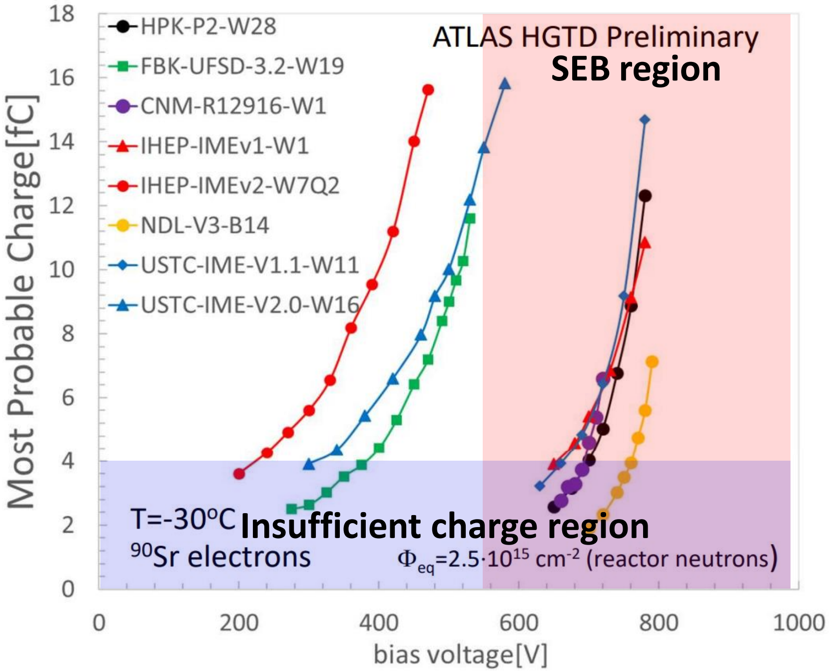
ATLAS HGTD Preliminary

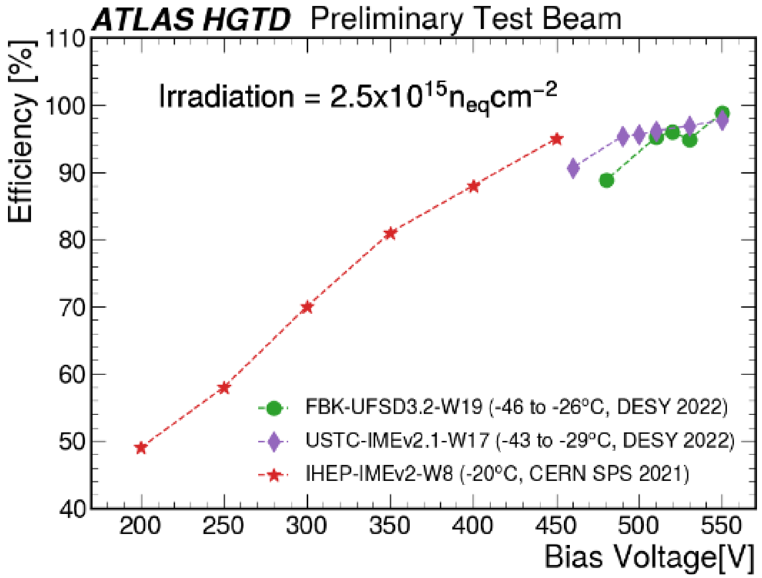


Courtesy of CNM

Charge collection and timing







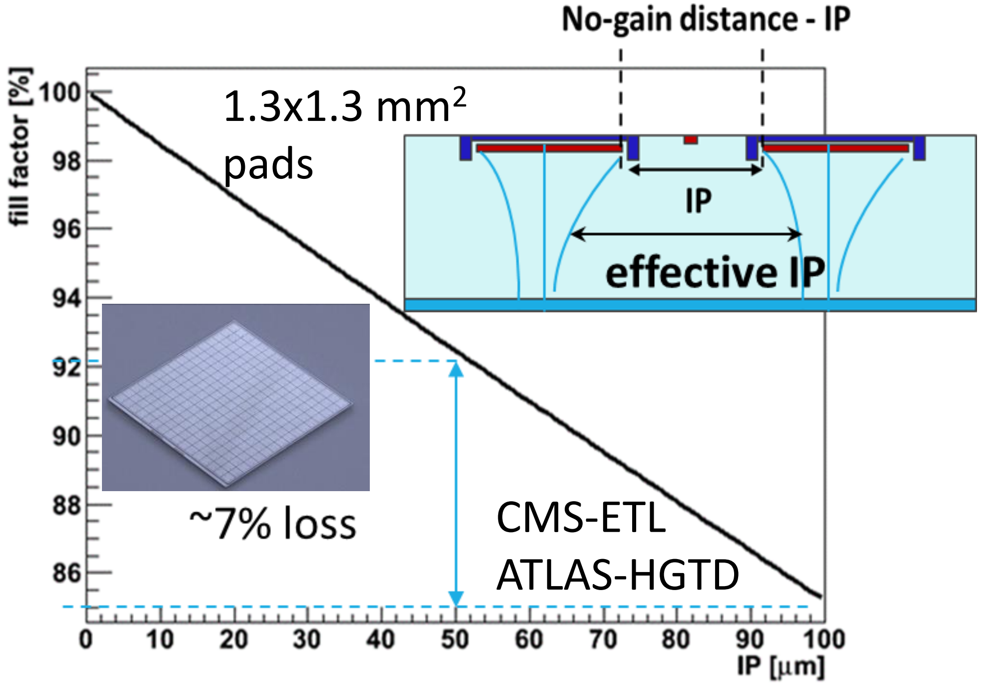
Only C-enriched GL design is in “white” region after the of 2.5e15 cm^{-2} at -30°C (HL-LHC application of LGADs)

- lower operational bias for C-GL assures smaller power consumption <50 mW/cm^2
- Note that the slope *dQ/dV* of C-GL devices is less steep – better control of operation

Fill factor or LGADs

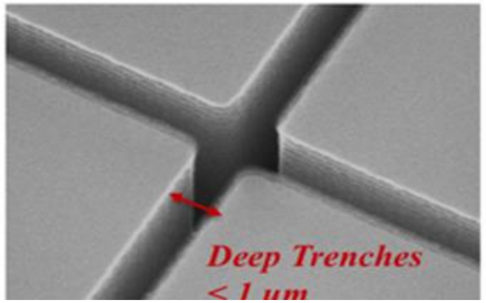
- Dima Maneuski, Performance studies of Inverse Low Gain Avalanche Detectors (i-LGAD) coupled to the Timepix3 ASIC
- Jenny Ott, AC-coupled Low Gain Avalanche Diodes for 4D tracking: impact of electrode geometry on charge sharing
- Simone Mazza, An LGAD-based full active target for the PIONEER experiment

Fill factor becomes the main problem for conventional LGADs once the pixel size becomes very small ~100 x 100 μm^2

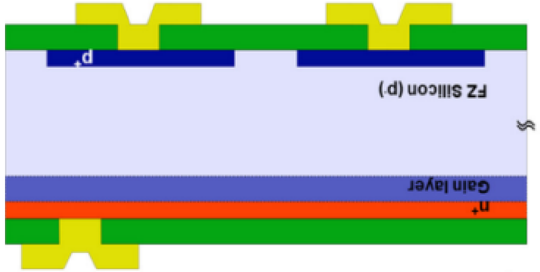


G. Paternoster et al., IEEE Elec. Dev. Letters, Vol. 41 (2020) p. 884

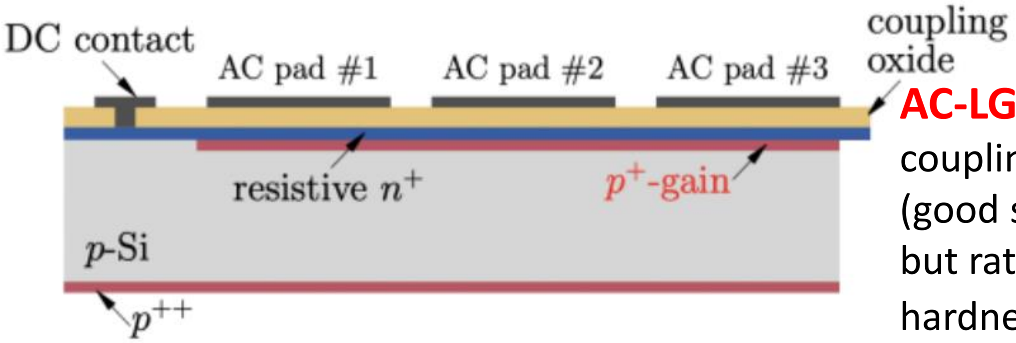
With most ambitious design IP->0!
Matias Senger, 41st RD50 Workshop



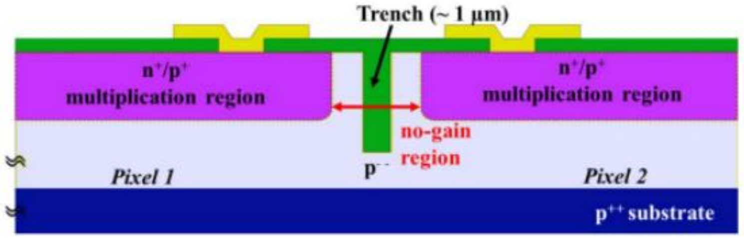
Several technologies were proposed and are investigated:



iLGAD – segment the side without multiplication no p-stop, JTE at the bottom (complex processing, radiation hardness, hole collection)

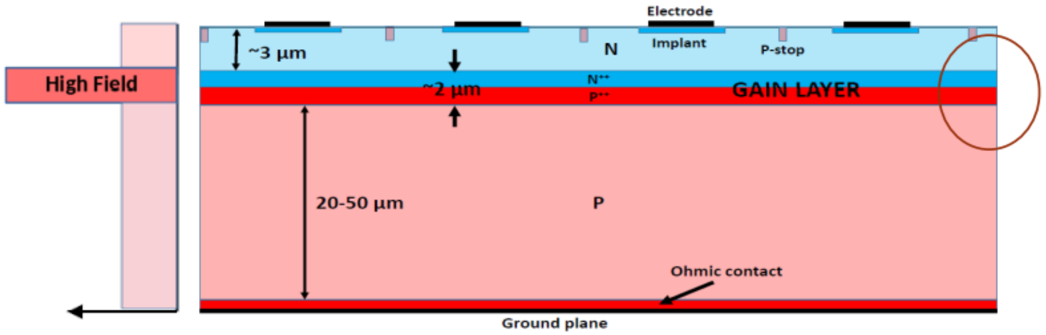


AC-LGAD / RSD– use AC coupling – bipolar signals! (good spatial and time resolution, but rate limited, radiation hardness?)



TI-LGAD – use SiO2 trenches to isolate the pads, reducing the gap by an order of magnitude.

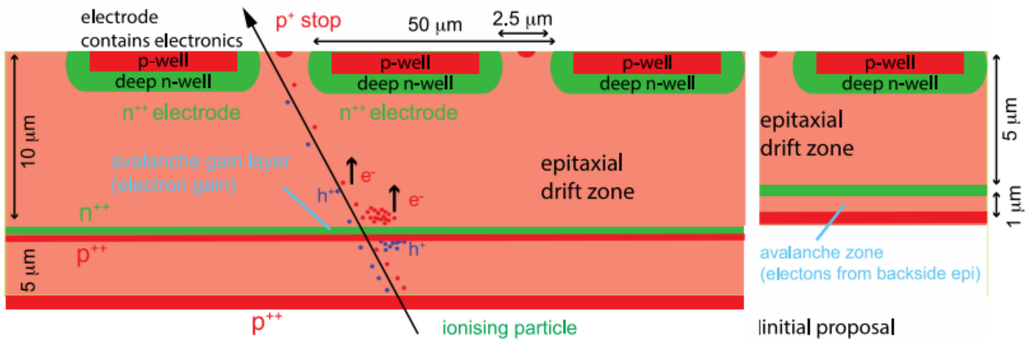
New ideas – fill factor and beyond



Deep Junction LGAD

UCSC/Cactus developments

- excellent temporal ~30 ps
- low field region at the surface – safe for breakdowns
- several open questions : tune N layer (changes with irradiations, scalability…)

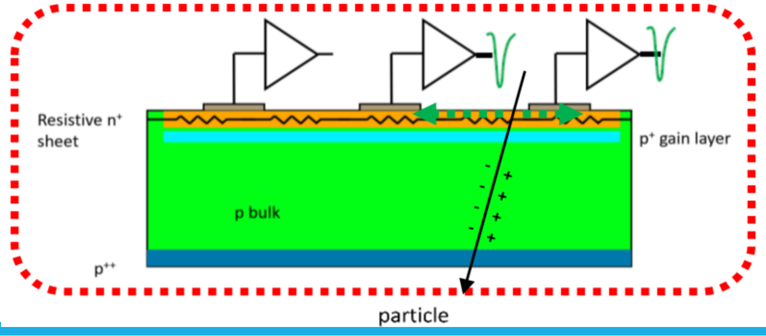


MONOLITH

- L. Paolozzi, MONOLITH - picosecond time stamping capabilities in fully monolithic highly granular silicon pixel detectors

- excellent temporal ~30 ps and spatial resolution
- radiation hardness (SEB, more sensitive to gain reduction)
- thin layer – most probable signal is lower/larger fluctuations, steep Q/V

DC-coupled RSD (DC-RSD)



DC-RSD

INFN-Torino/FBK developments

(charge sharing principle – gain is a saver)

- excellent temporal ~30 ps and position resolution ~few µm
- resistive layer doping control, size electrodes, high rate capability …

Way forward for LGADs?

- Solution to radiation hardness limitations (presently ~2.5e15 cm^{-2}):
  - Using compensated material P-B doped GL and exploiting the removal of both dopants, so starting with highly enough doped material one can have $N_{GL}=N_A\, exp(-c_B \Phi_{eq})-N_D\, exp(-c_P \Phi_{eq})$ under control *(EC AIDAINNOVA blue sky project,* V. Sola, 40th RD50 Workshop)
  - Using very high temperature annealing ~>250°C which leads to re-activation of active acceptors (how to implement that in a real experiment?) G. Kramberger, 40th RD50 Workshop
  - Unknowns: impact ionization can depend strongly on fluence as does the mobility – maybe gain mechanism will not even work at very high fluences

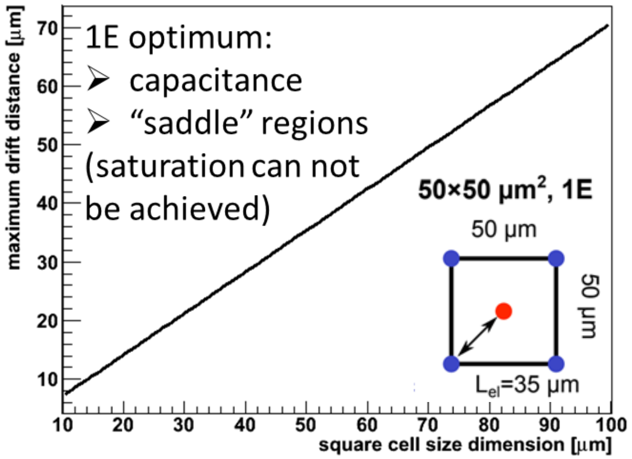
- Fill factor can be solved, but:
  - having small pixel have pitch/thickness so that σ_{wf} is becoming an important contribution!
  - iLGAD will lead to collection of holes – need to be studied at after irradiations
  - AC-LGAD, DC-RSD could have a rate issues …

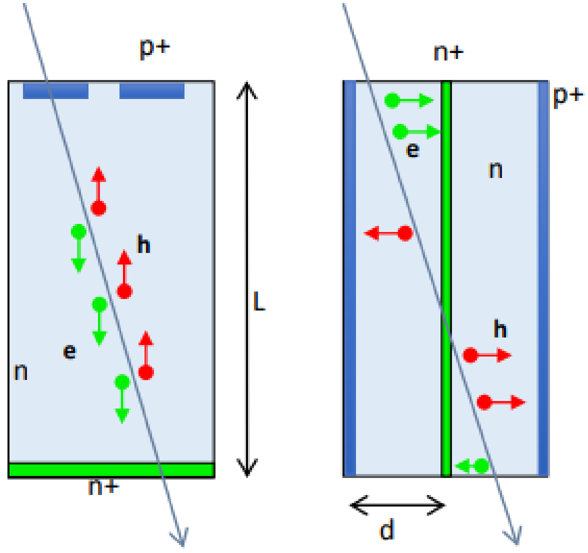
LGADs are the only planar technology good enough for precise timing (<50ps), but excellent electronics is needed. (marriage of LGAD + CMOS looks promising – DJ-LGAD, MONOLITH)

3D detectors for timing applications

3D technology as timing detectors:

- They have fill factor ~100% (inclined tracks)
- The radiation tolerance of small cell size devices is large (for signal) and allows operation at higher bias voltages – shown up to ~1e17 cm^{-2}
- Technology is more mature - IBL





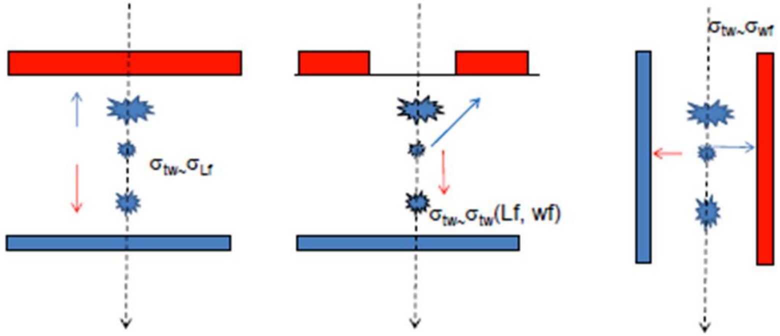
Planar sensor
d = L

3D sensor
d << L

S. Parker et al, Nucl.Instrum.Meth.A 395 (1997) 328-343

But/However:

- 3D can be fast – ☺ short drift distance, but ☹saddle regions in the field
- the weighting field – hit position - will impact the signal ☹
- they can be thicker as Landau fluctuations play a minor role
- the capacitance will be much larger (hence noise and the jitter) particularly for thick sensors
- Lower operation voltages than for planar detectors (LGAD) and possibly lower current ($I_{LGAD}=G\cdot I_{gen}$) result in smaller power dissipation



3D – for timing detectors

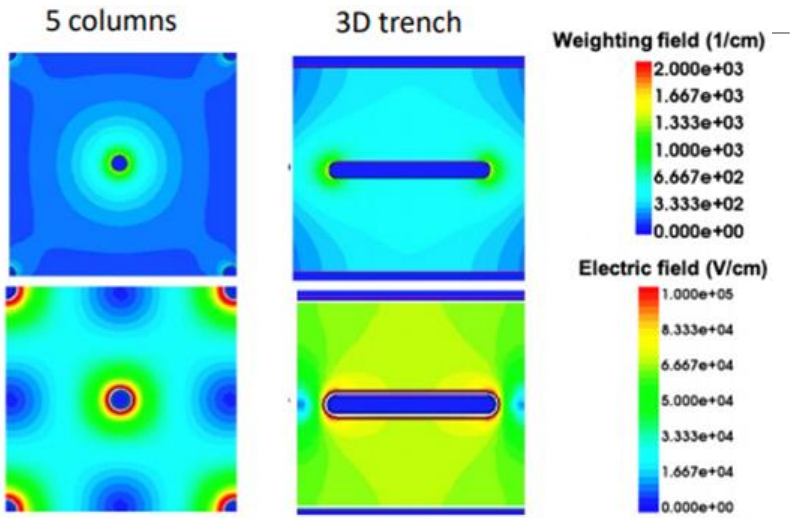
- A. Lai, 10-ps timing with 3D-trench silicon sensors at extreme rates

There are two approaches taken so far:

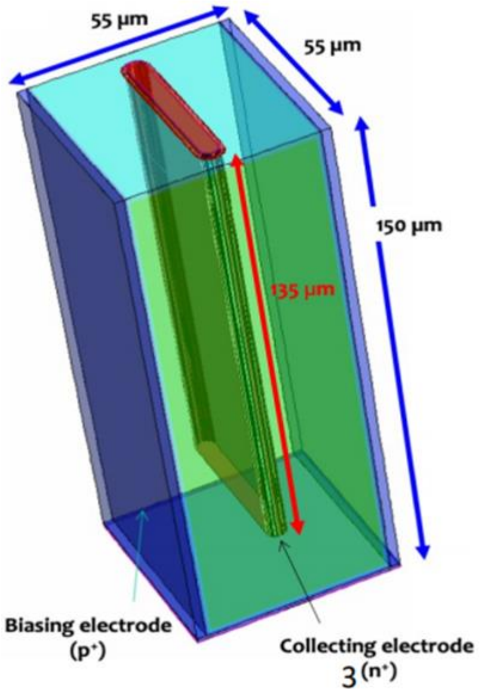
- Column 3D detectors (different patterns)
- Trench 3D detectors

(web.infn.it/timespot/)

$$i = q\,\vec{E}_w \cdot \vec{v}_d$$



TCAD simulation



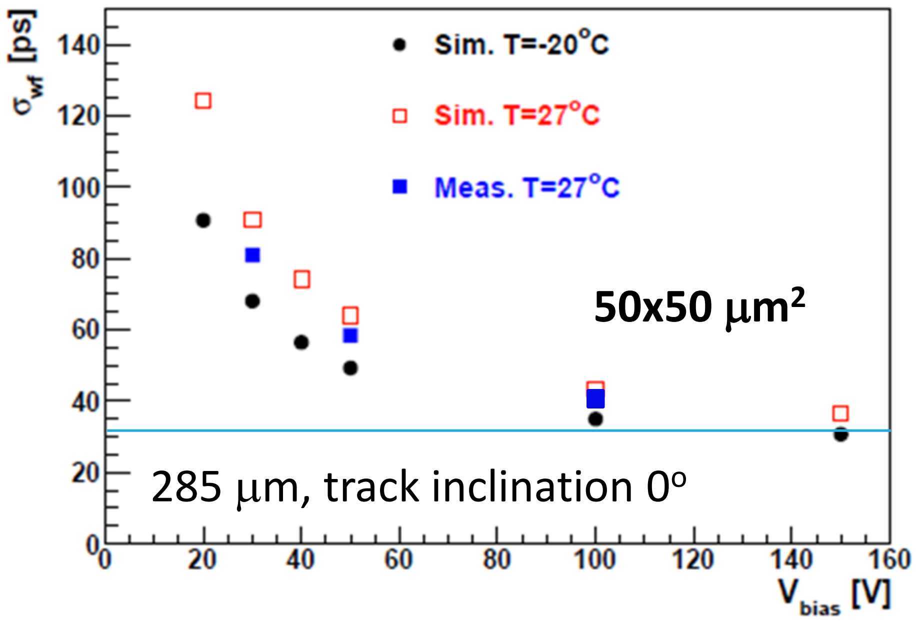
Trying to achieve constant E_w and velocity – minimum σ_{wf}

This can be seen as two pad detectors in back-to-back, rotated for 90^o and stacked together **-> the optimum design and should lead to the minimum achievable σ_{wf} for a given cell size**

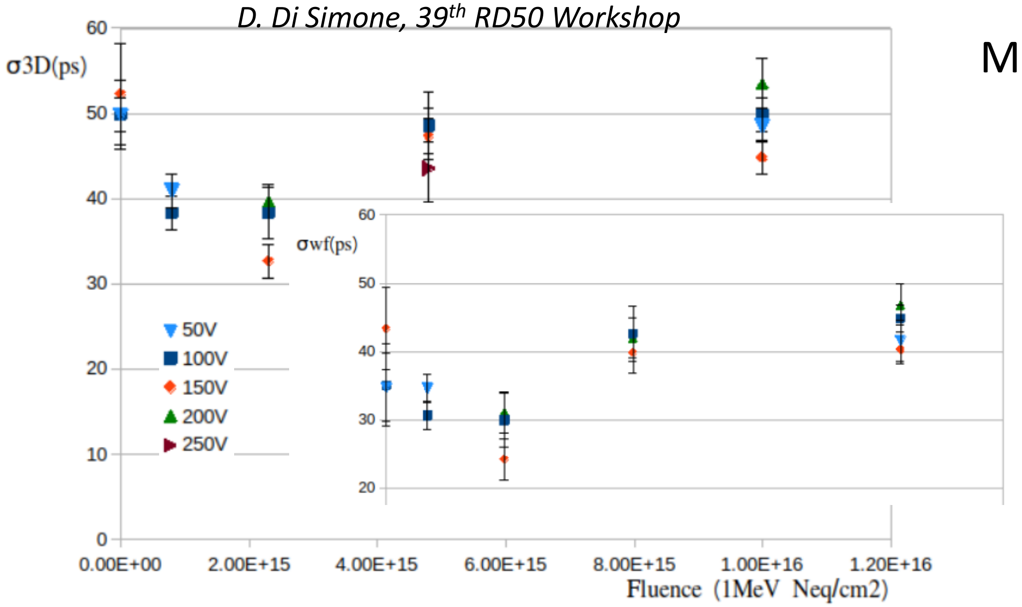
The price to pay:

- smaller fill factor which limits the cell size – hence efficiency and the position resolution
- significantly larger capacitance (**optimization σ_j vs σ_{wf} with power constrain is the key**)
- more complicated production – yield issues, scalability, ….

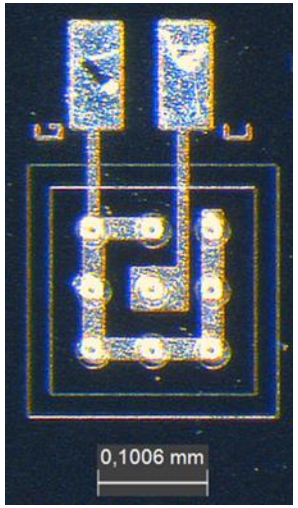
Column 3D - Measurements and simulations



G. Kramberger et al., NIMA 934 (2019) p. 26.


D. Di Simone, 39th RD50 Workshop

Measured device (CNM)



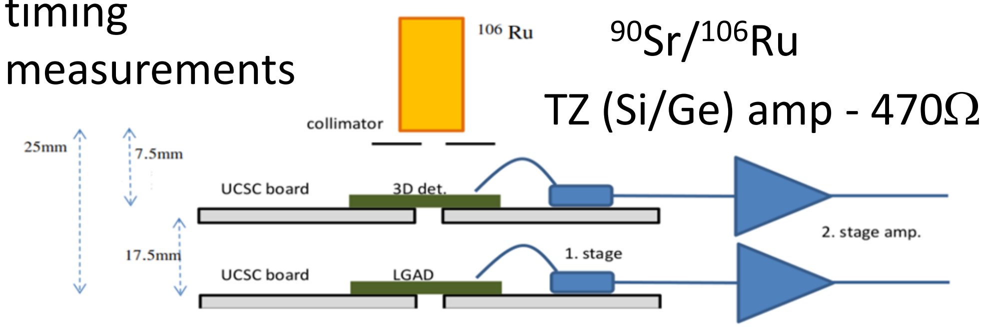
Single square cell readout σ_{wf} at -20°C and 100V

- **25x25 μm -> ~13 ps**
- **50x50 μm -> ~32 ps**

for multiple cell connected together and inclined tracks even better time resolution can be achieved

- around 20-25 ps for 50x50 μm² cell

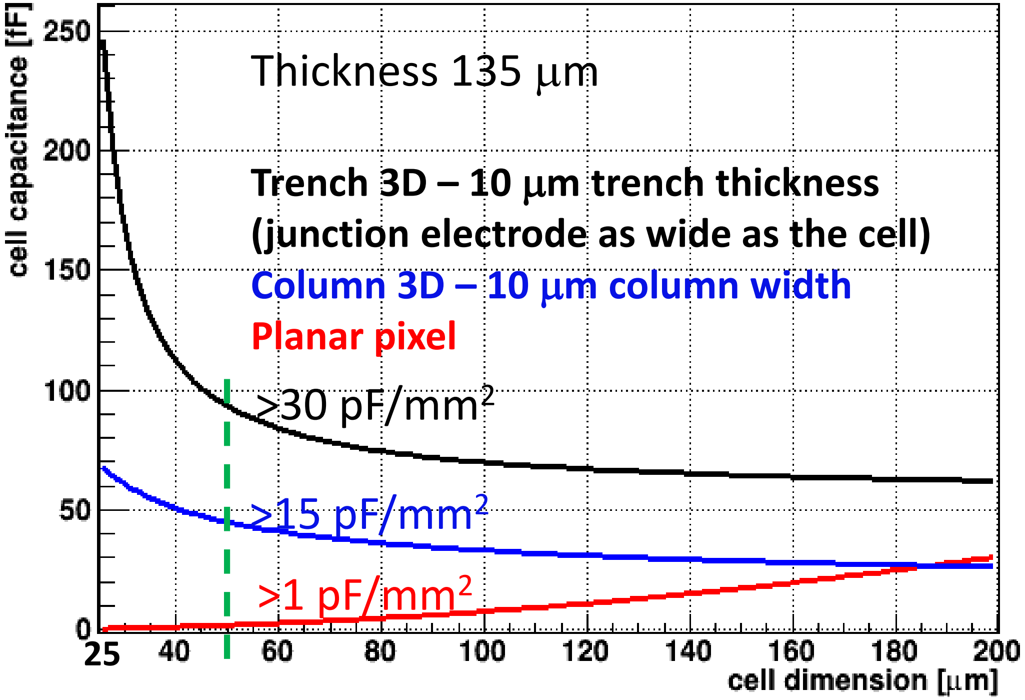
timing measurements

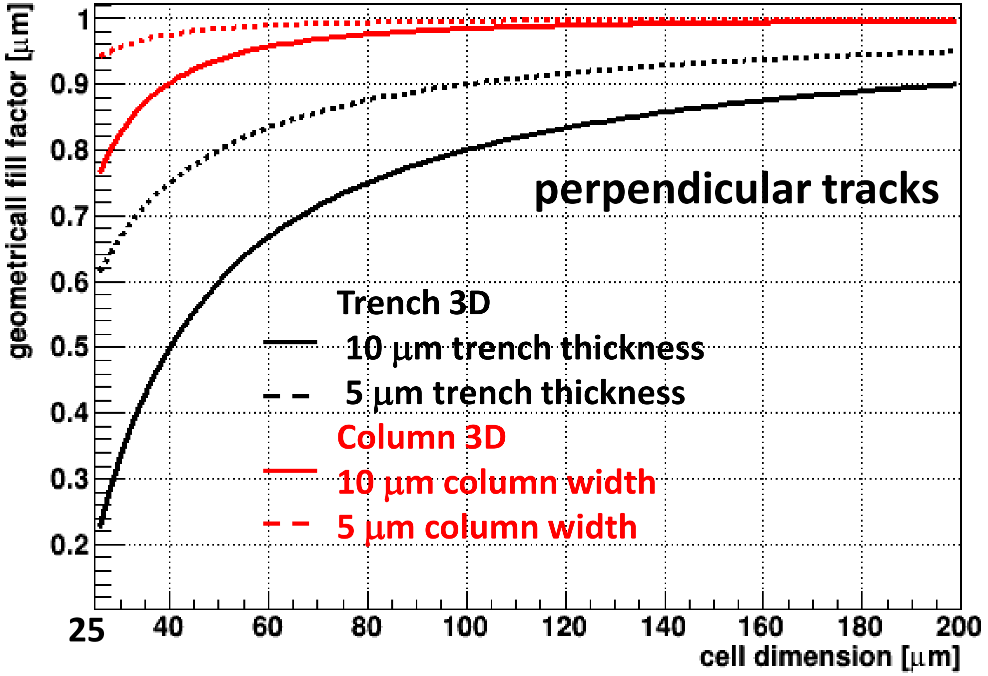


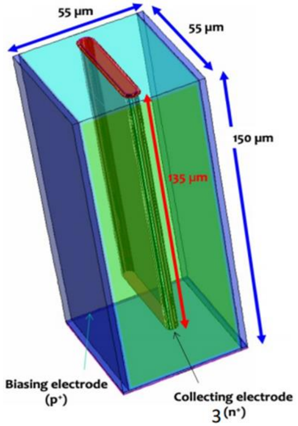
^{90}Sr/^{106}Ru

TZ (Si/Ge) amp - 470Ω

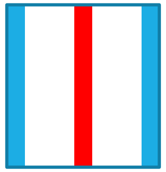
Drawbacks of 3D (Capacitance and fill factor)



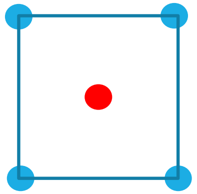




- ➢Much larger capacitance of the trench design wrt. to column and planar (ASIC is crucial)
- ➢At small cell sizes needed for superior timing resolution the fill factor can become a major issue:
  - ➢For column like the direction of the inclined tracks is not very important
  - ➢**For trench detectors the direction of tracks is crucial (detector design should be tailored to the application)**



not fully efficient for all φ at θ≠0



fully efficient at θ≠0

Way forward for 3Ds?

- Small cell size 25x25 μm^2 /25x50 μm^2 required for position resolution and high rates would allow also hit time resolutions **~10-20 ps**.
  - the column width reduction ~10 μm to <5 μm (reduction of capacitance, improvement of S/N, reduction of the jitter/power and increase of fill factor) – in the future column widths as low as ~1-2 μm may be possible allowing possible multi-cell configurations.
  - improved aspect ratio of Deep Reactive Ion Etching (DRIE) is crucial -> current aspect ratio of 25 should be improved, particularly for thicker detectors that may be required to improve the signal required in severe radiation hard environment - larger clusters become the problem.
  - The choice of design (Trench/Column) will be a matter of optimization σ_{wf} vs. σ_j vs. fill factor and there is no clear answer to which is better (it depends on application)
- New ideas will be important and may become possible and/or mature over the years:
  - “Marriage” of LGADs and 3D (either by trench filling, careful substrate selection with small interelectrode distance allowing charge multiplication without special processing of gain layer)
  - “Marriage” of CMOS and 3D.
- The scalability is a question for the producers:
  - single sided processing is a major step forward, the next is move to >=8” wafers, where thicker wafers are required
  - Yield improvement , robustness of the designs are key
- Operation conditions: cooling down as low as possible improves the performance in all respects not only power dissipation/leakage current, but also in speed and possible charge multiplication

Electronics – the key element!

- A. Lai, TimeSPOT ASIC developments for 4D-pixel readout
- The monolithic ASIC for the high precision preshower detector of the FASER experiment at the LHC

Transimpedance amplifier with: $\tau \sim t_c$
τ=peaking time
t_c=charge drift time

taken from A. Lai, INFN - Cagliari

$$\sigma_t = \frac{\partial t_{thr}}{\partial t_c}\sigma_{tc} \approx \frac{\tau}{2}\sqrt{\frac{V_{th}}{I_0 R_m}\frac{\sigma_{tc}}{t_c}} \approx \left(\frac{1}{2}\frac{\tau}{t_c}\sqrt{\frac{N}{S}}\right)\sigma_{tc}$$

→ depends on spread of charge collection times and S/N

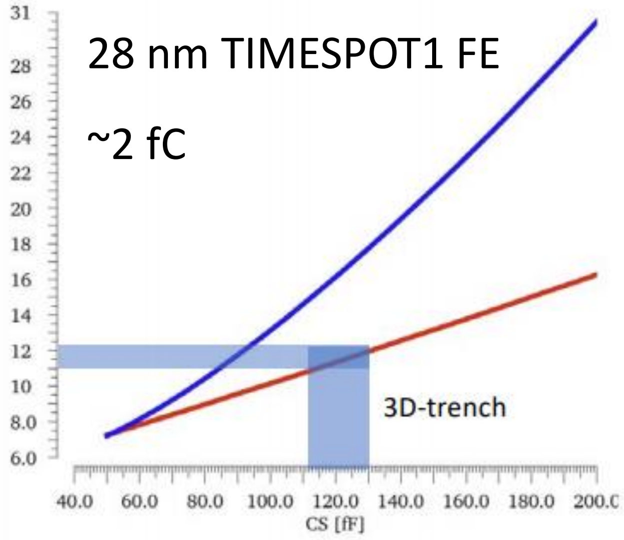
The price to pay for speed and better time resolution is power consumption

Currently the performance (ALTIROC, ETLROC, TimePix4, Fast2):
at power consumption ~few mW/mm^2

$$\left.\begin{array}{l}\text{FOM} \sim 20\text{-}40 \text{ ps fC/pF}\\ \sigma_j = \text{FOM}\cdot C_d/Q_{tresh}\\ \sigma_j \sim 40 \text{ ps (e.g. ALTIROC)}\end{array}\right\}$$

C. De La Taille, AIDAINNOVA meeting, April 2021)

It is likely that new developments in electronics (fast SiGe BiCMOS, 28 nm -> CMOS) are going to be needed to exploit the sensor capabilities with peaking/rise times of ~1 ns.



L. Piccolo – INFN Torino

σ_{ej} vs sensor capacitance

Conclusions

If you are looking at that slide, I am surely late….

The timing requirements are becoming a crucial component of many new detector technologies.

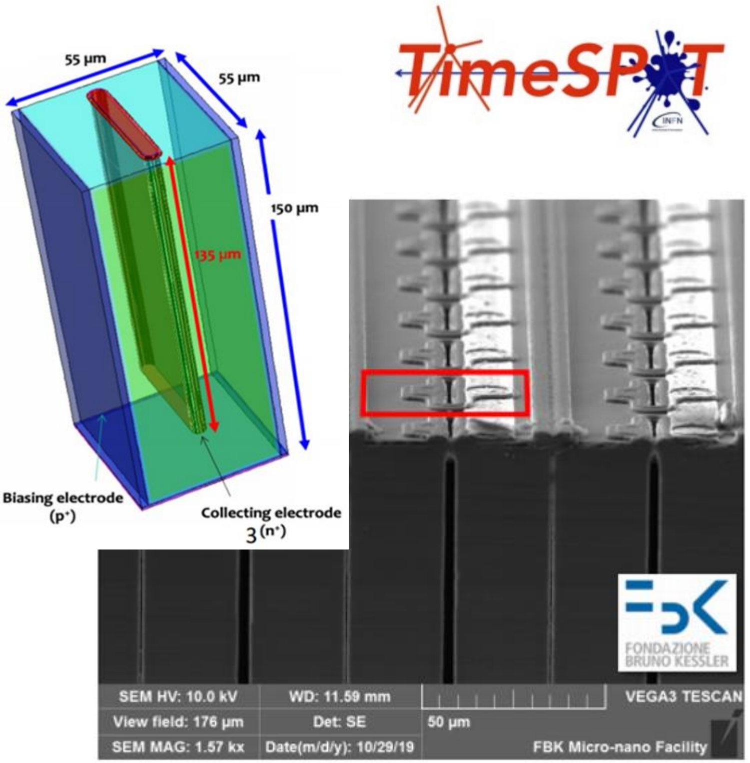
The ultimate goal is so ambitious that it looks almost impossible, but 30 years ago also present technologies looked impossible too....

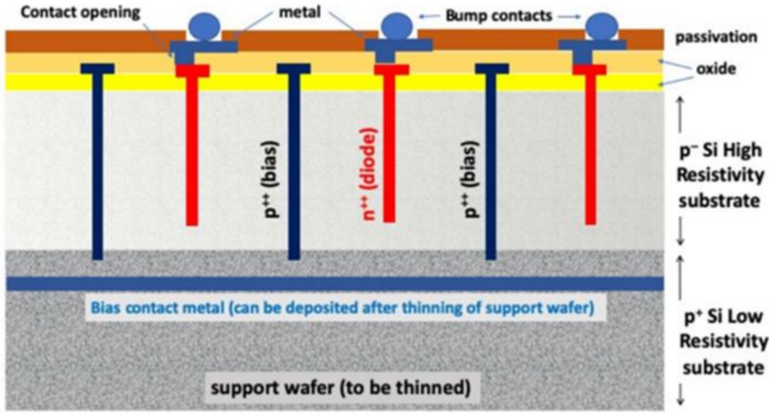
BACKUP

Trench - 3D detectors

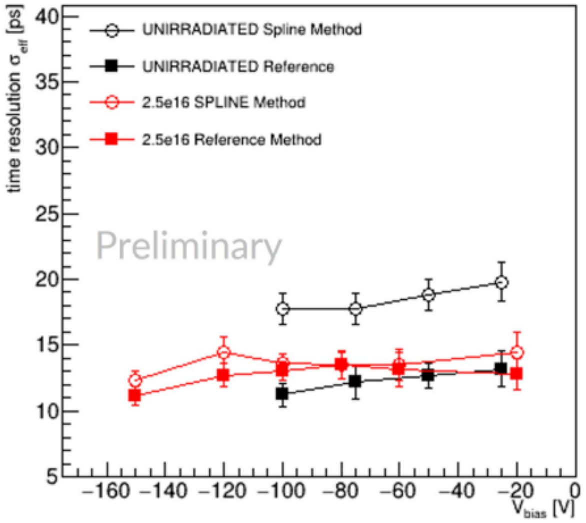
- A. Lai, 10-ps timing with 3D-trench silicon sensors at extreme rates

- **55x55 µm²** pixels
- **150 µm** active thickness
- Collection electrode **135 µm** deep





web.infn.it/timespot/



The σ_{wf} (intrinsic time resolution) of was found to be ~14-15 ps with accurate analysis **~10 ps.**

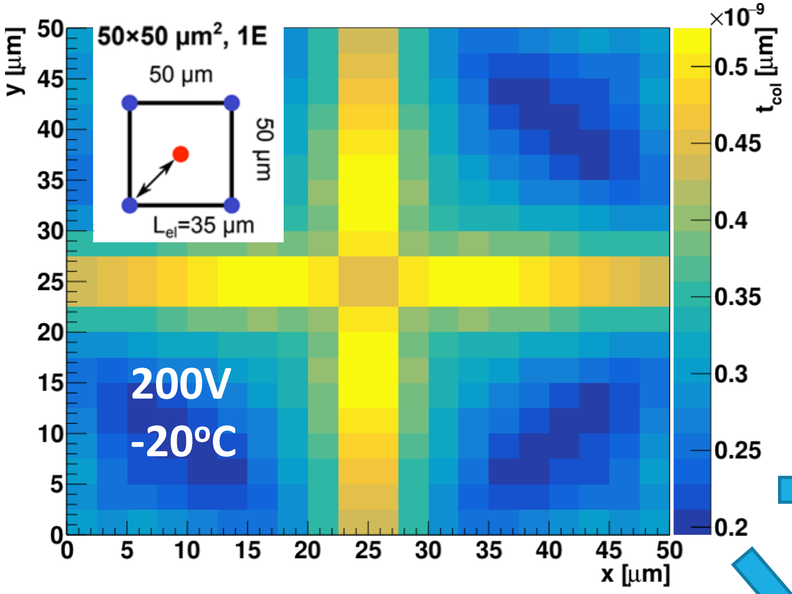
The tails in distribution due to low field regions in the space between the pads.

The reduction cell size may not improve the time resolution σ_t as the σ_{wf} may not be the limiting factor to the total time resolution.

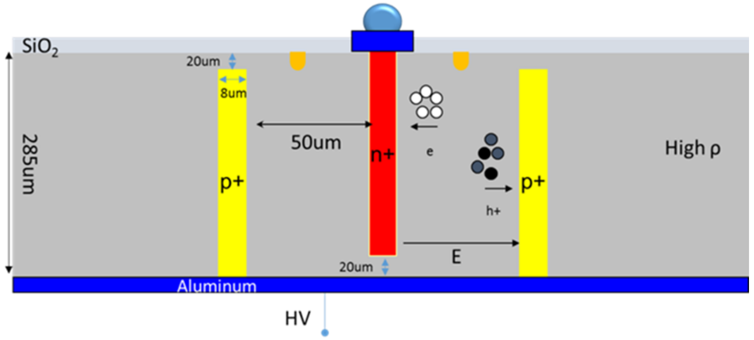
around 15-20 ps better time resolution than for similar cell size with 3D-columns.

A. Lampis, 16th TRENTO workshop, 2021
M. Garau, 16th TRENTO workshop, 2021

Column-3D detectors



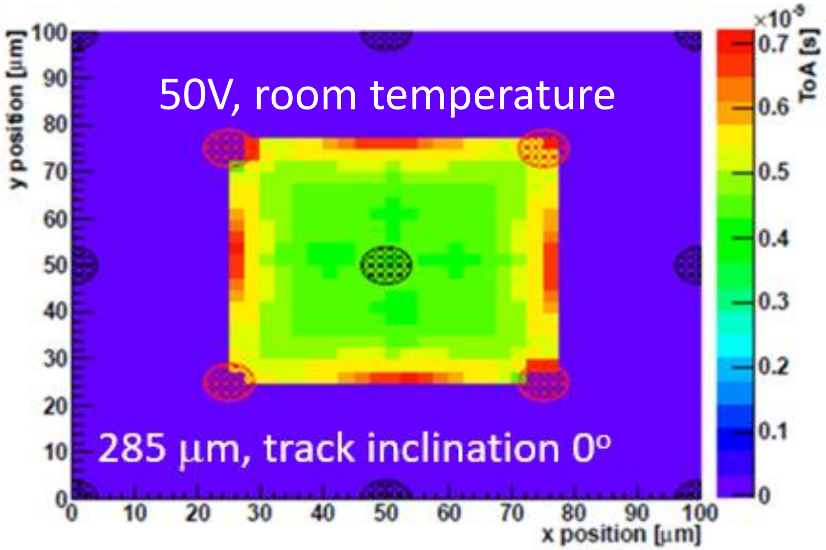
200V
-20°C



CSA τ=1.5 ns

CFD=25%

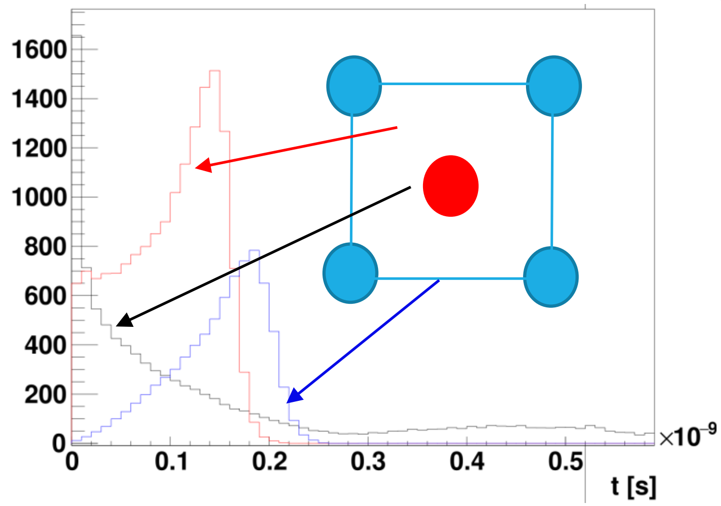
$$\sigma_{wf} \propto \sigma_{tc}$$

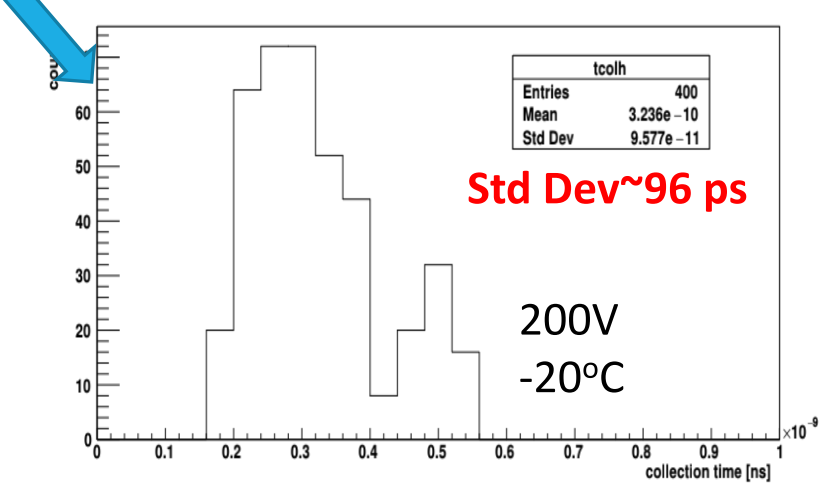


50V, room temperature

285 μm, track inclination 0°

G. Kramberger et al., NIMA 934 (2019) p. 26.



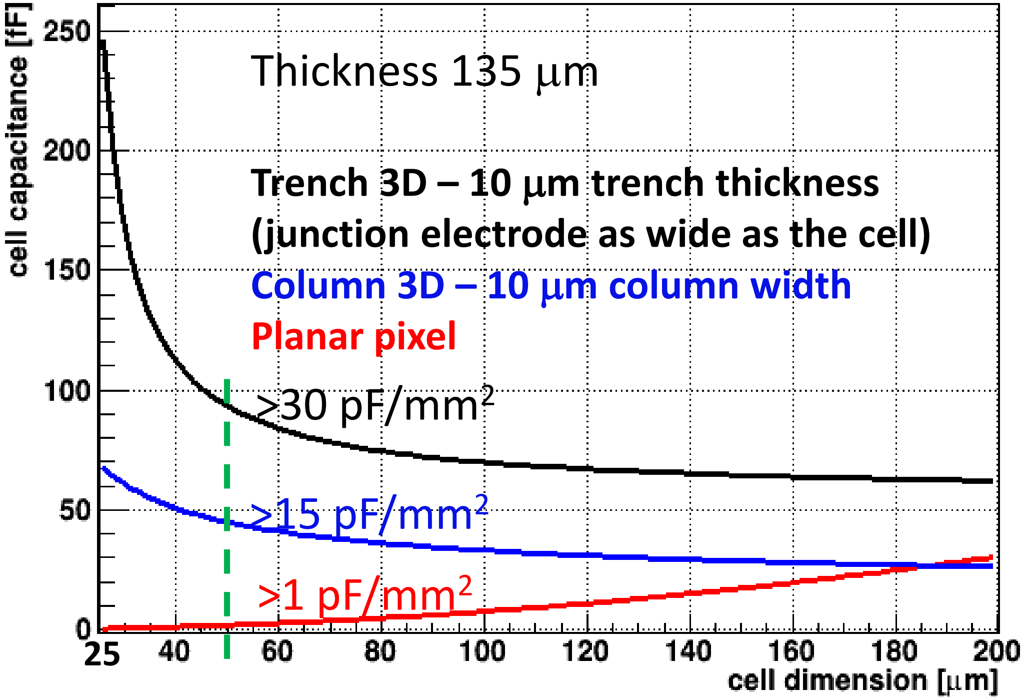


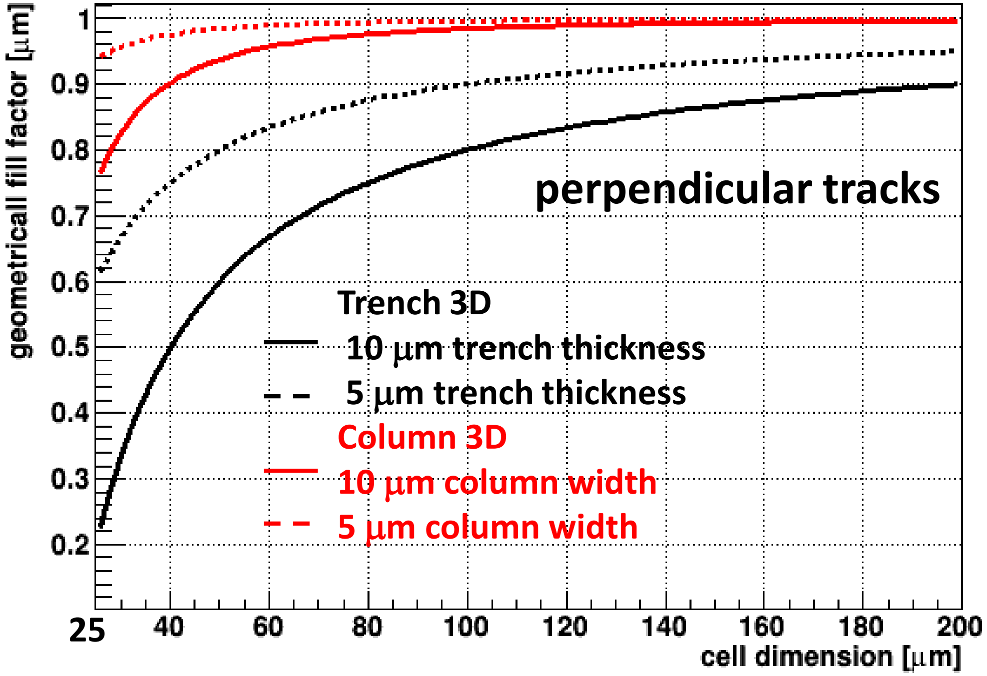
Std Dev~96 ps

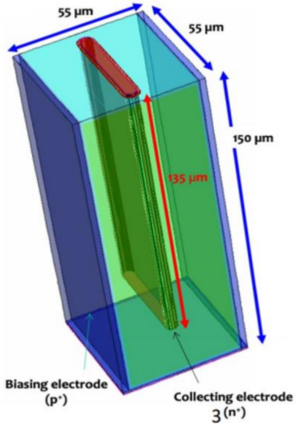
200V
-20°C

Low field regions (saddle) between ohmic columns worsen the timing resolution (spread in ToA)

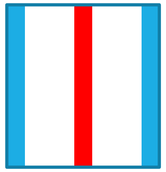
Drawbacks of 3D (Capacitance and fill factor)



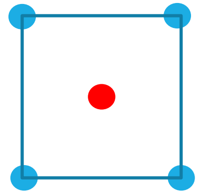




- Much larger capacitance of the trench design wrt. to column and planar (ASIC is crucial)
- At small cell sizes needed for superior timing resolution the fill factor can become a major issue:
  - For column like the direction of the inclined tracks is not very important
  - **For trench detectors the direction of tracks is crucial (detector design should be tailored to the application)**



not fully efficient for all φ at θ≠0



fully efficient at θ≠0

Conclusions

The 3D design developments can lead to sensor solution for 4D tracking where ultimate radiation tolerance accompanied with small pixel size is required. The challenges ahead are very large, but there is no a clear show stopper.

Appropriate ASIC development is likely more challenging in terms of radiation hardness, power consumption connectivity and required functionality per pixel (not to mention cost).

Connectivity of sensors is something that is very important/challenging, but the progress is very rapid (ACF, 3D Wafer-Wafer bonding).

see AIDAINNOVA 2021 kick-off meeting
D. Dannhein, F. Hugging talks