Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

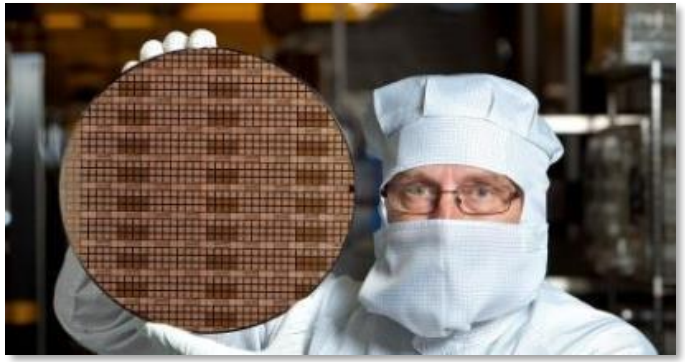
Trends in Electronic Packaging Technology

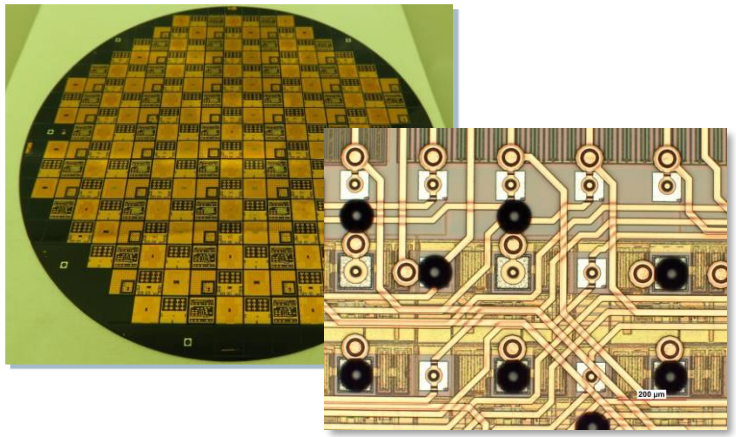
Thomas Fritzsch, Fraunhofer IZM, Berlin

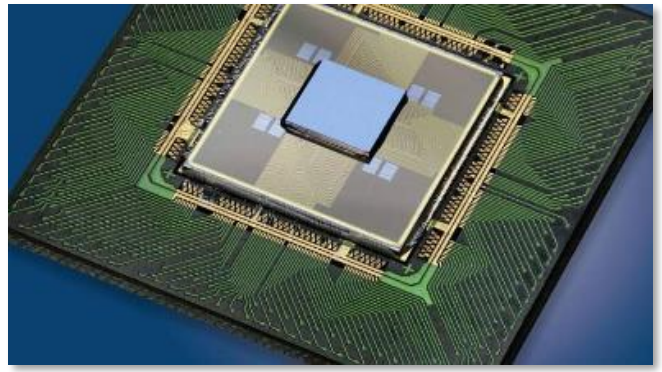
The Tenth International Workshop
on Semiconductor Pixel Detectors for Particles and Imaging

Electronic Packaging

Front-End Wafer Manufacturing	„Middle End“ Wafer Level Packaging	Back-End Assembly & Test
■ Implantation ■ PVD ■ CVD ■ Etch ■ Cleaning ■ Wafer test	■ RDL / wiring ■ Bumping ■ 2.5D Interposer ■ 3D TSV ■ FO-WLP ■ W2W Bonding	■ C2C, C2W, C2S Bonding ■ Underfill ■ Molding ■ Test







Classification according to High-End Performance Packaging: 3D/2.5D Integration 2022 | Report | www.yole.fr

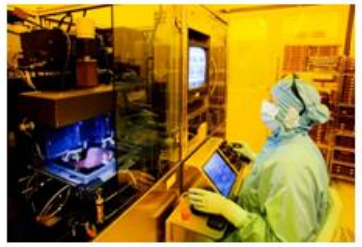
Wafer Level Packaging: Micro Bumping and Hybridization Process

General process flow

Seed layer	Resist coating	Lithography	Elecroplating	Strip/ Etch	Dicing	Assembly

PVD
(Physical Vapour Deposition)

Spin Coating
Spray Coating



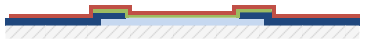
Mask aligner
LDI

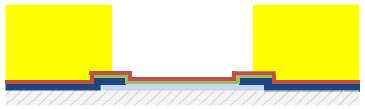
Electrolyte +
Plating tool

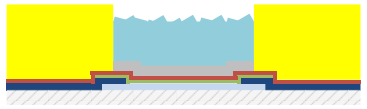
Wet etching
Spray / Immersion

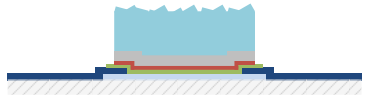
Dicing

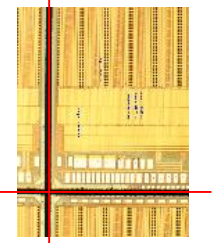
Flip Chip







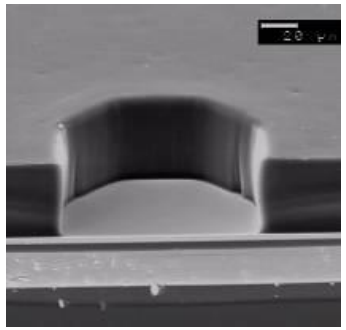




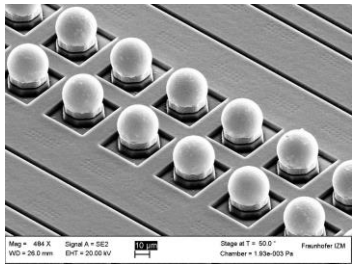
FC Bonding
C2C, C2W,
W2W

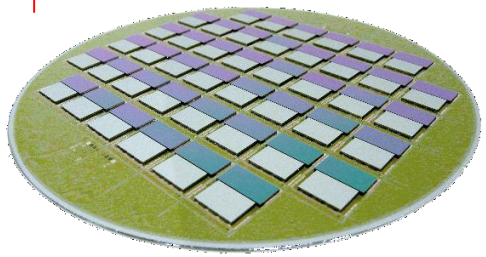
- Sputter etching, sputtering of adhesion layer and plating base.

- Coating and patterning of the resist layer
- Laser direct imaging or mask lithography

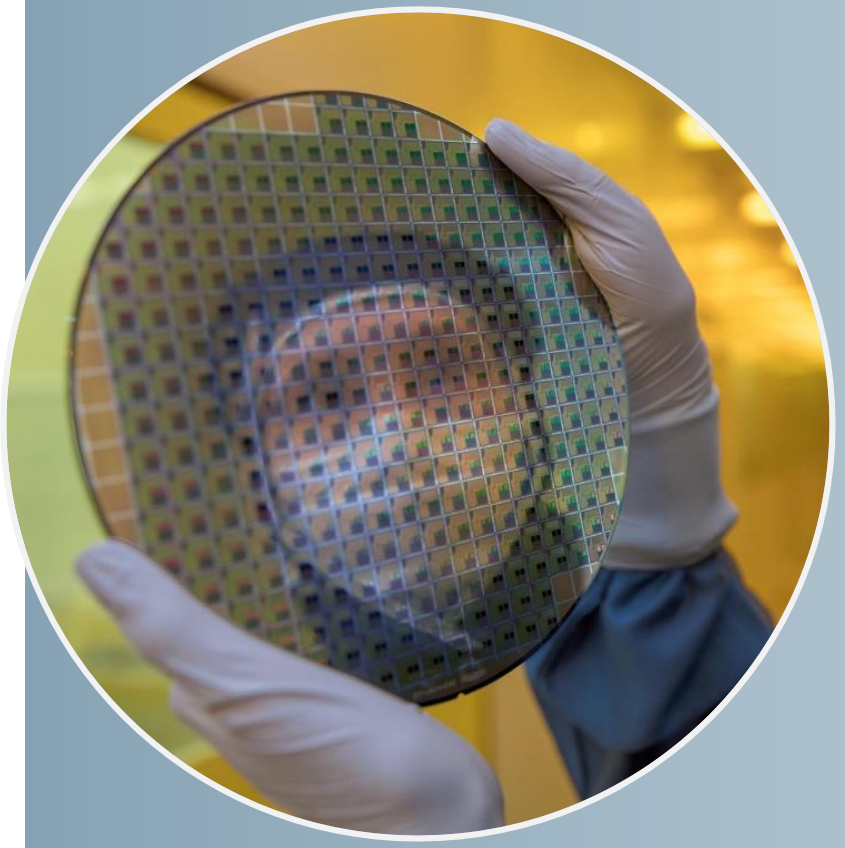


- Electroplating of UBM and Bump
- Resist stripping and etching of the plating base
- Optional: Reflow





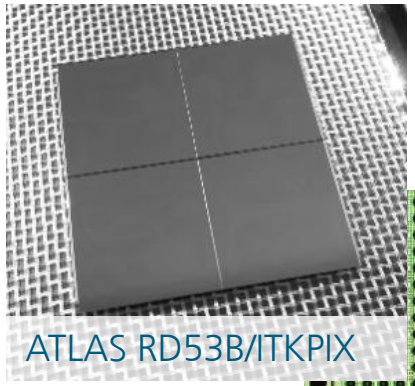
Outline

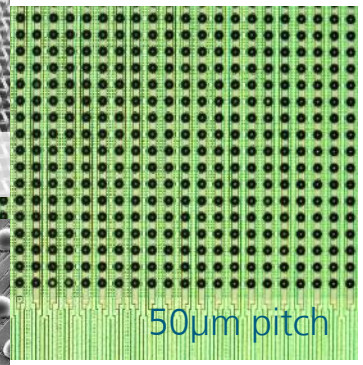


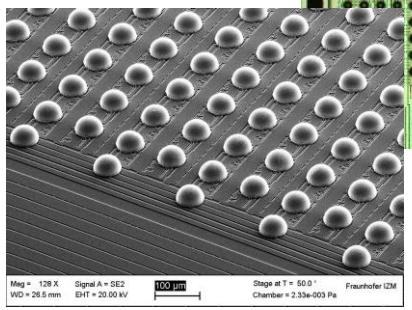
- **Status Hybrid Pixel Detectors**
- **New Developments**
- **Trends in Advanced Electronic Packaging**

Flip Chip Assembly Parameter - Interconnection Pitch

Fine pitch bumping

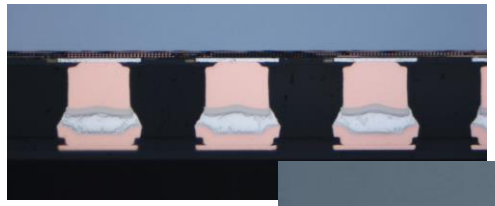


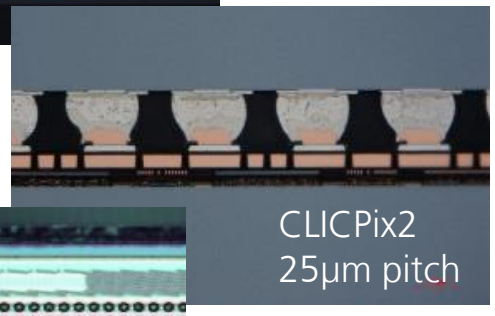


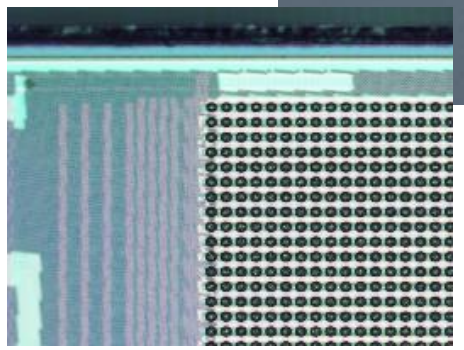


- Pitch 100…50µm
- Bump size: 50…25µm
- Material: Solder bumps, pillar bumps with solder cap

µ-bumping

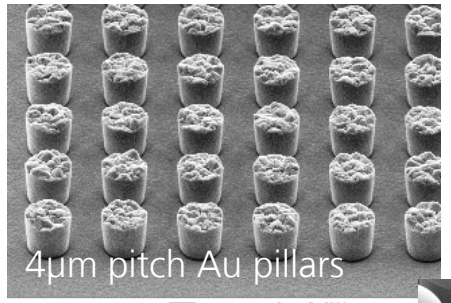


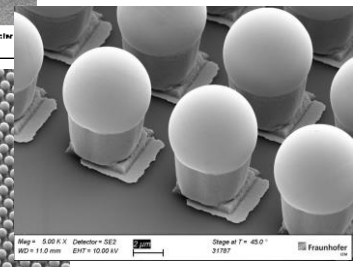


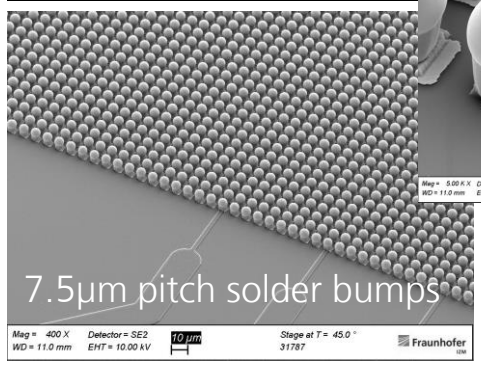


- Pitch 50…20µm
- Bump size: 25…12µm
- Material: Solder bumps, pillar bumps

Sub-10µ-pitch







- Pitch 10…2 µm
- Bump size: 6…1µm
- Material: pillar bumps, metal pins

Process Line Parameter – Wafer Size

300mm (12“)

- 65nm technology
- ATLAS ITKPix/CMS CROC/ TIMEPIX4
- pitch 50x50 µm², ~20 Mio. bumps/w (RD53B)
- thin wafer handling (≤ 150µm)
- 3D TSV processing

200mm (8“)

- 180/130/65 nm technology
- Readout: ATLAS FE-I4, MEDIPIX3, TIMEPIX3, ePIX10k,…
- Sensor: CMOS, DMAPS
- pitch 55x55 µm², ~6 Mio. Bumps/w (MEDIPIX3)
- thin wafer handling (≤ 100µm)
- 3D TSV process

150mm / 100mm (6“ / 4“)

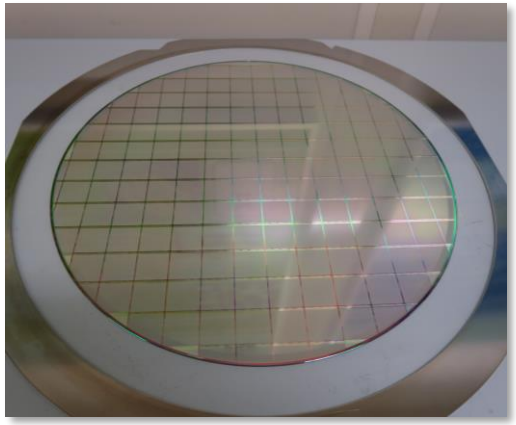
- Planar, 3D sensor technology
- Bumping/UBM deposition process: electro-plating, e-less (NiAu), PVD
- Thin Wafer Handling: 150µm … 50µm

4“/ 3“ III-V-compound semiconductor

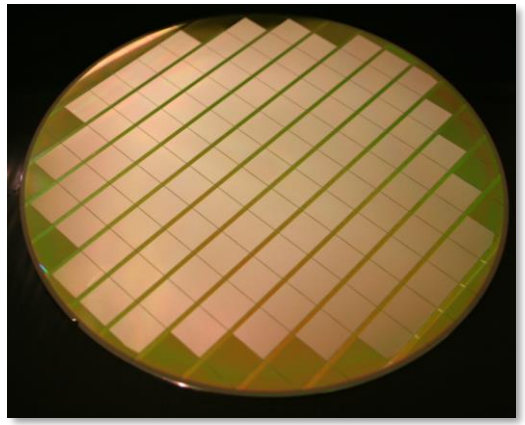
- GaAs, CdTe, CdZnTe, InGaAs

Single chip

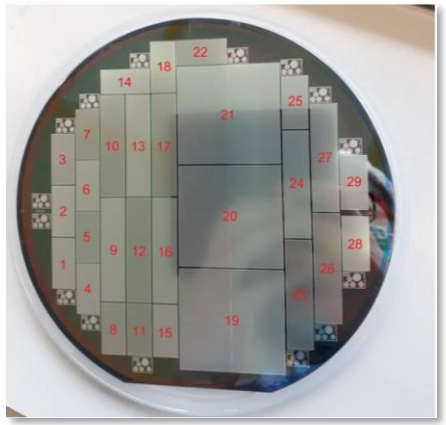
- 65nm/28nm readout chips from MPW
- diced sensor (i.e. 3D diamond)



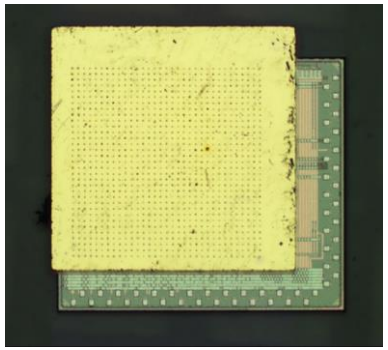
300mm RD53B/ITKPix ROIC wafer with solder bumps



200mm MEDIPIX3 Wafer with solder bumps



150mm FBK planar sensor wafer, 150µm thickness



TIMESPOT ASIC with 3D diamond sensor, both chips processed at single die level

Fabrication Volume: Production Level

CERN ATLAS/CMS ITK Pixel Detector Upgrade

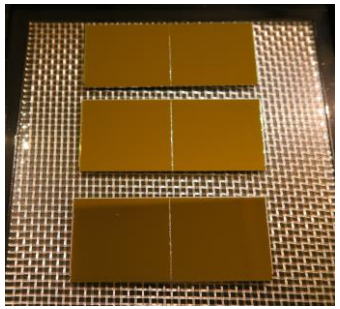
- ITK detector upgrades using hybrid modules with 50x50µm² bumping pitch
- Assembly of 1-chip, 2x1-chip and 2x2-chip hybrid modules:
  - 6“ planar sensors: 100µm, 150µm thickness
  - 4“/ 6“ 3D sensor wafer: 250µm thickness
  - 8“ CMOS sensor wafer: 150µm thickness
- Readout chip size:
  - 300 mm RD53B (ITKPIX) wafer
    chip size ~21x20mm²; thickness 150µm
  - 300 mm CROC wafer
    chip size ~22x19mm²; thickness 150µm
- ITK Detector Upgrade:
  - i.e. ATLAS ITK Pixel: **~10,000 4-chip + 2,150 1-chip modules**

RD53 collaboration
https://rd53.web.cern.ch/RD53/

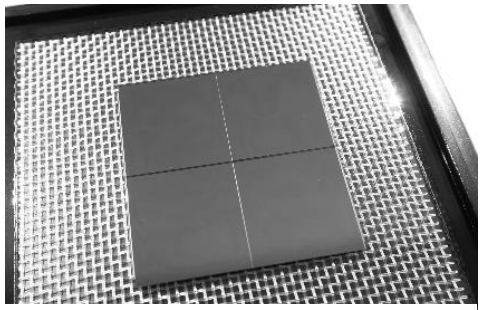
ATLAS collaboration
https://atlas.cern/discover/collaboration

CMS collaboration
https://cms.cern/collaboration

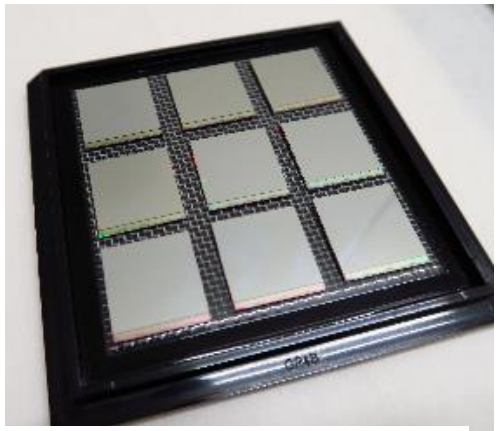
ITKPIX 2x2 hybrid module



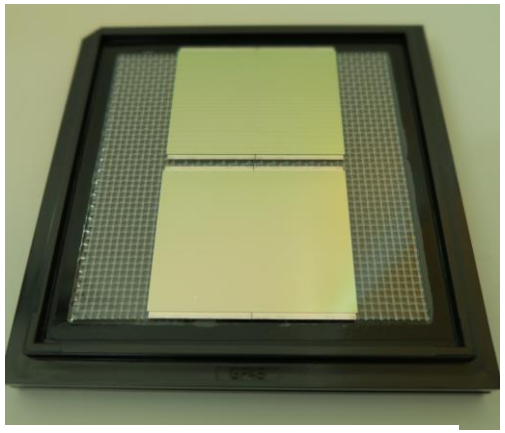
CROC 2x1 hybrid modules



ITKPIX 2x2 hybrid module



ITKPIX 1x1 hybrid modules

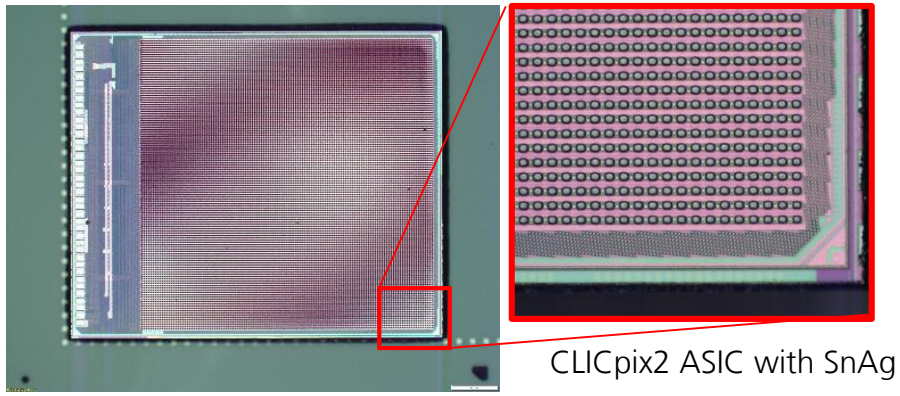


CROC 2x2 hybrid modules

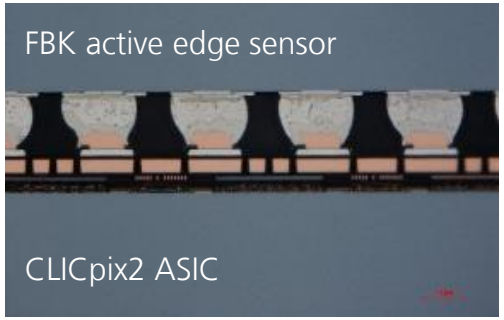
Fabrication Volume: Prototyping Level

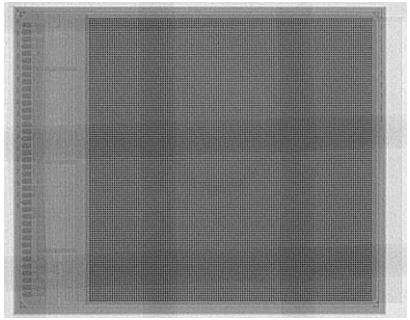
CLICpix2 - 25µm Pitch Single Chip Bumping

- Single Chip bumping of individual die from multi-project wafer (MPW):
  - Aligned chip bonding onto carrier wafer
  - Bumping process using wafer level process line:
    - PVD – mask lithography – electroplating of UBM/solder bump
  - Removal from carrier
- Hybrid module:
  - TSMC 65nm CLICpix2 ROC
  - Bumping 128x128, 25µm pitch, bump size 12µm
  - UBM on FBK active edge sensor:
  - Thickness 50µm, 100µm and 130µm
  - Connection yield up to 99,9%
- PCB assembly, wire bonding & test done at CERN

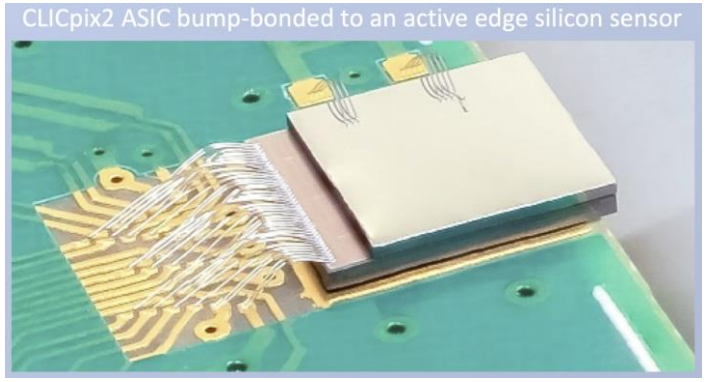


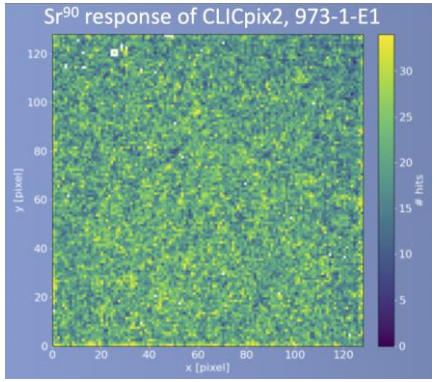
CLICpix2 ASIC with SnAg bumps





X-ray image of CLICpix2 module – no bump shorts visible

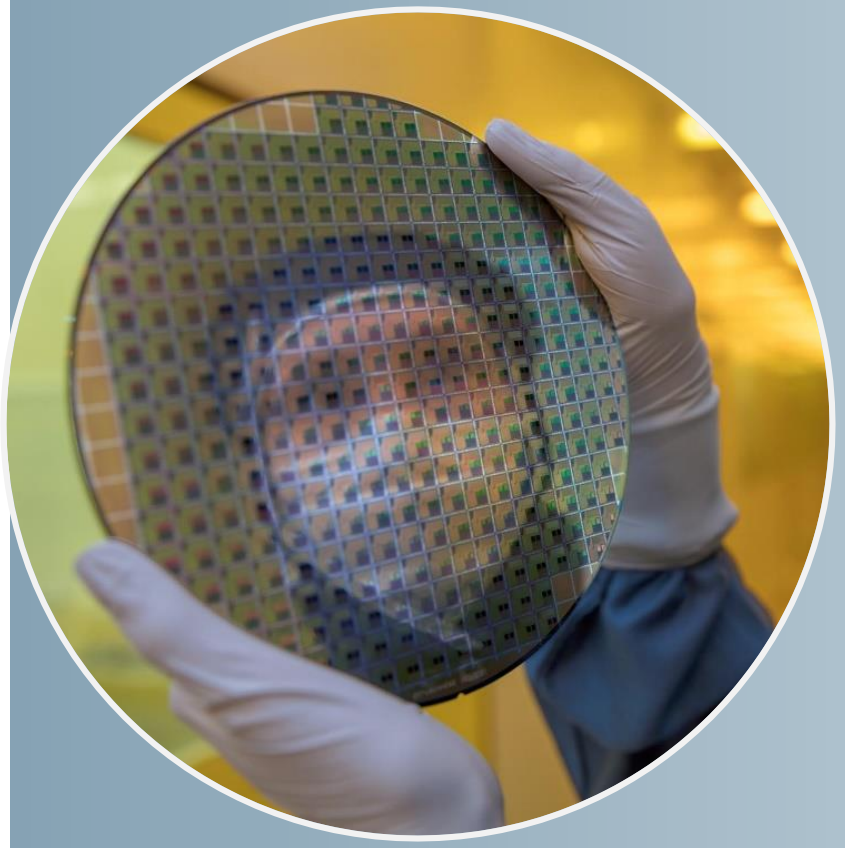




P. Svihra [IWORID 2022]

See also: P. Svihra et al. IWORID 2022
https://doi.org/10.48550/arXiv.2210.02132
arXiv:2210.02132v1 [physics.ins-det] 5 Oct 2022

Outline



- Status Hybrid Pixel Detectors
- **New Developments**
- Trends in Advanced Electronic Packaging

Hybridization: New Interconnection Methodes for Sub-10µm Pitch

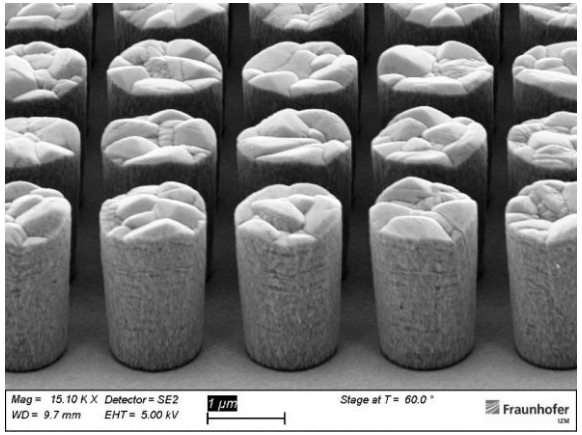
Nano-porous Gold-Pillar-Interconnects

Motivation:

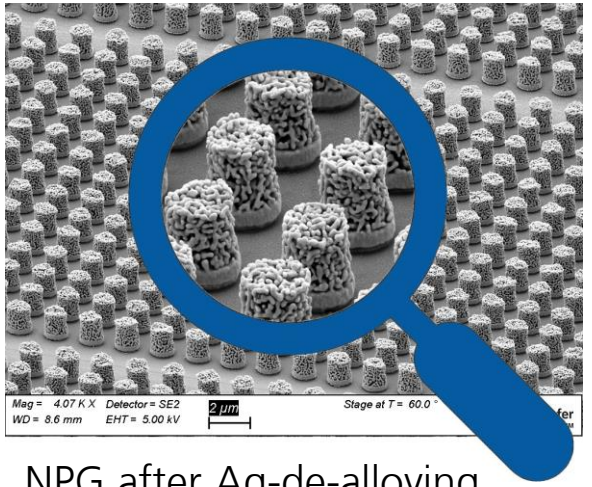
- sponge-like metal for I/O bumps with superior compressible behavior
- Bump deformation in z-axis with less spreading in lateral x/y-direction featuring smallest bump space
- Applicability of reduced bonding parameters like temperature and force

Features:

- Electro-plating of Au/Ag pillars and de-alloying of Ag results in sponge like Au-bump (nano-porous-gold – NPG)
- Bump size ~2µm, bump pitch 4µm

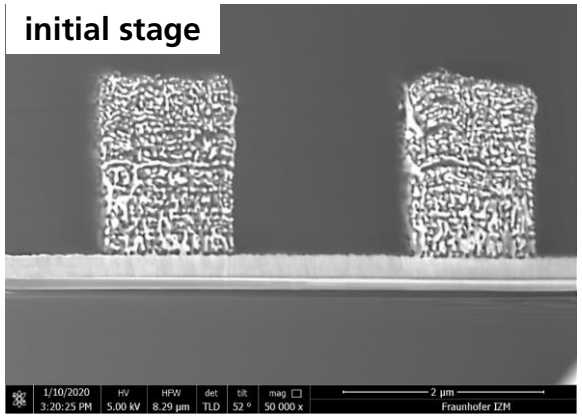


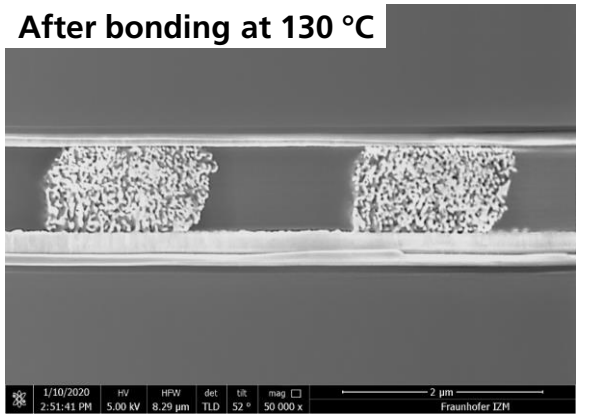
Au/Ag pillars as plated



NPG after Ag-de-alloying

NPG µ-bumps before and after thermo-compression bonding





Advanced Bonding Technologies

Metal-Oxide-Hybrid-Bonding

Motivation for DBI®

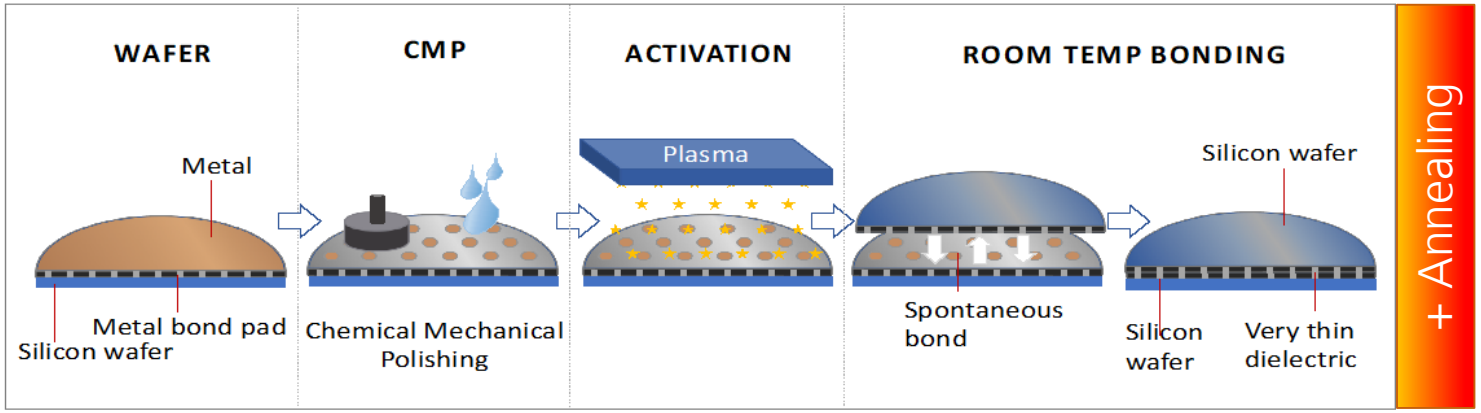
- W2W , D2W, D2D
- Highest interconnect density: I/O pitch down to 1 µm
- High alignment accuracy
- No bumps, no intermetallics
- No gap – no underfilling
- 3D chip stacking: memory chips, CMOS image sensors (CIS)

Process

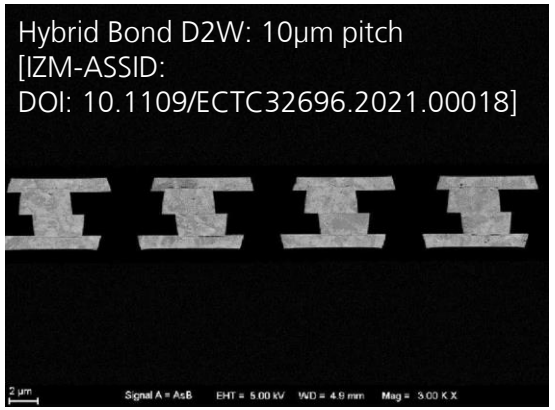
- SiO2 passivation + Cu pads
- Surface planarization (CMP)
- Surface activation (plasma, chemicals)
- Room temperature bond
- Annealing 200 – 350°C

Challenges

- Particle free surface required
- Cu-Oxide surface roughness <1nm
- Cu dishing ≤ 5nm
- Delicate die and wafer handling to avoid contamination and particles
- Processes licenced by XPERI/ADEIA:
  - DBI-Ultra: D2W HB, DBI: W2W HB
  - Zi-Bond: W2W DB



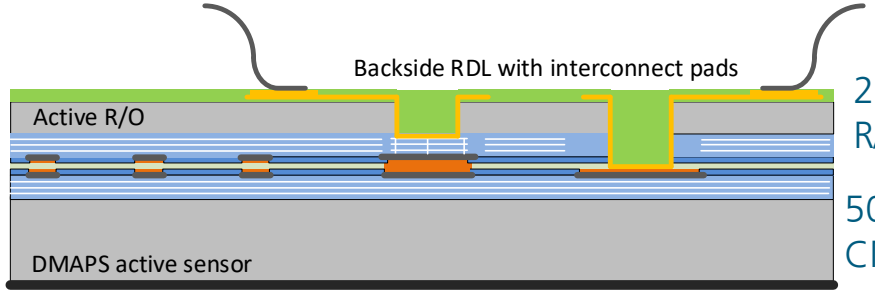
Drawing by F.Huegging, University of Bonn



IEEE 72nd ECTC 2022: papers from AMD, Samsung, Sony, Xperi, Applied Materials, SK Hynix Semiconductor, …

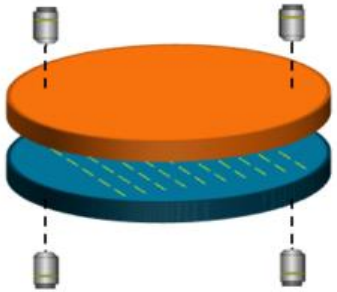
Advanced Bonding Technologies

AIDAinnova: Ultra Thin Hybrid Pixel Detectors



20 µm
R/O electronics

50 -100 µm
CMOS sensor

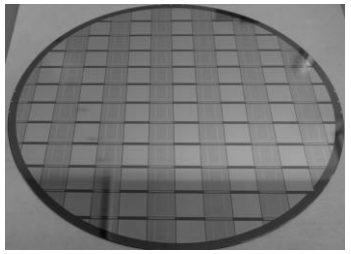


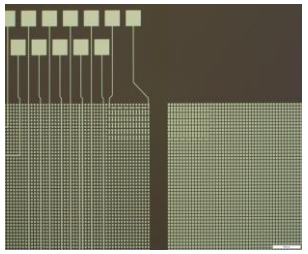
Task 6.4: Wafer to wafer bonding technique

Slides: F. Huegging (Bonn), I. Gregor (DESY&Bonn), T. Fritzsch (IZM)

Features:

- R/O backside redistribution layer (RDL) with contact pads
- Thinned R/O wafer (i.e. TIMEPIX3) with backside via last interconnection
- Combined polymer – metal - bonding
- Thin DMAPS sensor with contact pads and backside processing

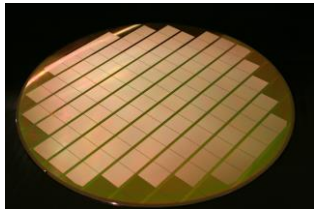




Process setup
wafer from IZM

Tasks:

- Fabrication of technology development and characterization wafer by Fraunhofer IZM
- W2W bonding process development by Fraunhofer IZM
- TIMEPIX3 wafer provided by CERN MEDIPIX collaboration
- TIMEPIX3 adapted sensor design by University of Bonn
- 200mm sensor wafer fabricated by Lfoundry



TIMEPIX wafer
from CERN

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

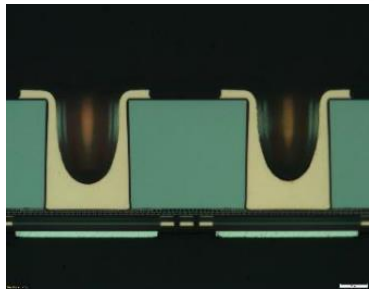
3D Integration Technologies

TSV in electronic readout chip wafer – TSV backside via last process

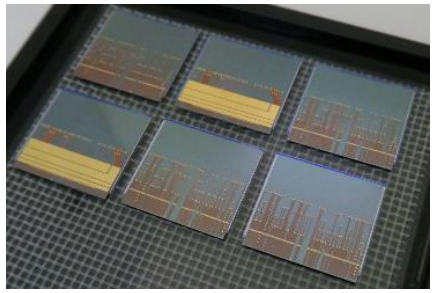
UNIVERSITÄT BONN

DESY

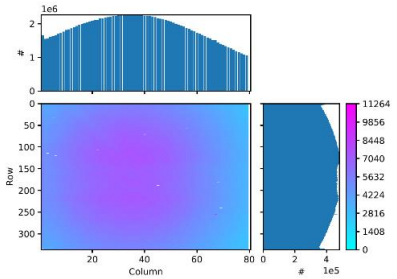
ATLAS FE-I4



TSV Ø60µm, wafer thickness 80µm



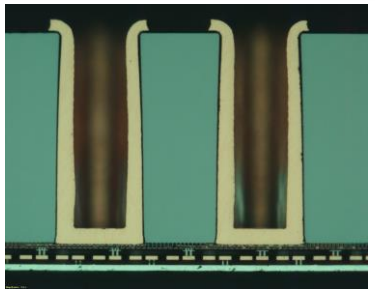
ATLAS FE-I4 TSV single chip modules



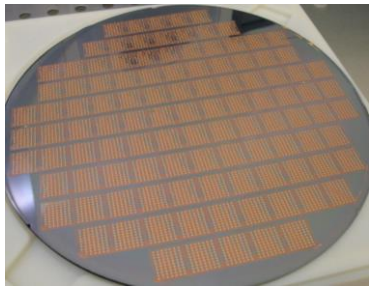
Source scan: Sr90, 60s, 60V

[JINST 2022: https://doi.org/10.1088/1748-0221/17/01/C01029]

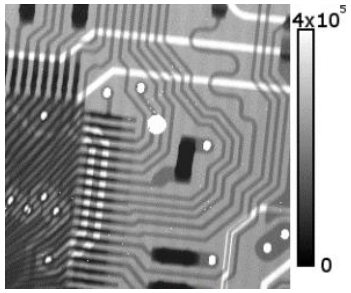
MEDIPIX3



TSV Ø40µm, wafer thickness 100µm



MEDIPIX3 TSV wafer view onto BS-RDL



PCB sample imaged with X-ray tube, Mo target, 51 kV

[2017 JINST 12 C12042]

- TSV backside, via last process
- TSV connection to CMOS M1 layer landing pad
- Level 1 assembly: TSV readout chips flip chip bonded onto silicon sensor chip
- Level 2 assembly: module assembly onto PCB and functional test at project partner side: ATLAS/University of Bonn, MEDIPIX3/DESY
- Ongoing projects:
  - TSV backside via last process in TIMEPIX4 wafer with CERN/MEDIPIX collaboration
  - Current status: TSV metallization process ongoing
  - MEDIPIX3 TSV projects with industry partners

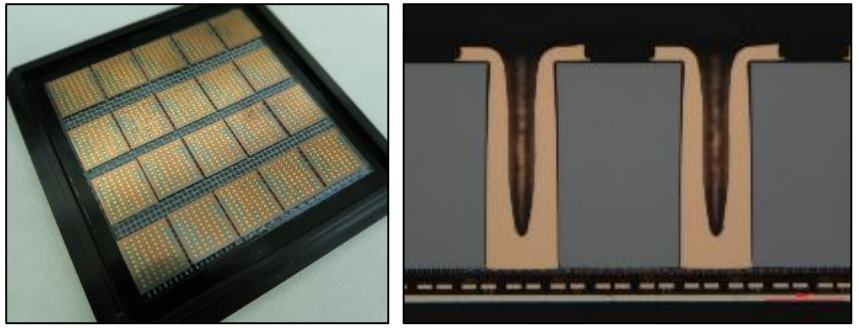
In cooperation with: AMSTERDAM SCIENTIFIC INSTRUMENTS

MEDIPIX3 TSV based 1MPix Electron Microscope Camera

Project: Amsterdam Scientific Instruments – MEDIPIX3 TSV Process and Module Assembly

Project Goal

- Development and fabrication of MEDIPIX3 X-ray camera with TSV
- 1MPix gap-less camera image by combination of MEDIPIX TSV chips and edgeless silicon sensor chips



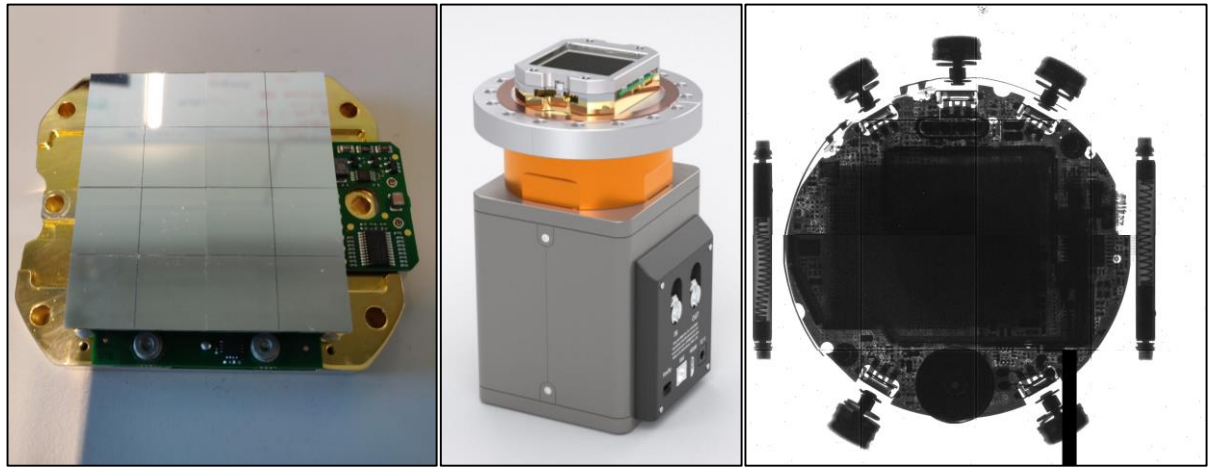
MEDIPIX3 chips after TSV process

Contribution of the Fraunhofer IZM

- TSV backside - via last process at IZM using MEDIPIX3 readout chip wafer
- Flip Chip Assembly onto Si-pixel sensor chips with SnAg bumps
- Level2-Assembly onto connector substrate

ASI: 1MPix Electron Microscope Camera Features

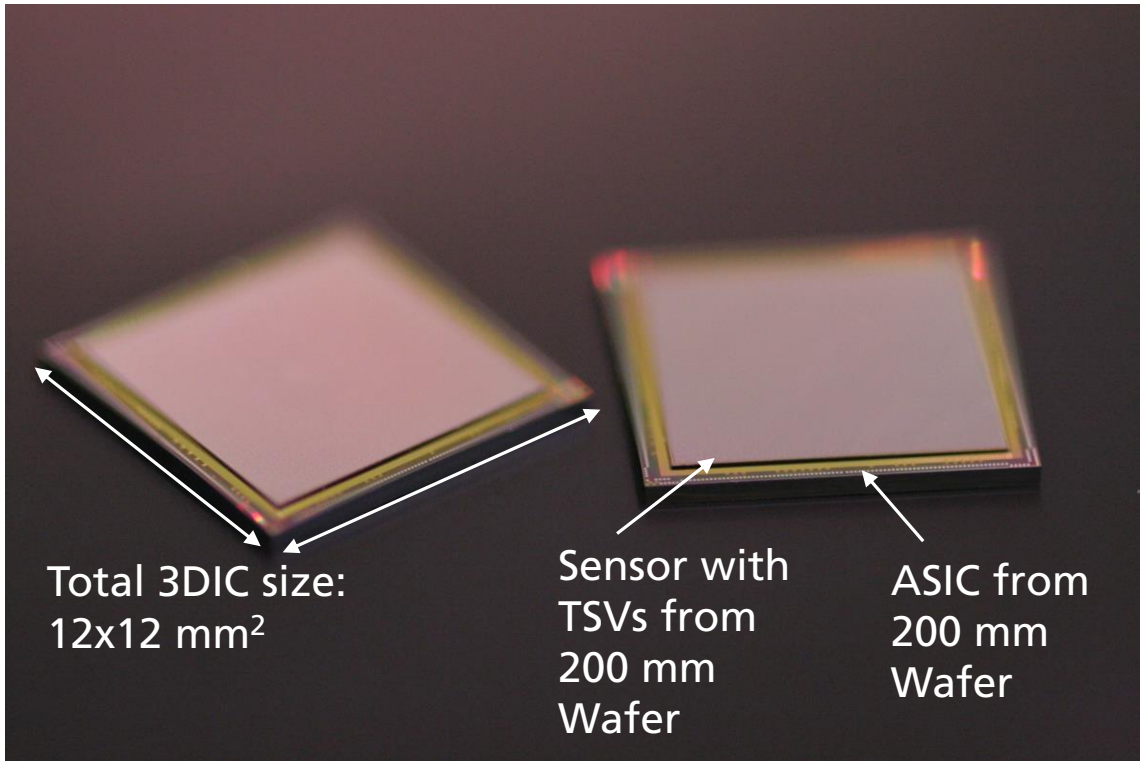
- 1024x1024 pixels full detector area (56 x 56mm²)
- 4x4 single MPX3 TSV modules assembled without gaps
- 300 µm edgeless silicon sensor (200 kV electron microscope)
- Fits on CF100 standard flange for mounting in a TEM

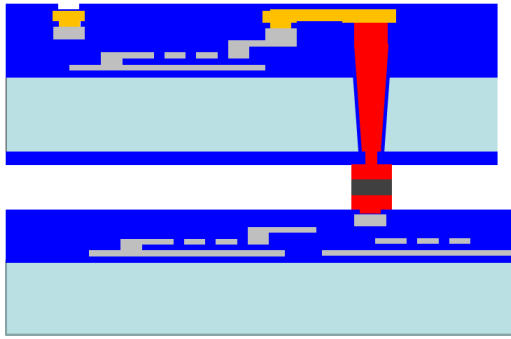


1MPix camera assembled at ASI and x-ray test image of a watch

3D Integration Technologies

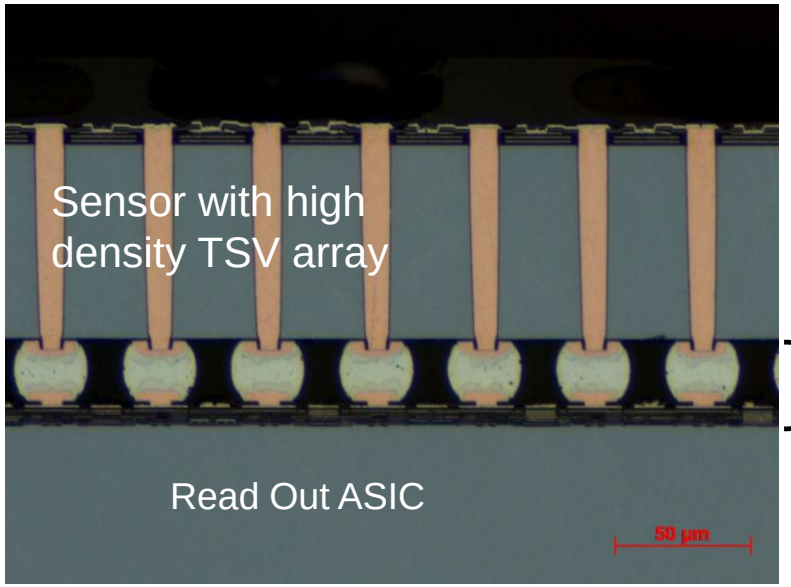
TSV in SPAD sensor array – TSV frontside via last process





80 µm thick SPAD Sensor Array with 256x256 pixels with TSVs (pitch 40µm)

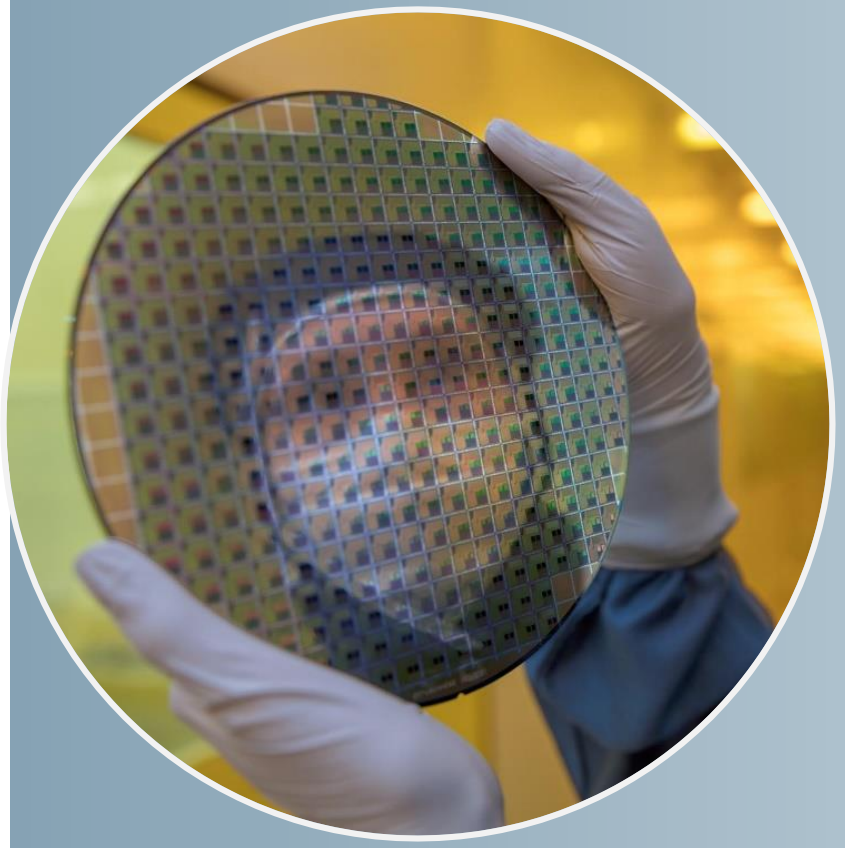
Read Out ASIC



Micro solder bump connections with 40 µm pitch

Example:
3DIC of SPAD Sensor Array with TSVs on ASIC for LIDAR Applications

Outline



- Status Hybrid Pixel Detectors
- New Developments
- Trends in Advanced Electronic Packaging

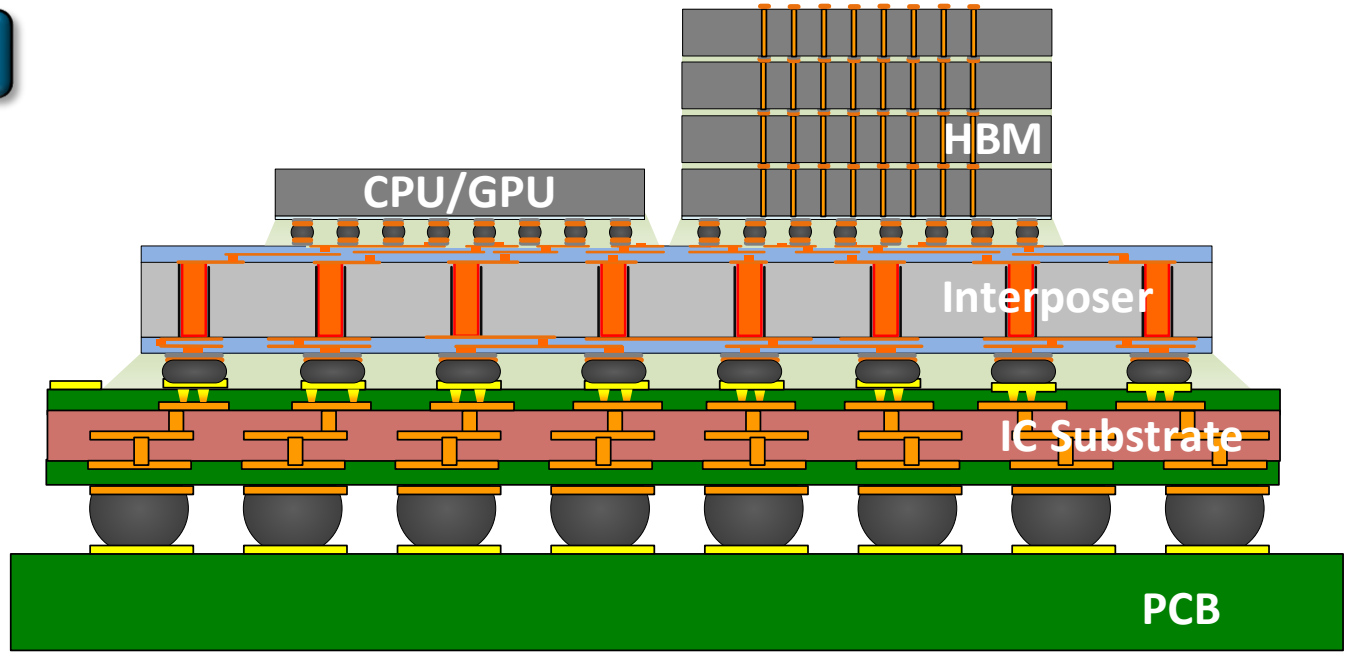
Advanced Electronic Packaging

3D/2.5D Package for High-End Performance Applications

TSVs

HBM TSV:
Diameter 6µm
Height: 55µm
Pitch: 50µm

Interposer TSV:
Diameter 10…15µm
Height: ~100µm
Pitch: 75…225µm



Interconnects

HBM stack
Diameter 20µm
Pitch 48µm

CPU/GPU/HBM to Interposer
Diameter ~25µm
Pitch 95µm

Interposer to IC substrate:
Diameter 100µm
Pitch 200µm

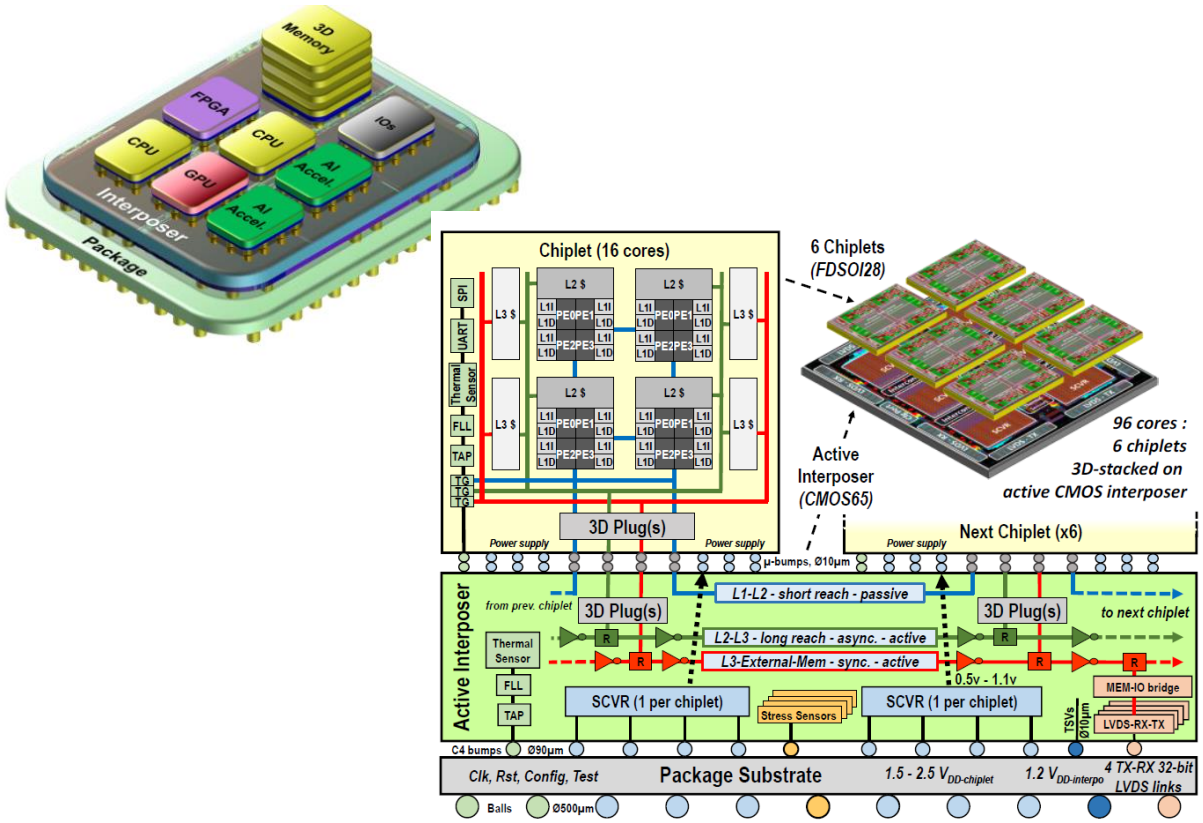
Datacenter Networking | **High-Performance Computing** | **Autonomous Vehicles**

Developed by global players like SAMSUNG, INTEL, AMD, TSMC

Numbers according to High-End Performance Packaging: 3D/2.5D Integration 2022 | Report | www.yole.fr

Advanced Electronic Packaging

Processor Chiplet Assembly on Active Interposer



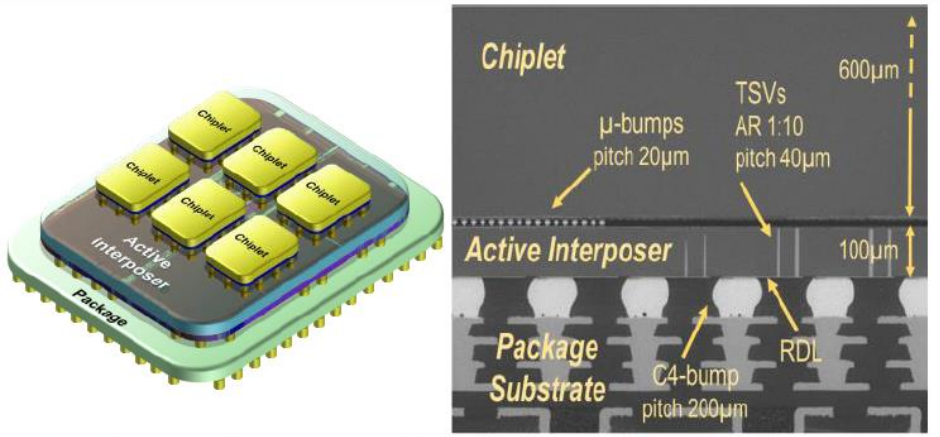


Fig. 5. INTACT : from concept to 3D-cross section

TABLE I: INTACT MAIN CIRCUIT FEATURES AND 3D TECHNOLOGY DETAILS

Chiplet technology	FDSOI 28nm, 10 metals, 0.5V-1.3V+adaptive biasing
Chiplet area	4.0 mm x 5.6 mm = 22.4 mm^2
Chiplet complexity	395 Million transistors, 18 transistors/µm^2 density
Interposer tech.	CMOS 65nm bulk, 7 metals, MIM option, 1.2V
Interposer area	13.05 mm x 15.16 mm = 197.8 mm^2
Interposer complexity	15 Million transistors, 0.08 transistors/µm^2 density
3D technology	Face2Face, Die2Die assembly onto active interposer
µ-bump technology	Ø10µm, pitch 20µm
#µ-bumps	150 000 (20k signals + 120k powers + 10k dummies)
Inter-chiplet distance	800µm
TSV technology	TSV middle, Ø10µm, height 100µm, pitch 40µm
#TSV	14 000 TSV (2 000 signals + 12 000 power supply)
Backside RDL	10µm width, 20µm pitch
C4-bumps	Ø90µm, pitch 200µm, 4,600 bumps
Flipchip package	BGA 39 x 39, 40mm x 40mm, 10 layers
Balls	Ø500µm, pitch 1mm, 1 517 balls

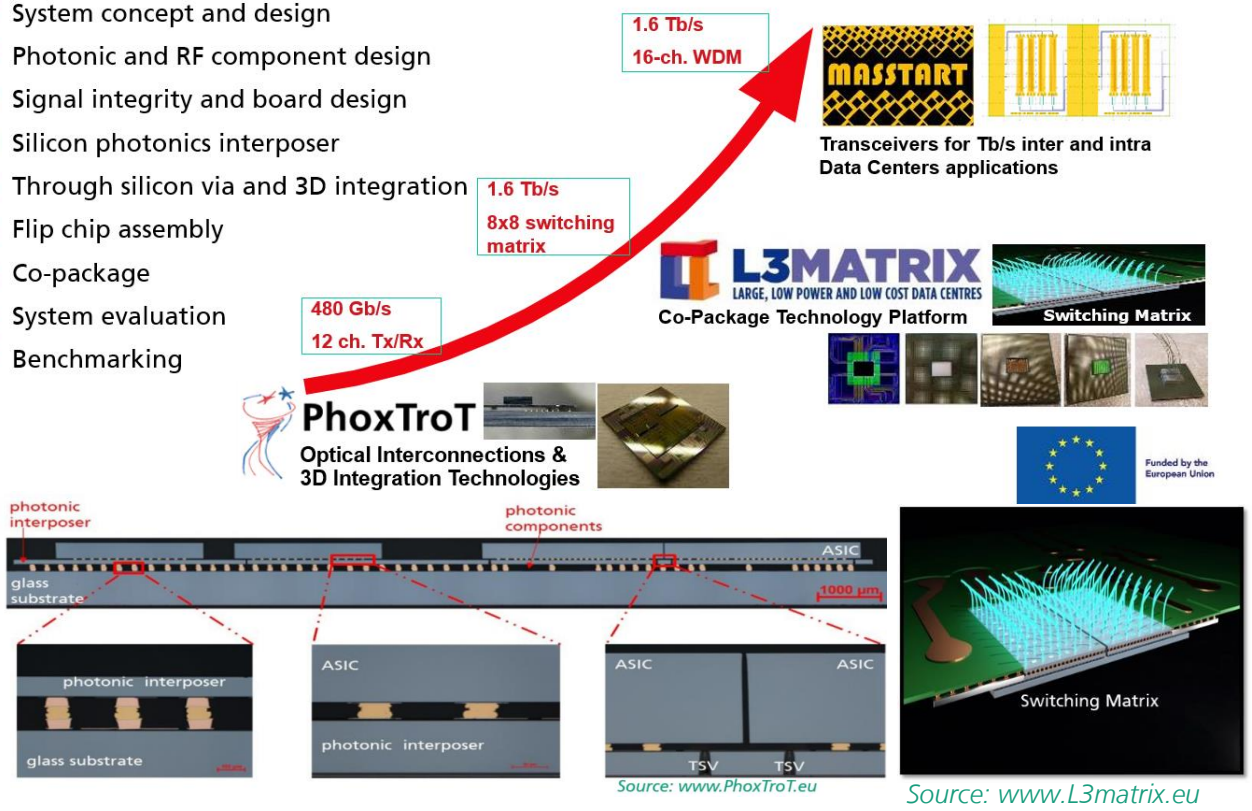
Pascal Vivet, Eric Guthmuller, Yvain Thonnart, Gaël Pillonnet, Cesar Fuguet, et al.. IntAct: A 96-Core Processor With Six Chiplets 3D-Stacked on an Active Interposer With Distributed Interconnects and Integrated Power Management. IEEE Journal of Solid-State Circuits, Institute of Electrical and Electronics Engineers, 2020, pp.1-1. 10.1109/JSSC.2020.3036341 . hal-03072959

Advanced Electronic Packaging

Photonic Integration Technology

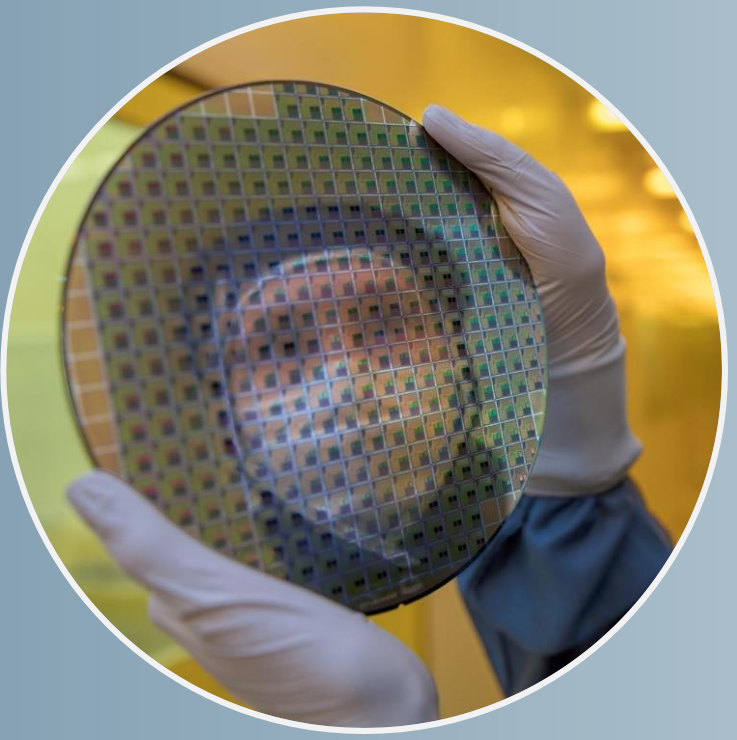
Empowering Photonic Interconnects for Data Center and NGC

- System concept and design
- Photonic and RF component design
- Signal integrity and board design
- Silicon photonics interposer
- Through silicon via and 3D integration
- Flip chip assembly
- Co-package
- System evaluation
- Benchmarking



- High data rate communication using Photonic IC (PIC)
- Drivers in Industry: next generation computing - cloud, edge, node HPC
- Electrical and optical integration on silicon photonic interposer and PIC
- Optical off-chip interconnection for chip-to-chip communication: low-latency, high-bandwidth, high density, low power
- Massive switching beyond 400 Gb/s with new developed Serializer/Deserializer circuits and optical links
- How to enable mass-manufacturing of datacom photonics products? – lower cost, lower power consumption, higher reliability

Summary



- Current hybridizaton projects cover the range from 300mm wafer to single chip processing: requires a high level of flexibility in your process line
- Requested module numbers from several thousand to only one prototype: requires capabilities for volume production and process slots for R&D projects
- Interconnection pitch one benchmark for flip chip product developments: interconnection pitch reduction from 50µm pitch to sub-10µm pitch
- New developments in bonding technologies and integration: cover C2C, C2W and W2W bonding, 3D integration and chip stacking
- Advanced packaging developments ongoing for high preformance computing: 3D/2.5D system in package, chiplet integration, silicon photonics integration, qubit-chip packaging

Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

Thank you for your attention!

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Backup

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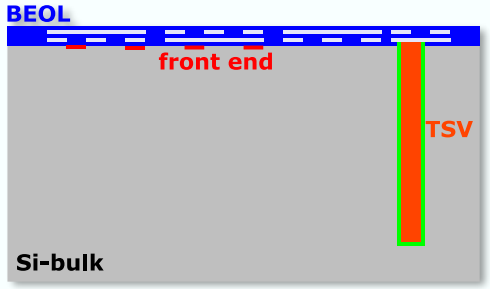
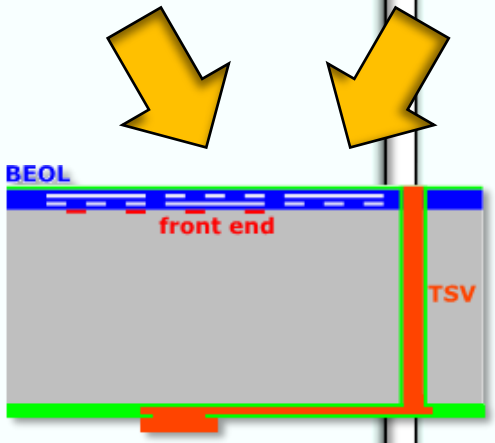
TSV Integration Schemes

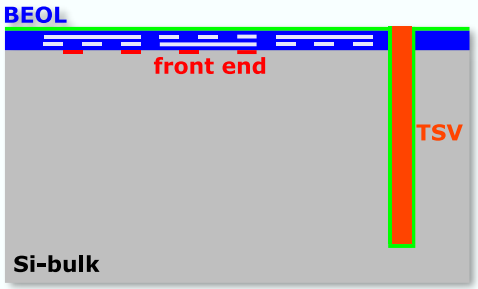
Via middle



- TSV integration after FEOL / before BEOL
- Processes established at IDMs, in production for HBM stacks



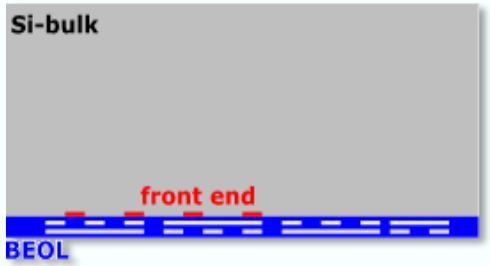
Front Side - Via last



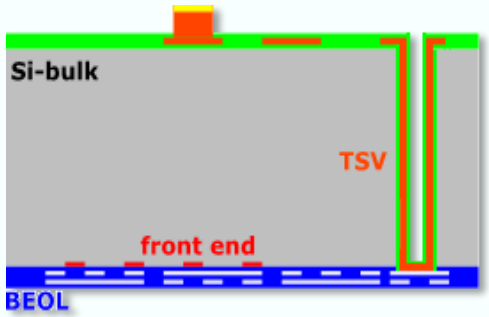
- TSV integration after complete wafer processing
- TSV through thick BEOL oxide
- Requires keep out zones in FEOL and BEOL for TSV integration

- Support wafer bonding
- Wafer backside thinning
- TSV reveal
- Backside RDL and bump formation
- Support wafer de-bonding

Back Side - Via last



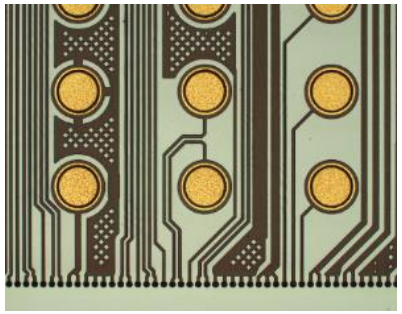
- TSV integration after complete wafer processing
- Requires TSV adapted landing pad design in BEOL for TSV connection



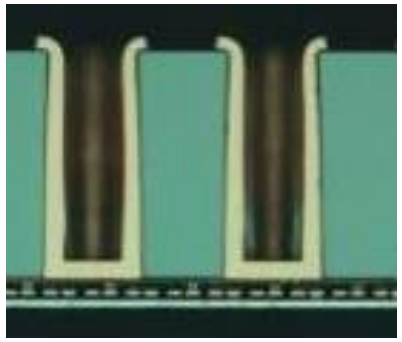
- Support wafer bonding
- Wafer backside thinning
- TSV formation with access to landing pads
- Metall liner and back side RDL formation
- Support wafer de-bonding

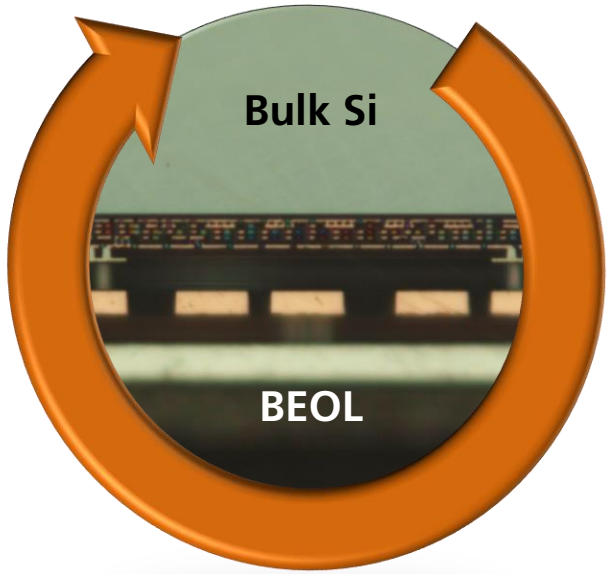
Basic Process Steps of TSV Formation – Back Side Via Last

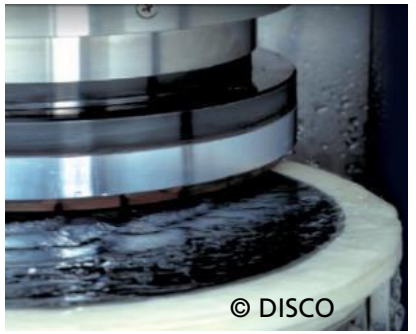
8. Backside Passivation and Bond Pad UBM



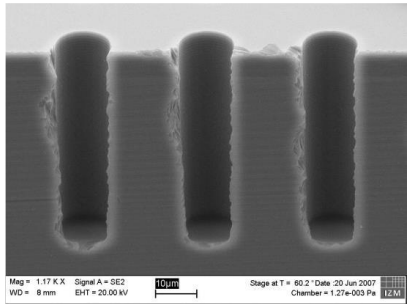
7. TSV Cu filling + RDL Cu by ECD



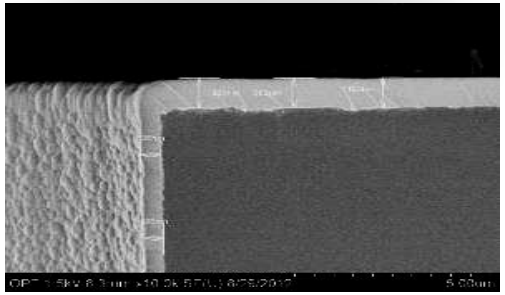




1. Frontside process / carrier wafer bonding
2. Si- wafer thinning



3. TSV silicon etching DRIE BOSCH Process

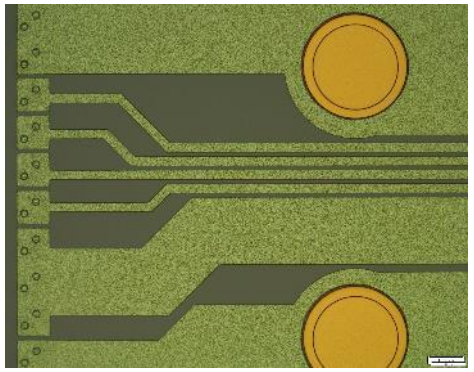


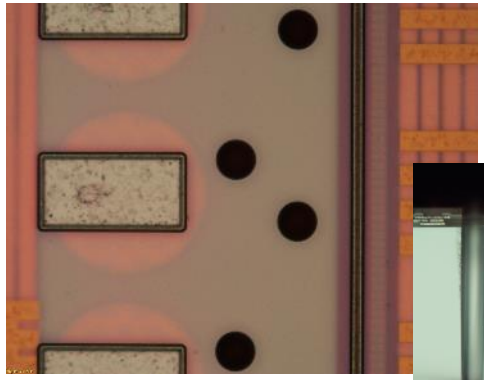
4. TSV and wafer surface oxide passivation TEOS, PE-CVD, SA-CVD
5. Oxide Etch at via bottom

6. Barrier-/Seed-Layer Ti (TiW, TiN, Ta(N)) / Cu HI-PVD

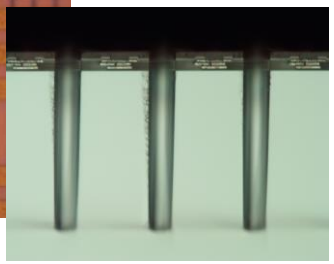
Basic Process Steps of TSV Formation – TSV Frontside – Via Last

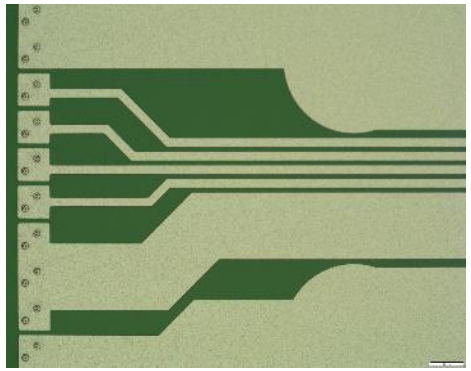
11. Passivation
12. BGA Bump Pad Formation



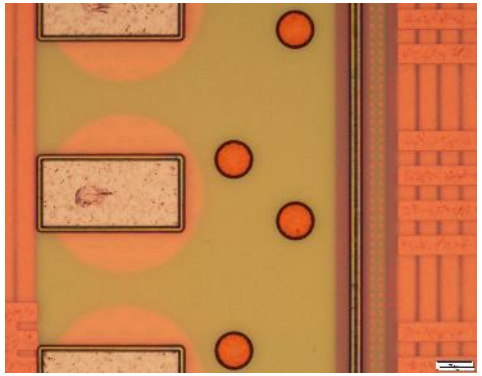


1. TSV blind hole etch and isolation

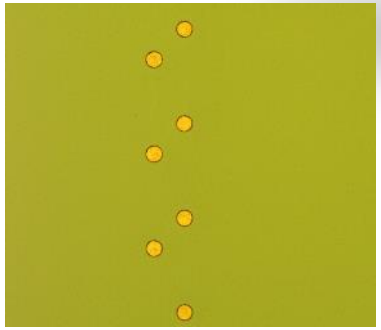




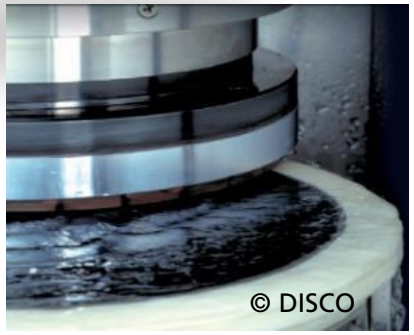
9. Passivation Opening
10. Back Side RDL



2. TSV filling
3. Front side RDL
4. Front Side Passvation / IO Formation



7. TSV Reveal
8. Back Side Passivation



5. Temporary bonding
6. Si- wafer thinning