Germanium Charge-Coupled Devices

Christopher Leitz (on behalf of the germanium imagers team)

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Unique Focal Planes in Support of National Security and Science

MIT KAVLI INSTITUTE

Space Surveillance

Astronomy & Near Earth Object Detection

Space-Based Astronomy

AMOS (AF)

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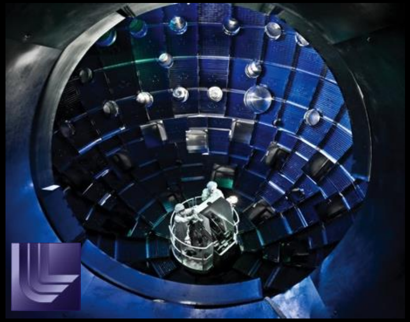
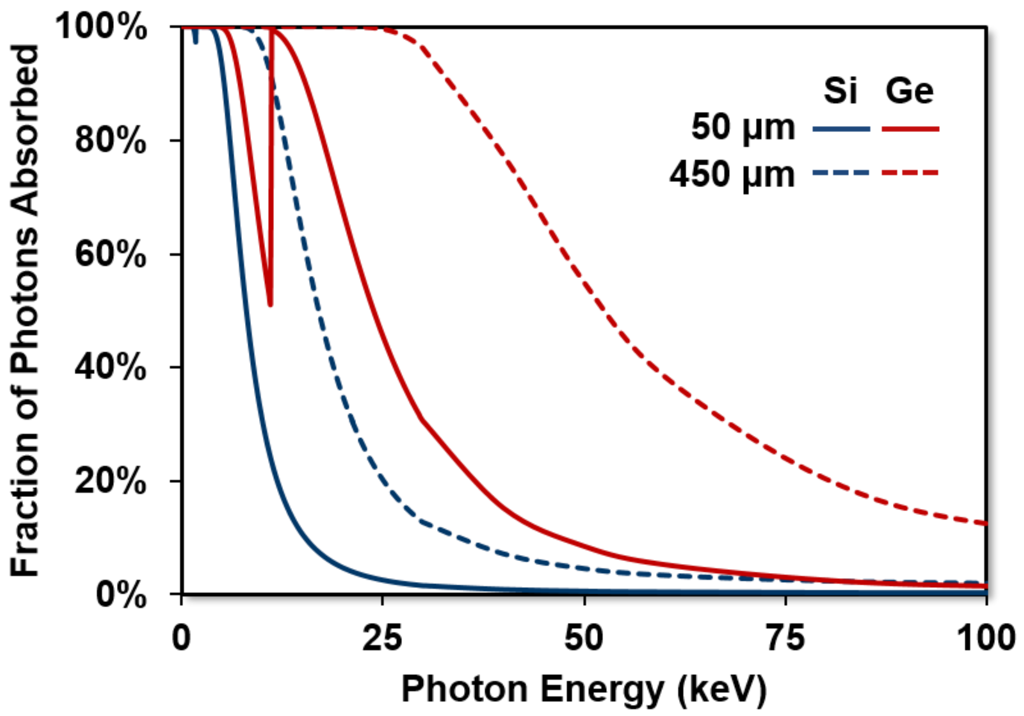


National Ignition Facility (LLNL)

Nuclear Stockpile Stewardship (LANL)

Germanium Detectors Opportunity

X-Ray Sensitivity Comparison



- Elemental high-Z detector material with broadband sensitivity

MITLL Microelectronics Laboratory

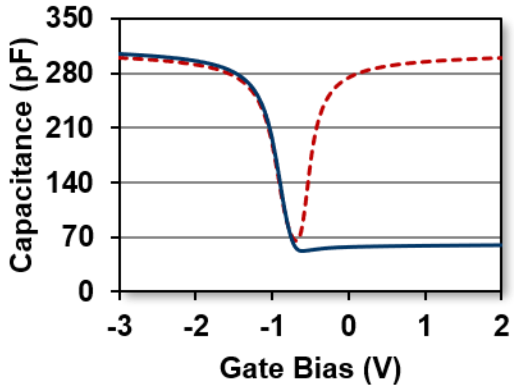
- Germanium wafers processed in same tools used to build silicon detectors for flight missions

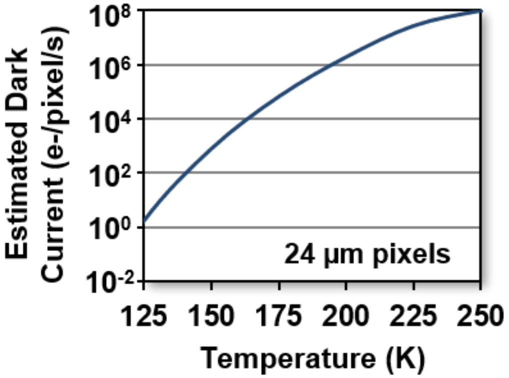
Vision: extend the advantages of CCDs (format, noise…) into new material

Germanium CCD Development Timeline

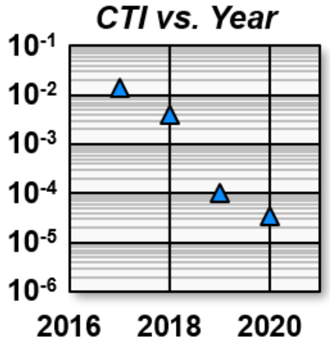
2013 | 2015 | 2017 | 2020+

Test Devices



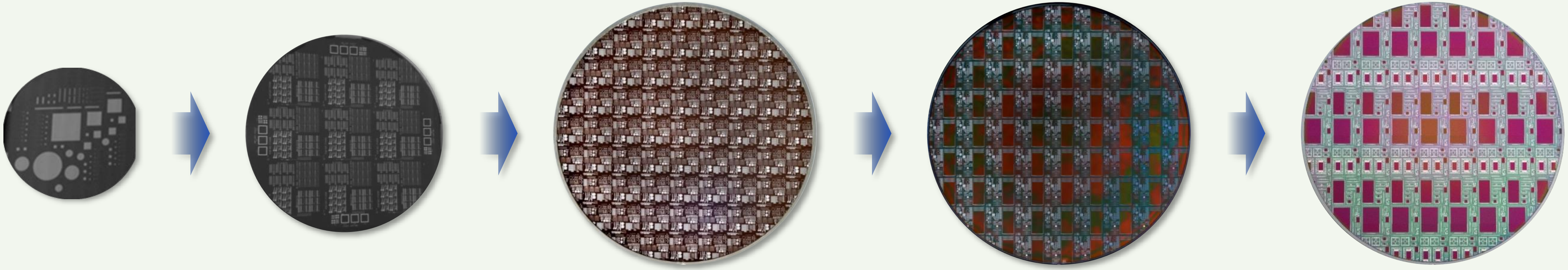


1st-Gen Imagers



2nd-Gen Imagers

Area of current focus



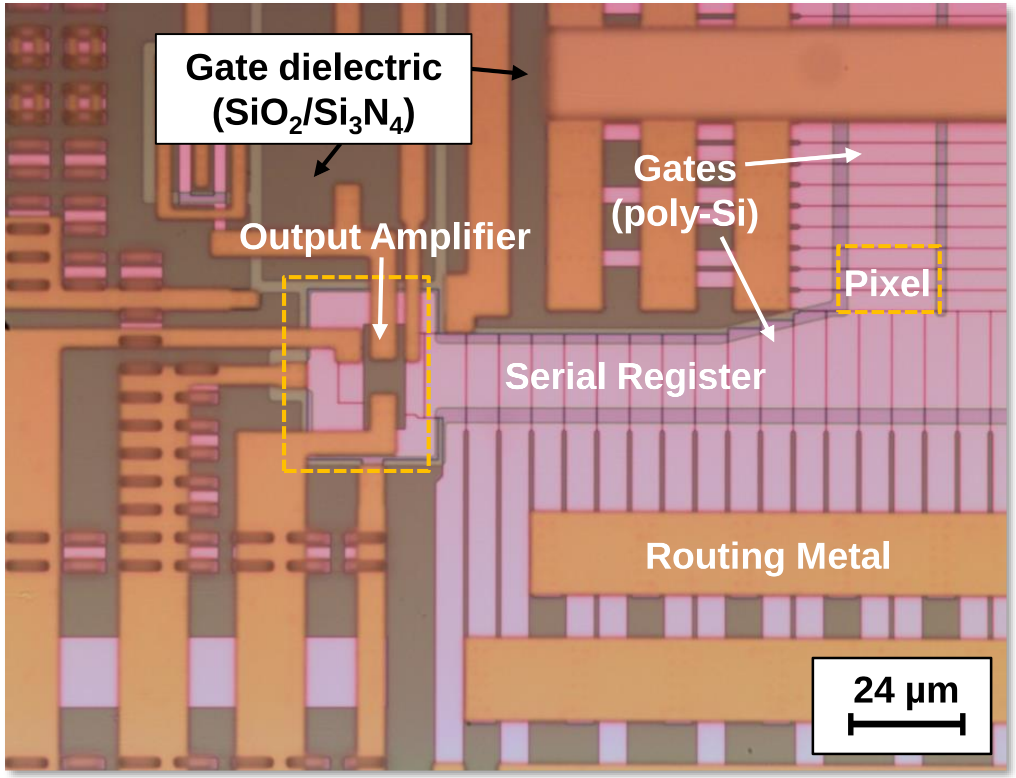
CTI = Charge-Transfer Inefficiency

C.W. Leitz, *SPIE Proc.* **11454** (2020) C.W. Leitz, *SPIE Proc.* **11118** (2019); C.W. Leitz, *SPIE Proc.* **10709** (2018); C.W. Leitz, *J. Inst.* **12**(5) CO5014 (2017).

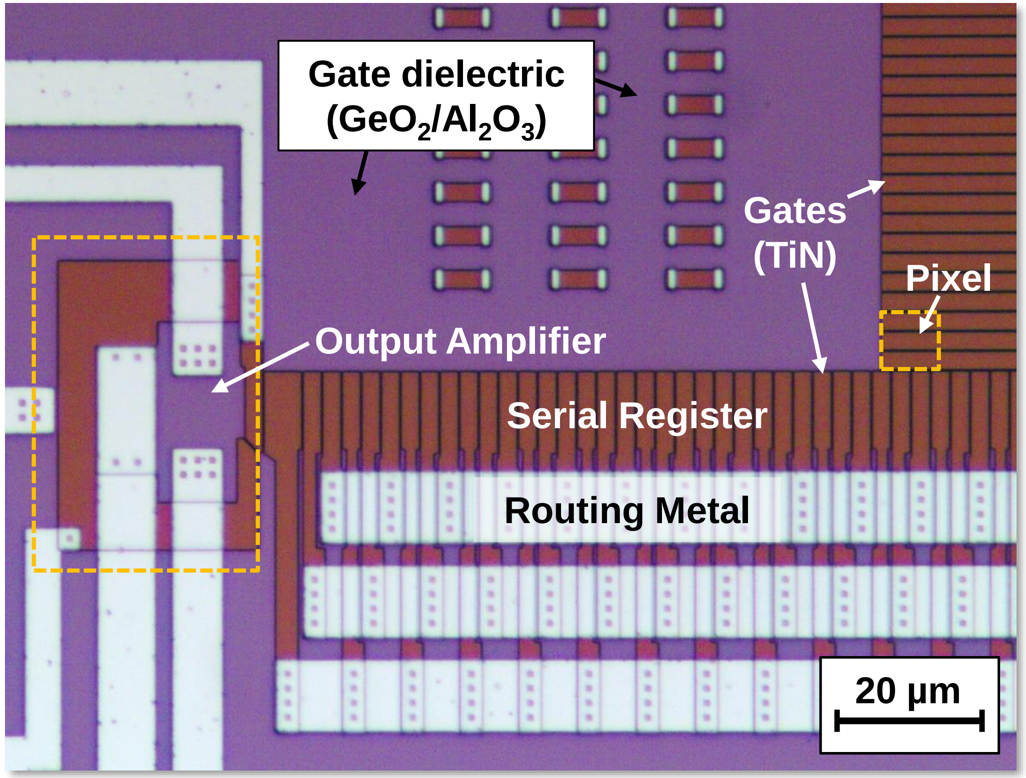
Silicon and Germanium CCD Comparison

Germanium CCDs draw upon long heritage of silicon CCD designs and processes

Silicon CCD



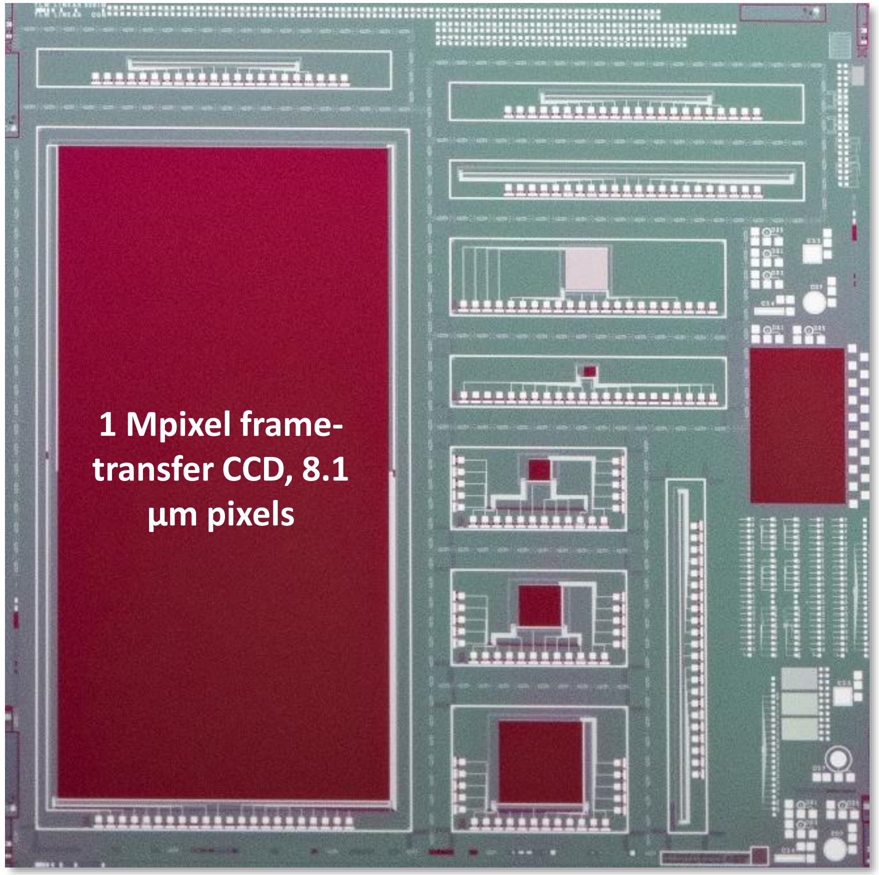
Germanium CCD

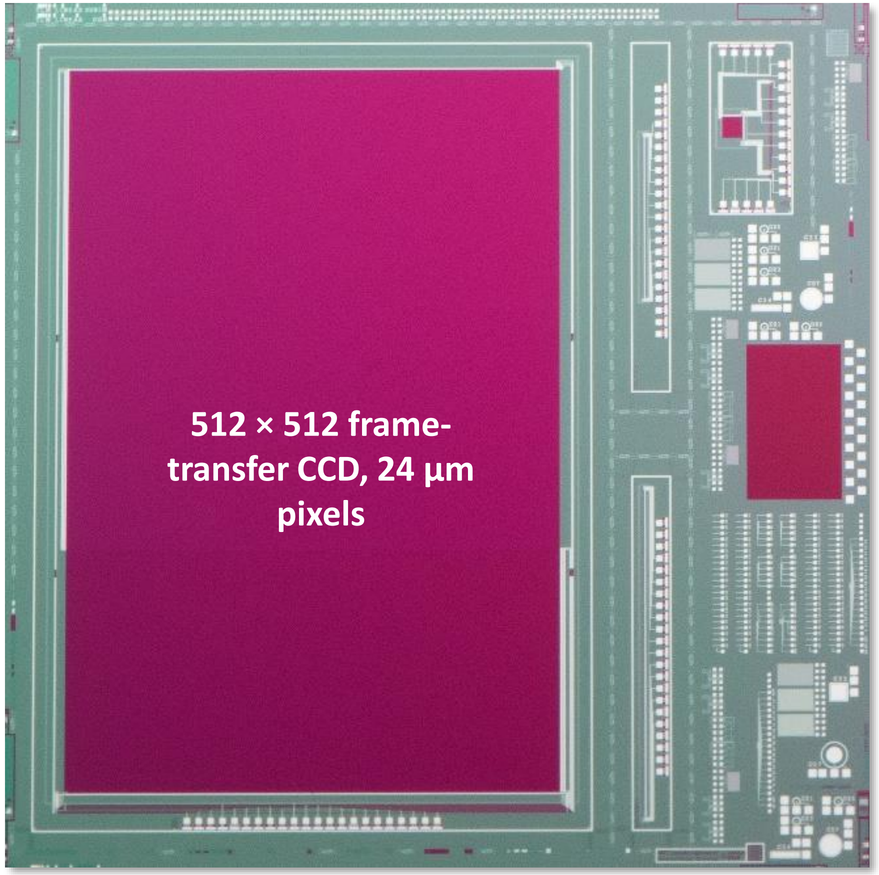


Outline

- Background and motivation
- Status of technology development
  - 2nd-generation imager design
  - First batch of wafers (“pilot wafers”) & yield enhancement
  - Latest batch of wafers
- Plans for FY23 and beyond

Second-Generation Imagers

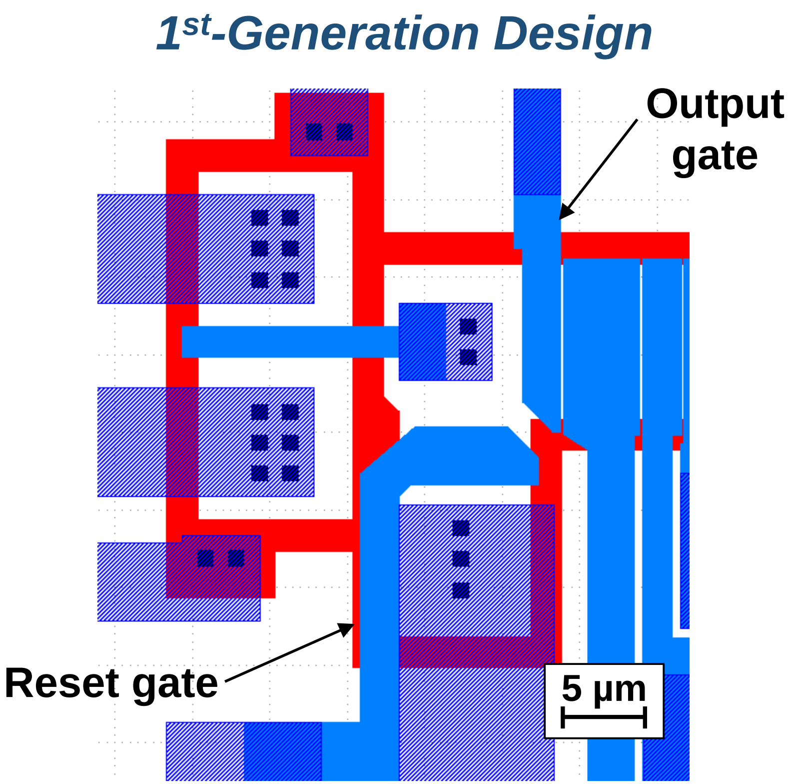


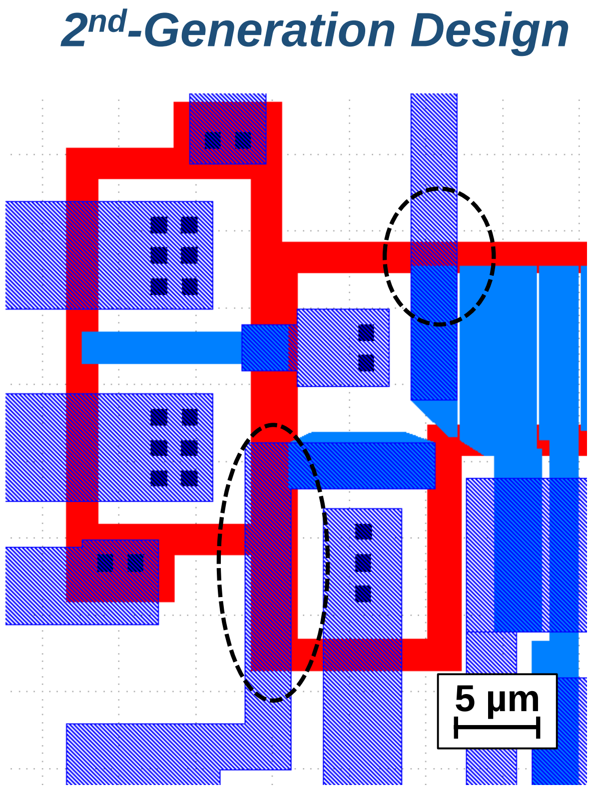


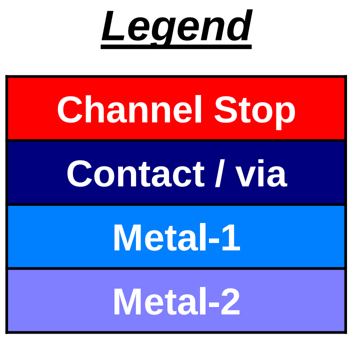
- **512 × 512 frame-transfer CCD with 24 µm pixels, two MOSFET outputs**
- **256^2, 128^2, 64^2 full-frame CCDs with 8.1 µm pixels, one MOSFET & one JFET output**
- **Key yield diagnostic testable at metal-1**

Wide range of new devices, reflecting lessons from first-generation imagers

Elimination of Parasitic MOSFET in Output Region



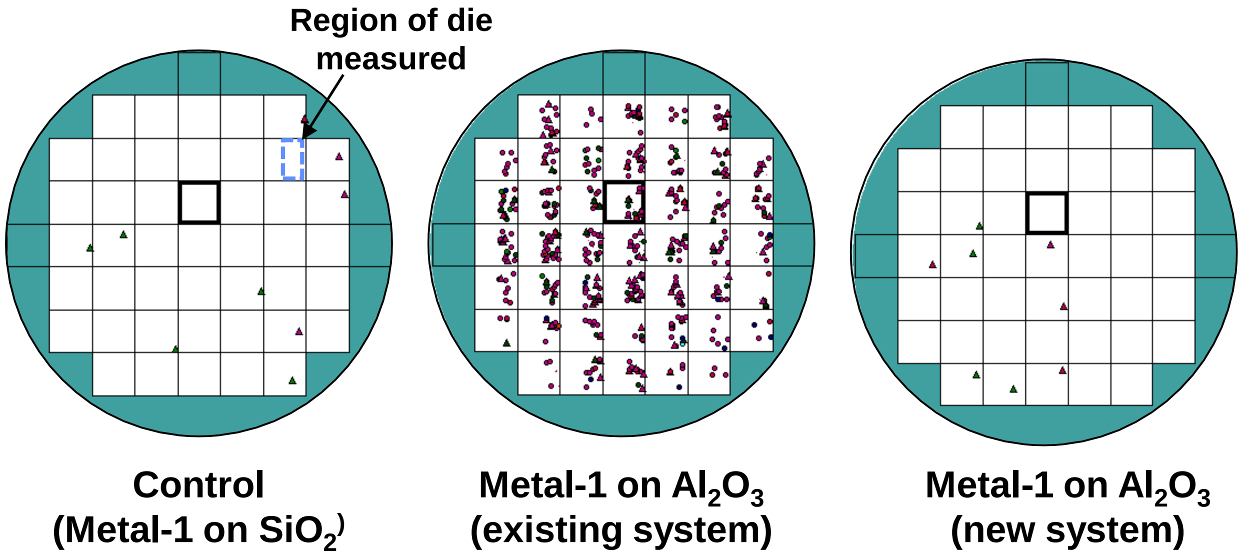




Rerouted metal-1 features to eliminate parasitic transistors to further improve device performance

New Al_2O_3 Deposition System

Defect Maps



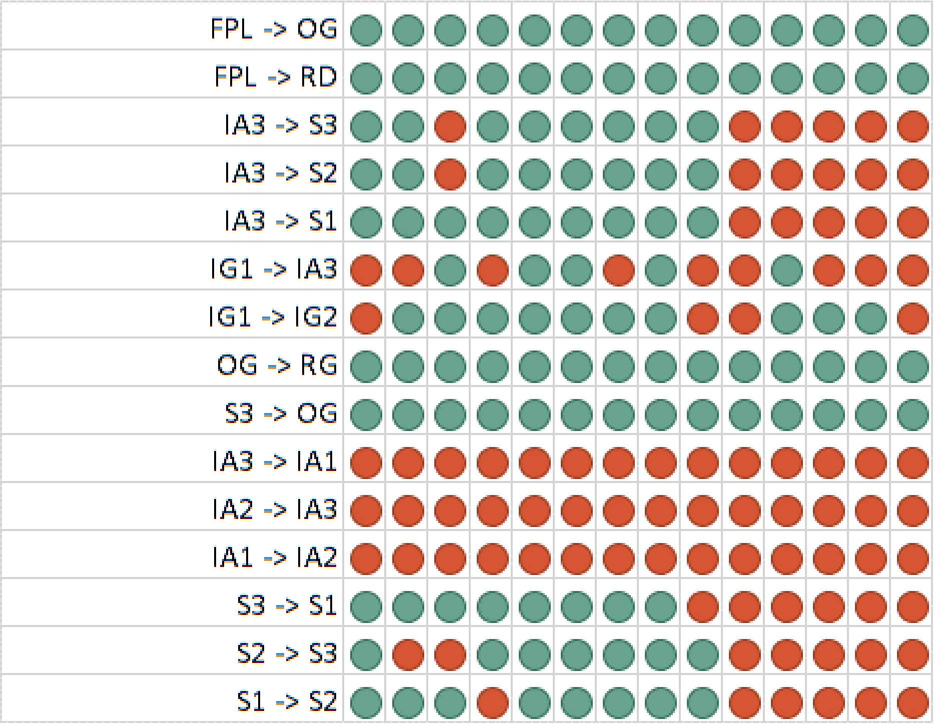
- **Particles from previous Al_2O_3 deposition system caused patterning defects which short phases of device**
- **New system with vastly lower particle counts installed and qualified in late 2020**

New, more capable Al_2O_3 deposition system used on four pilot wafers

Shorts-Opens Test Summary on Pilot Wafers

Shorts/opens testing showed poor yield on pilot wafers despite use of new Al_2O_3 deposition system

Sample Yield Map for 256 × 256 Full-Frame CCD
All greens needed in a column to ensure that device functions



- **Analysis of pilot wafers began with shorts/opens testing**
  - **A single short among the 15 different tests results in device failure**
- **No significant yield improvement over previous device runs**
  - **Multiple shorts on all 256^2 devices tested (at left)**
  - **Average short spacing a few mm**
- **New investigation into yield launched**
  - **Discovered that new Al_2O_3 deposition tool, with much lower particle counts, lifted the veil on a previously hidden failure mechanism**

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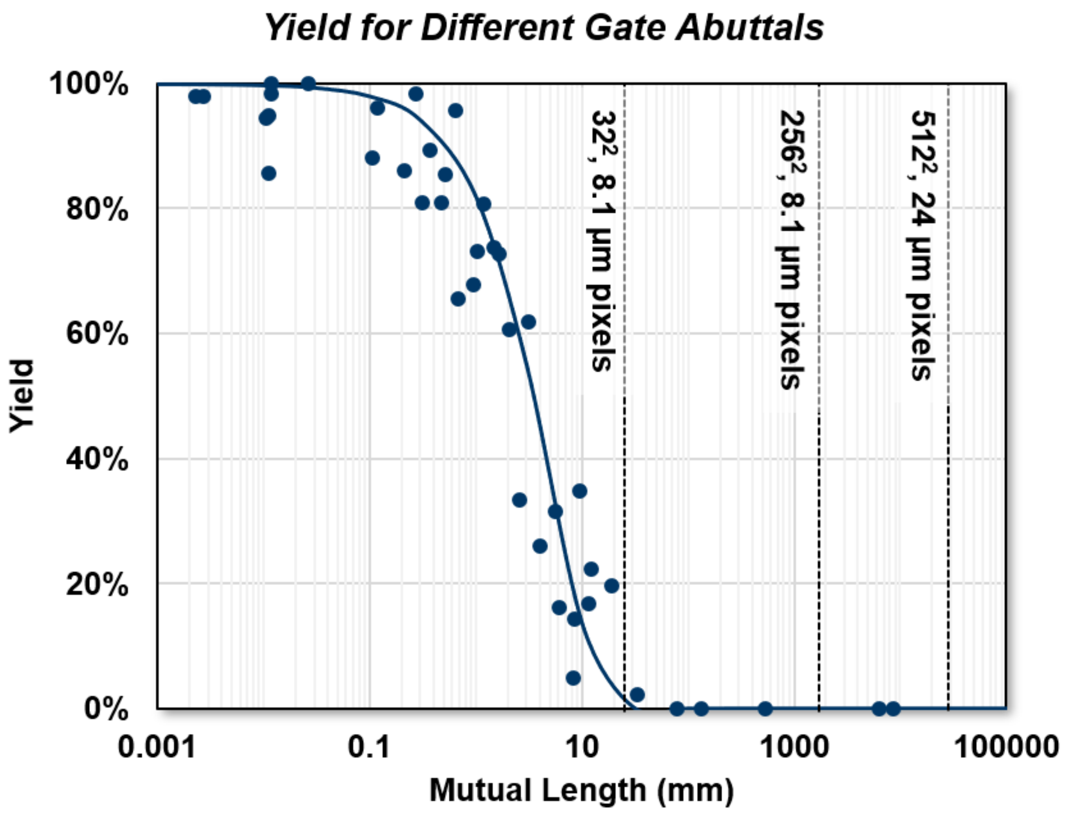

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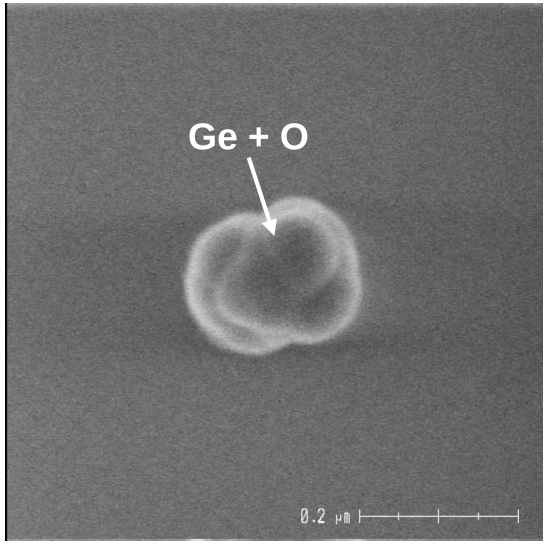
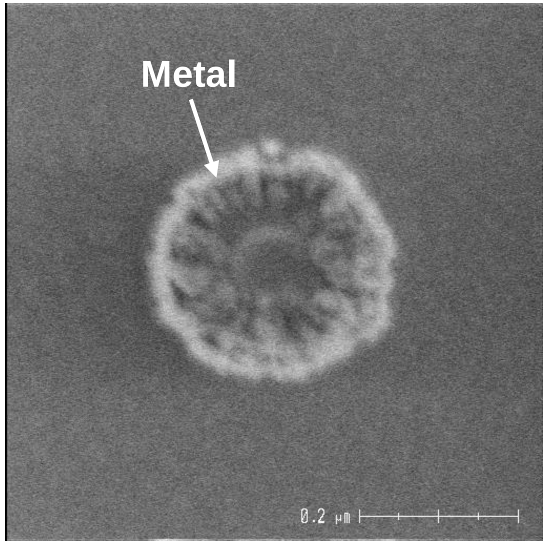
"Starry Night" Defects

Diagnosis

Post-Oxidation



Post-Metal Dep & Etch

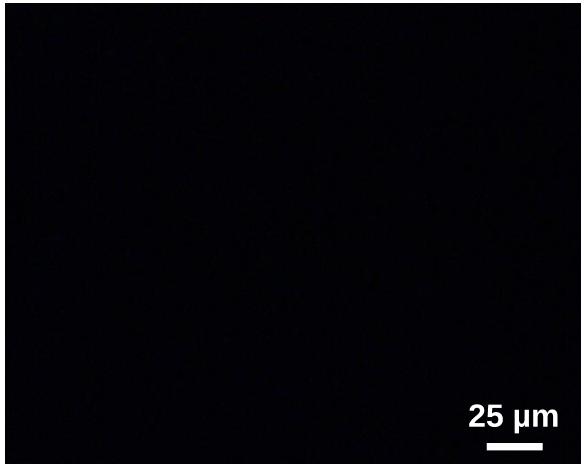


- **Root cause traced to nodules present on wafer surface after gate dielectric growth, composed only of Ge & O**
- **Nodules micro-mask metal gate etch, leaving ring of metal around the center nodule & leading to shorts**

Mitigation

Previous Process

New Process



- **New oxidation condition sharply reduces density of starry night defects**
- **Electrical tests on monitor wafers positively correlated starry night defect density to shorts-opens yield**

Shorts-Opens Test Summary on Second Batch of Wafers

Sample Yield Map for 256 × 256 Full-Frame CCD
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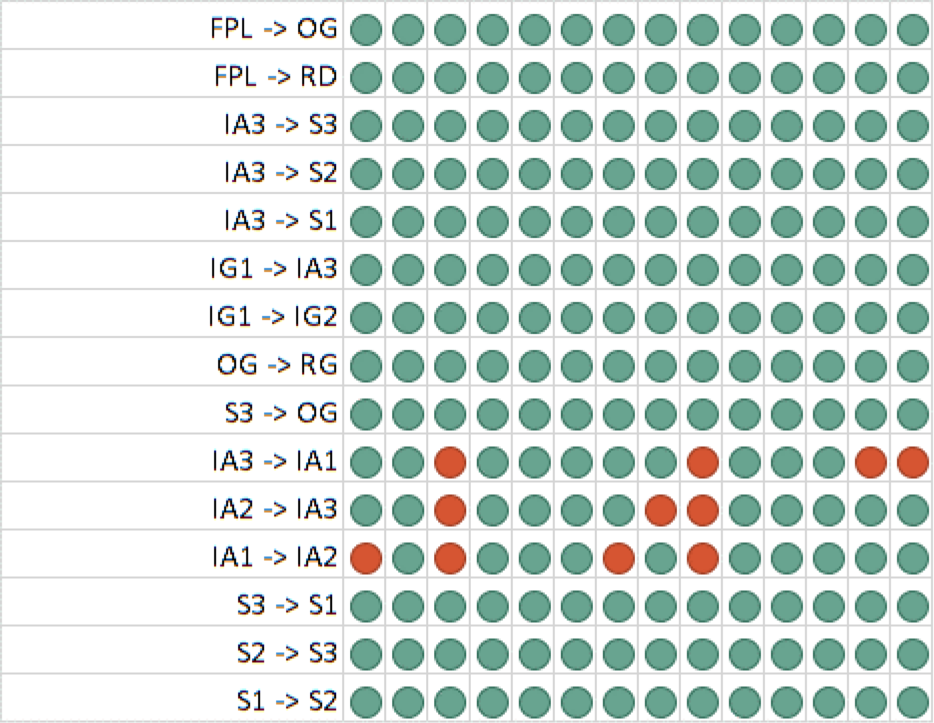

- **Average short spacing ~ 1 m**
  - **Approximately 200x improvement in average short spacing**
- **Enables us to routinely yield larger arrays**
  - **Example here: 7/14 256^2 arrays are clean**
- **Known issue at metal patterning on these wafers**
  - **Wafer flatness issue mentioned in previous slide**
  - **Yield would have been even higher if not for that**

Significant yield improvement in this second batch of wafers & no shortage of ideas for additional improvement!

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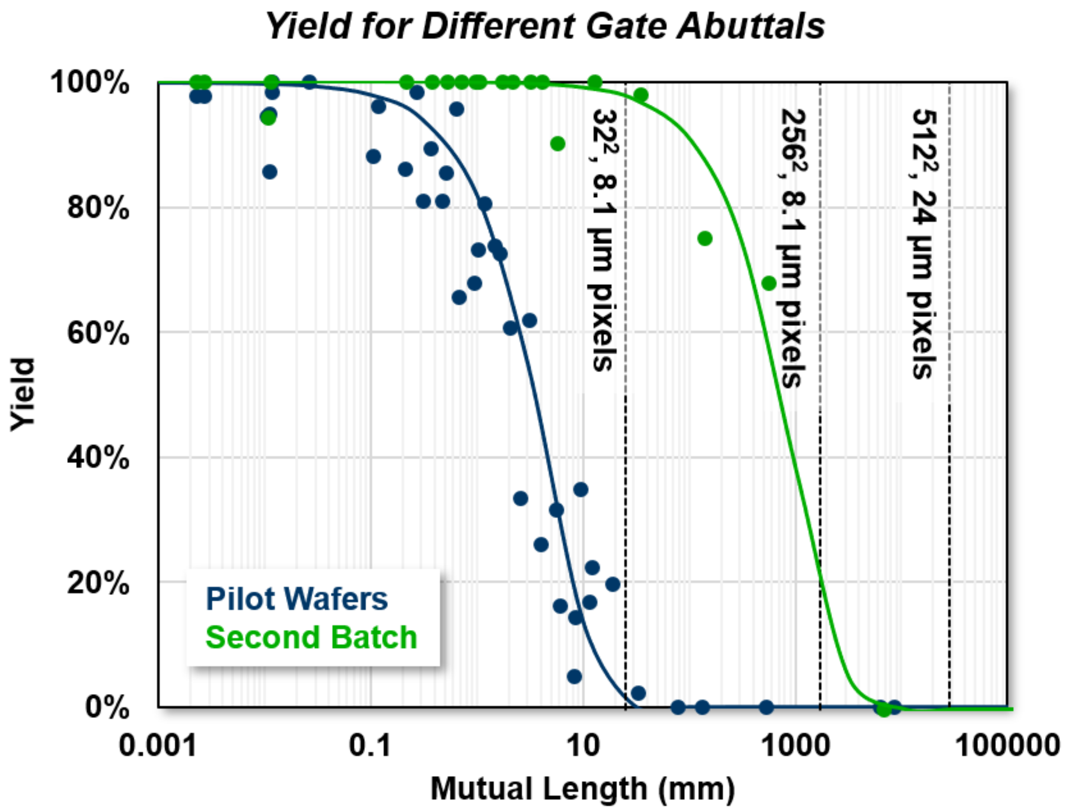

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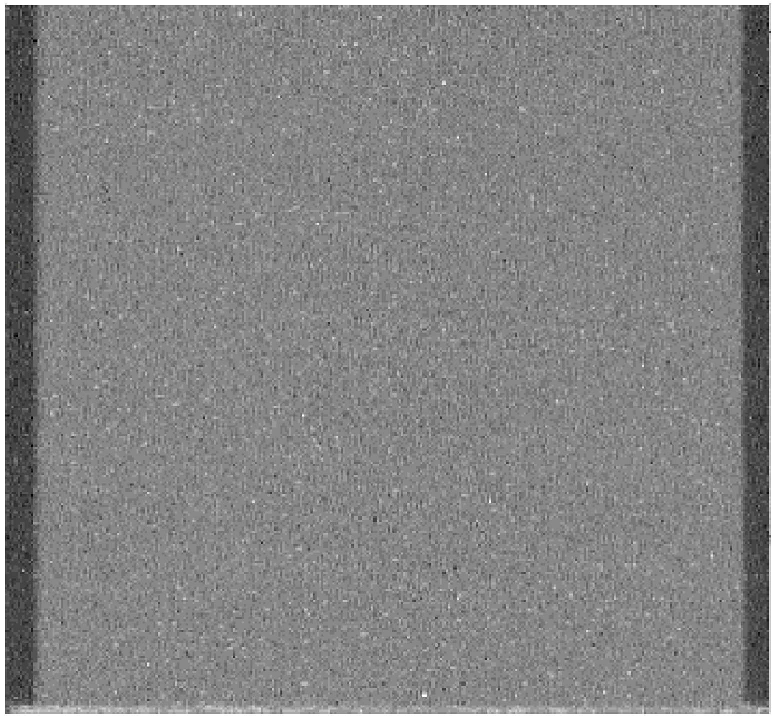
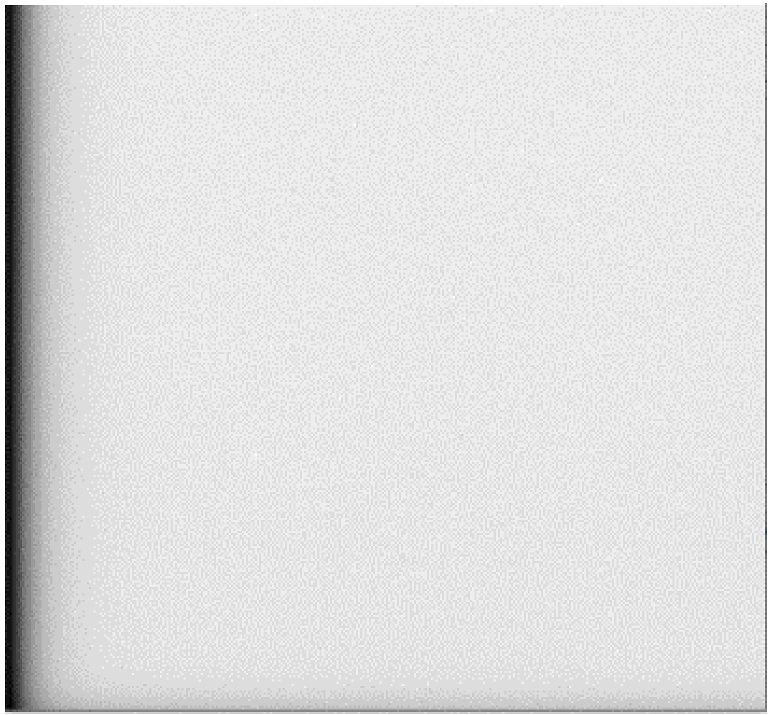
First (Preliminary) Test Results on Newest Devices

Dark



Flood-Illuminated



- **256 × 256-pixel array being clocked through MOSFET output at -60°C**

Encouraging early result; still a lot of work to do to optimize clocking biases

Conclusions and Future Work

- We have realized germanium CCDs that show promise for future scientific detectors
- Our current efforts are focused on improving performance and yield
  - New output amplifier designs to lower read noise and dark current
  - Improved processes to reduce density of gate-to-gate shorts which limit device format
- Future work:
  - Perform device screening on newly completed wafers
  - Transition device testing to cryogenic environment
    - Collaboration with MIT Kavli Institute for Astrophysics & Space Research
  - Begin back-illuminated detector development (pending NASA award)
  - Incorporate lessons learned on newly completed wafers to partially-processed wafers
    - Seven wafers staged ~6 weeks from completion