Pixel-detector developments for future Lepton Colliders

Tenth International Workshop on Pixel Detectors for Particles and Imaging – Pixel2022

December 12-16, 2022

Santa Fe, New Mexico

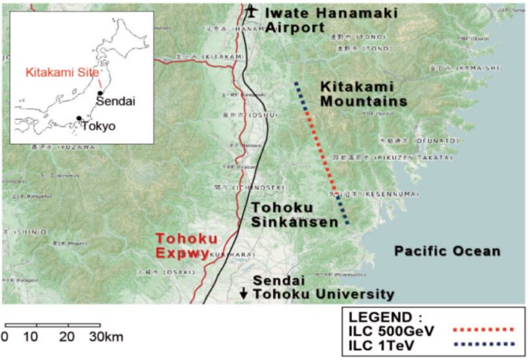
Dominik Dannheim (CERN)

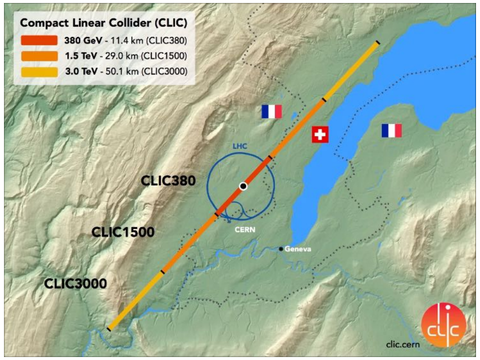
on behalf of the CLICdp collaboration

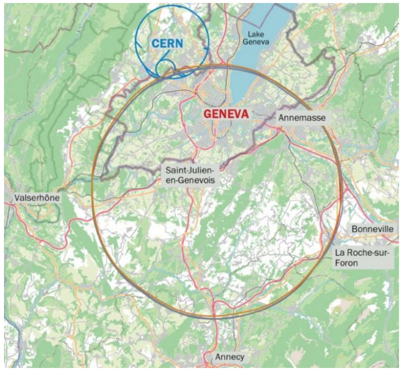
Outline

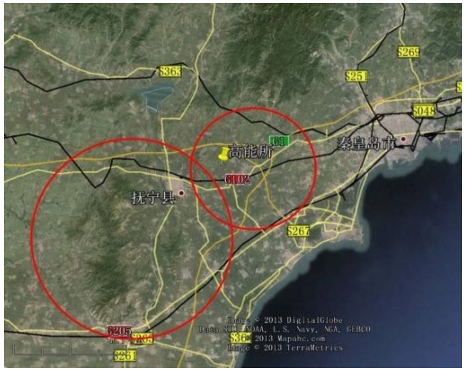
- Requirements for tracking and vertexing at future e^+e^- colliders
- Vertex and tracker concepts
- Pixel-detector technology R&D examples
- Conclusions

Disclaimers:
- Not a complete overview; showing only few examples of many ongoing developments
- For this talk: Lepton Collider = e+e- collider = Higgs Factory (Muon Collider not covered)



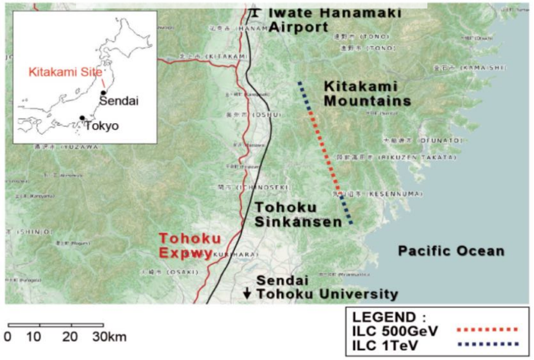




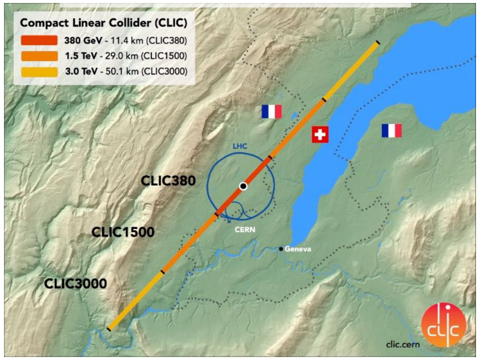


Higgs Factory vertex/tracker physics requirements

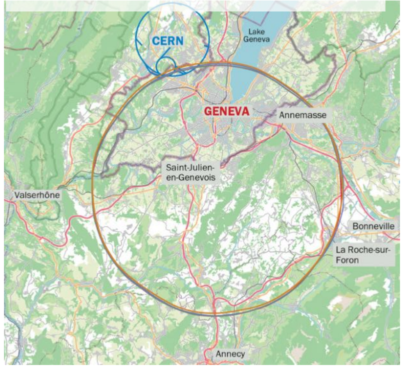
ILC in Japan
$\sqrt{s}_{max}$ =250-1000 GeV



CLIC @ CERN
$\sqrt{s}_{max}$ =380-3000 GeV



FCC-ee @ CERN
$\sqrt{s}_{max}$ =240-365 GeV



CEPC in China
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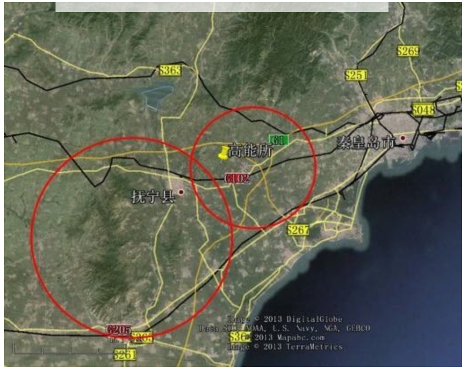
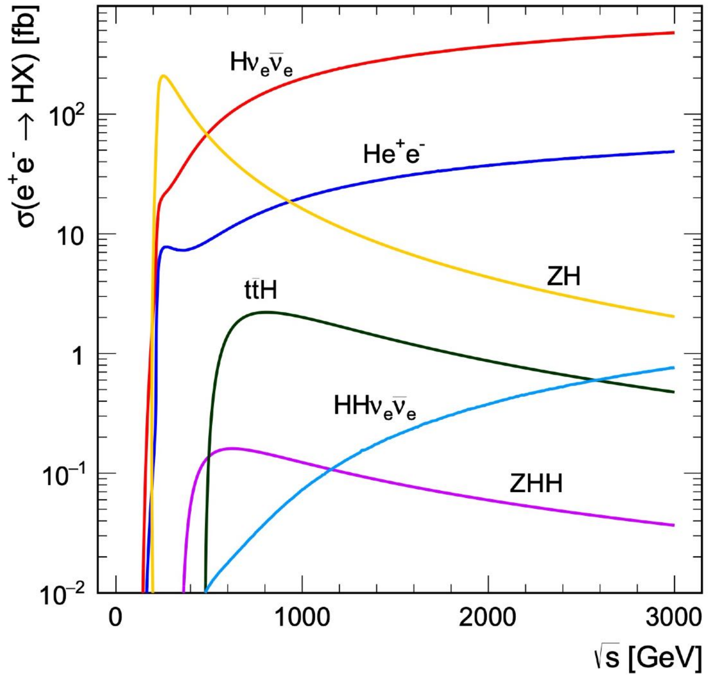


Physics goals for post-LHC (>2035) Lepton Colliders:

- Precision Higgs / EW / top measurements
- Direct/indirect BSM searches

Requires excellent vertex/tracking detector performance:

arXiv:1812.07986



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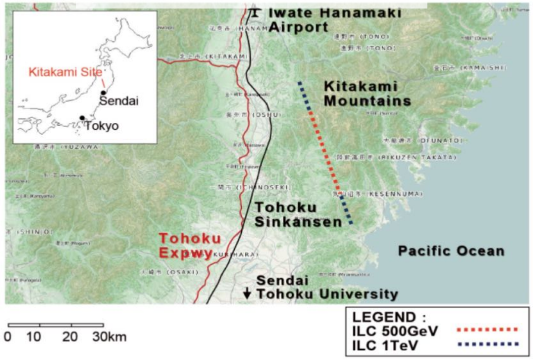

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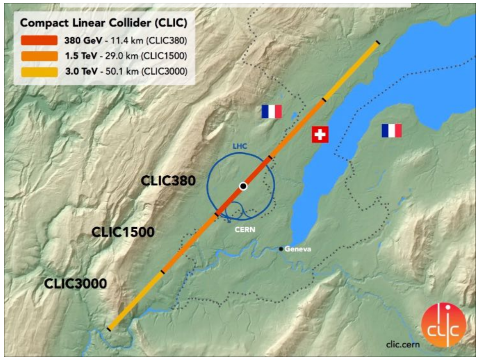

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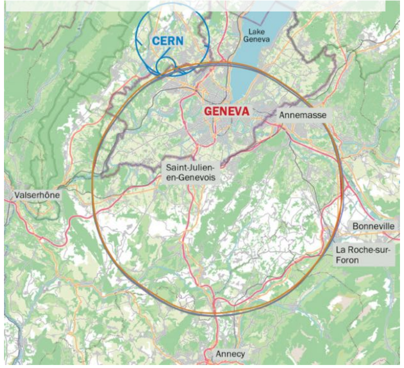

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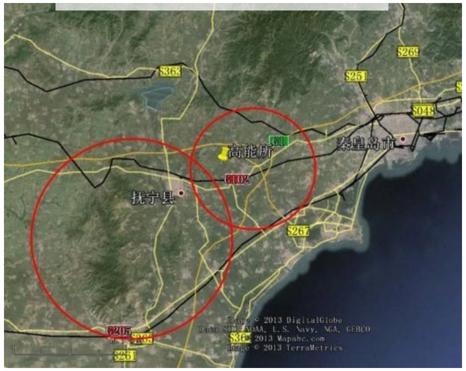

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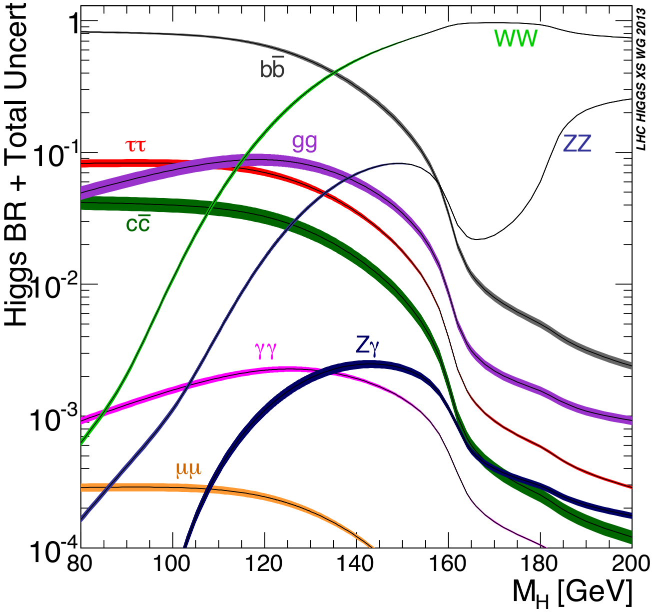
→ Vertex detector: $\sigma_{SP} \sim 3\ \mu\mathrm{m}$, $\lessapprox 0.2\%X0$ / layer (air cooling)



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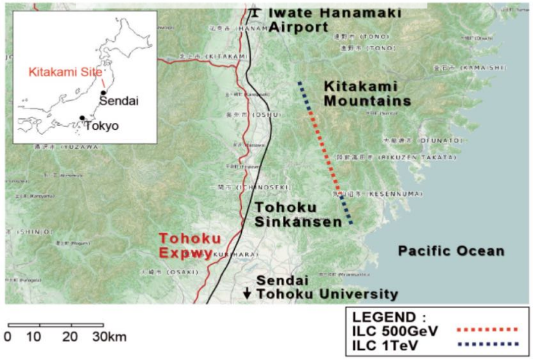

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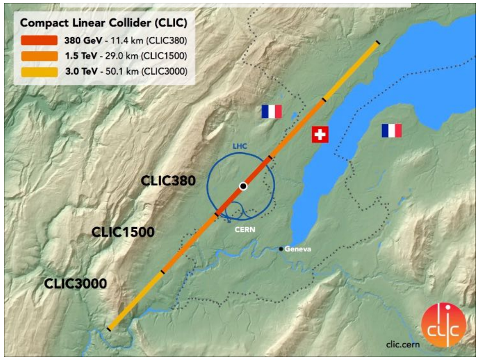

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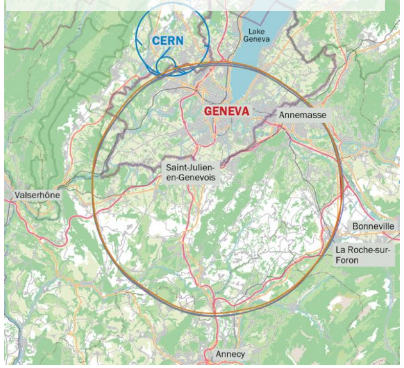

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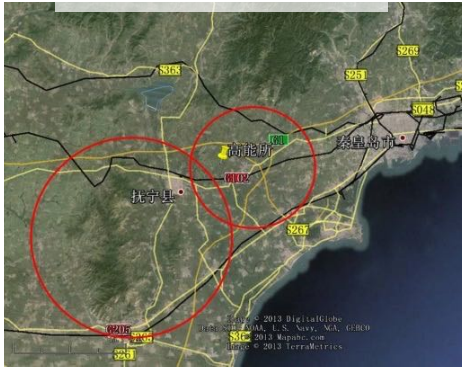

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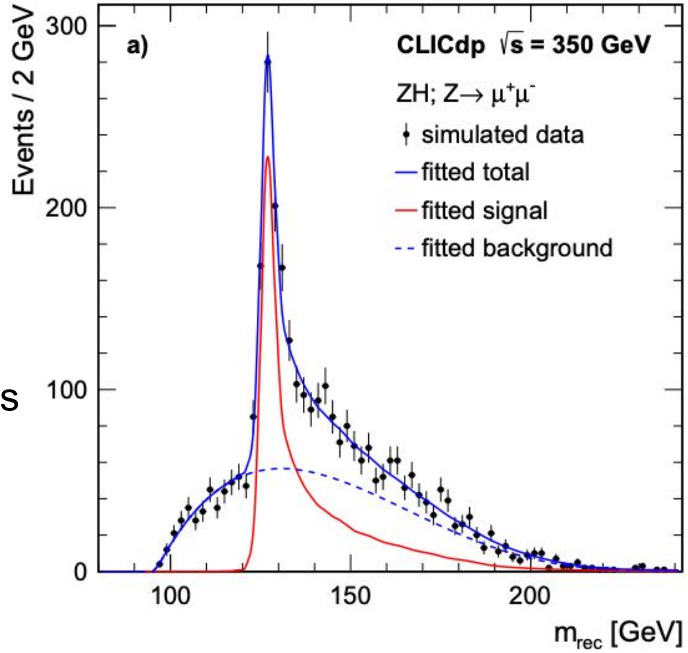
  (e.g. recoil-mass measurement in ZH)

→ Track-momentum: $\sigma(p_T) / p_T^2 \lesssim 2 \times 10^{-5}\ \mathrm{GeV}^{-1}$

→ Tracker: $\sigma_{SP} \sim 7\ \mu\mathrm{m}$, 1-2% X0 / layer, large radius, many layers



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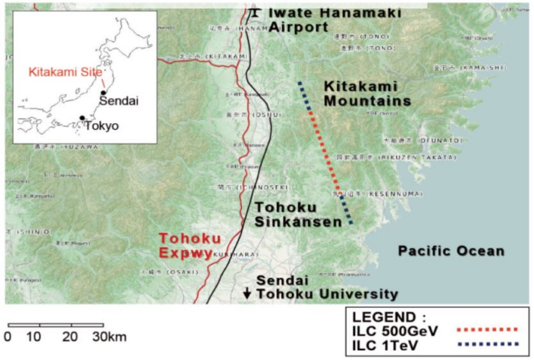

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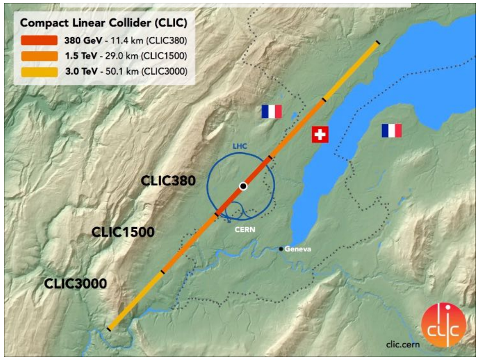

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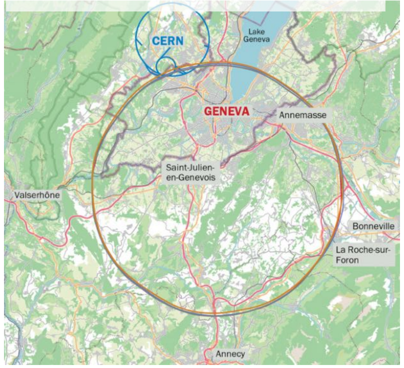

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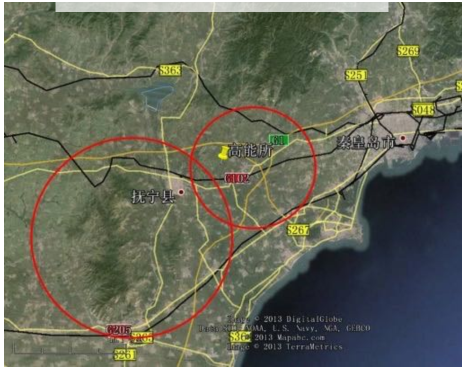

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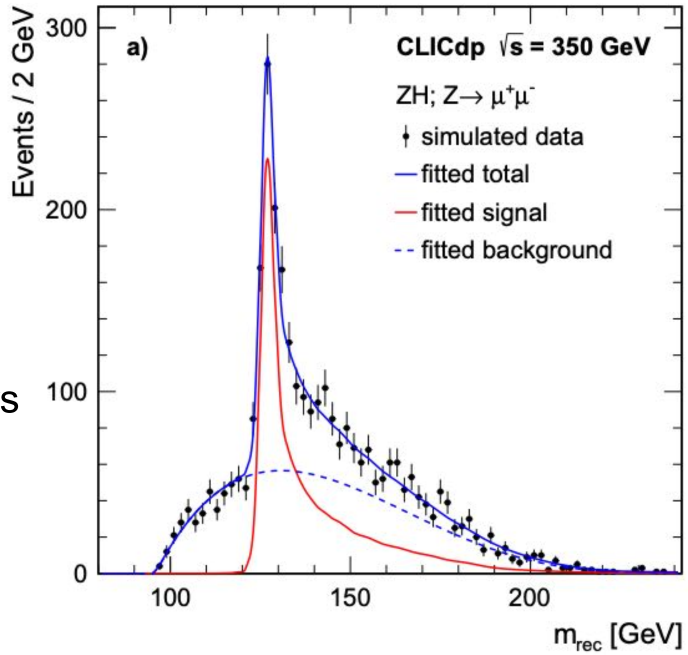
- Heavy-flavor physics → PID (K/pi separation) by dE/dx, dN/dx and/or 10's of picosecond timing layers
- Background rejection → low-angle coverage, timing
- Exotics (e.g. highly-ionizing or feebly-coupled particles)

→ dE/dx, many layers, large radius, precision timing



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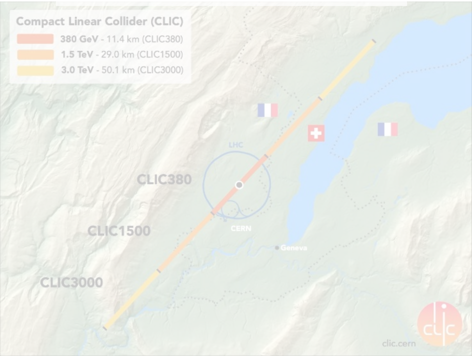

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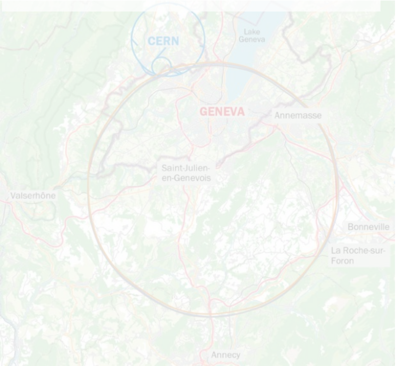

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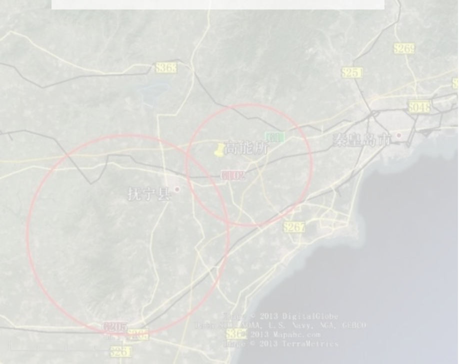

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R

- Similar physics requirements for trackers in all collider concepts
- More focus on asymptotic position resolution for high-energy stages of Linear-Colliders
- More focus on material budget and particle ID (dE/dx, dN/dx, ToF) for high-luminosity low-energy stages of Circular-Colliders

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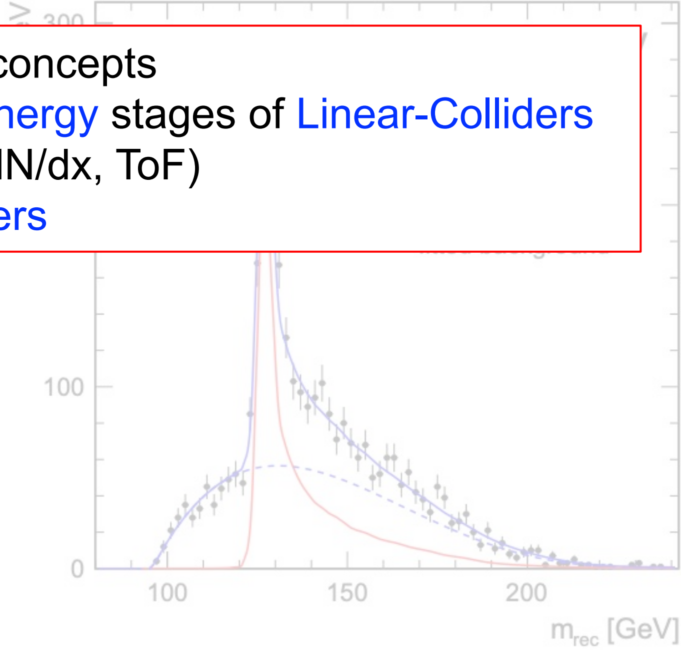


Experimental constraints on vertex/tracker

Main experimental constraints in **linear lepton colliders**:

- Significant rates of beam-induced backgrounds (incoherent e^+e^- pairs, $\gamma\gamma$→hadrons):
  - Constrains layout, granularity, impacts physics
- Backgrounds concentrated in very short bunch trains

→ High instantaneous hit rates (up to 6 GHz/cm² @ 3 TeV CLIC)

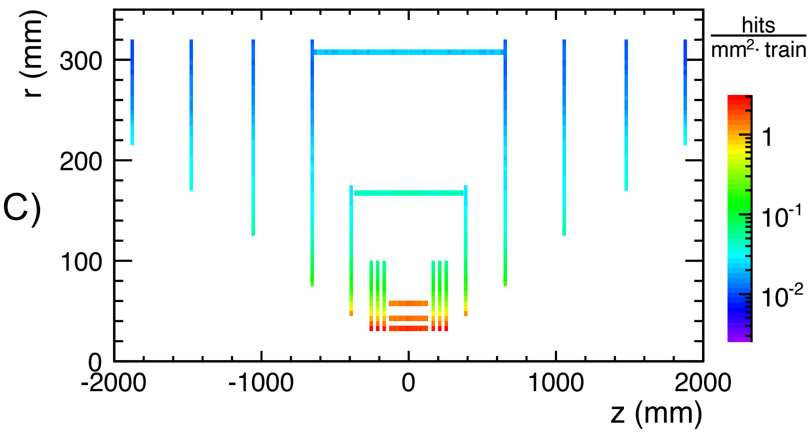
→ Time-stamping: few ns @ 3 TeV CLIC, ~1-10 µs @ ILC

→ Fast detector signals / frontend

- Low duty cycle: ~20-200 ms gaps between bunch trains

→ trigger-less readout, pulsed powering

CLIC backgrounds in tracking region



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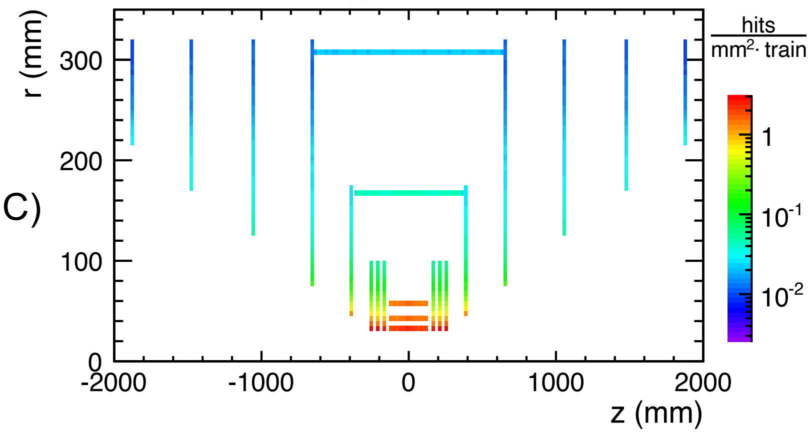

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- 30 mrad crossing angle of beams, focusing quadrupoles inside det. volume

→ B-field limited to ~2 Tesla

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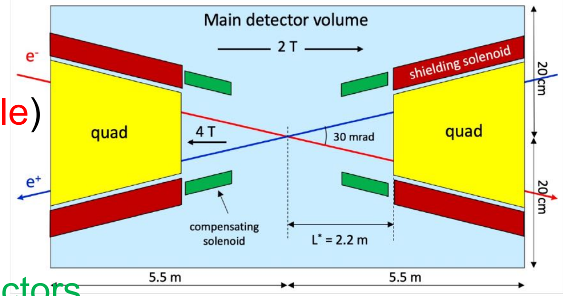
→ Fast detector frontend and DAQ

- Main backgr.: synchrotron radiation (reduced by shielding), incoh. pairs
- Continuous collisions (100% duty cycle)

→ Beam-induced backgrounds more spaced out, less severe impact on detectors, t.b.c. for FCC-ee, following recent reduction of beam-pipe radius from 15 to 10 mm

→ Pulsed powering not possible

FCC-ee detector region



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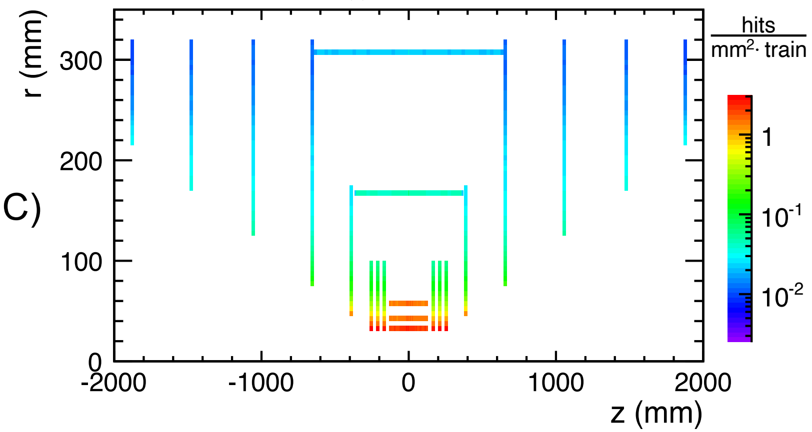

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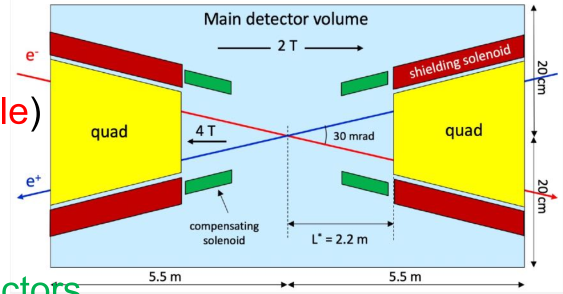
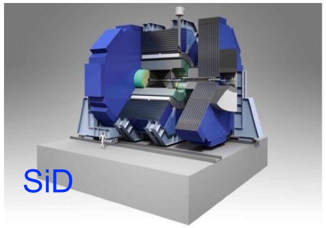


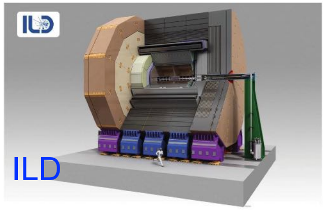
- Moderate radiation exposure (>~10^4 below LHC run 1!) for all lepton-collider proposals:
  - NIEL: $< 10^{11}$ n_{eq}/cm^2/y
  - TID: < 1 kGy / year

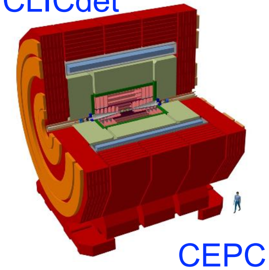
Vertex/tracking detector concepts

Collider	**ILC**		**CLIC**	**FCC-ee**			**CEPC**	
Detector Concept	SiD	ILD	CLICdet	CLD	FCC-ee IDEA	Noble LAr/LKr	CEPC baseline	CEPC IDEA
B-field [T]	5	4	4	2	2	2	3	2
Vertex inner radius [mm]	14	14	31	17 → 12	17 → 12	17 → 12	16	16
Tracker out. radius [m]	1.25	1.8	1.5	2.2	2.0	2.0	1.81	2.05
Vertex	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel
Tracker	Si-strips	TPC/ Si-strips	Si-pixel	Si-pixel	DC/ Si-strips	DC/Si-strips or Si-pixel	TPC/Si-strips or Si-strips	DC/ Si-strips

arXiv:1306.6329 *arXiv:1812.07337* *arXiv:1911.12230* *doi.org/10.1140/epjst/e2019-900045-4* *arXiv:1811.10545*


SiD


ILD

CLICdet


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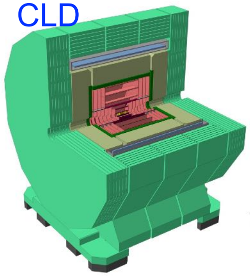
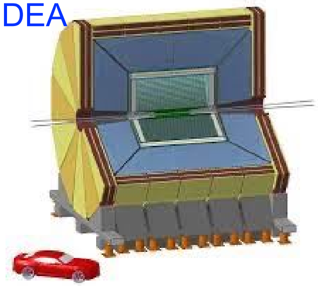
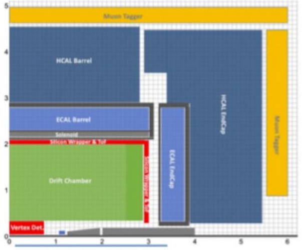
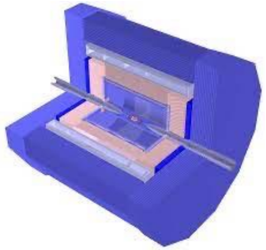
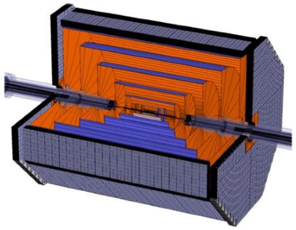


IDEA


Noble LAr/LCr


CEPC baseline


FST


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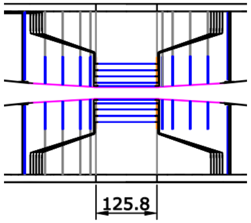
arXiv:1306.6329 *arXiv:1812.07337* *arXiv:1911.12230* *doi.org/10.1140/epjst/e2019-900045-4* *arXiv:1811.10545*

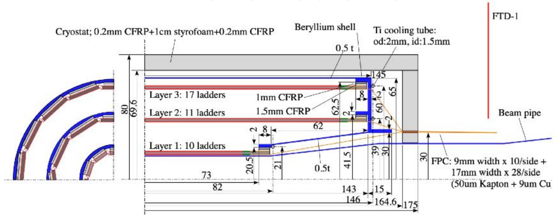
All concepts contain silicon-pixel vertex detectors:

- 5-6 barrel and up to 6 endcap layers (in doublets or singlets)
- high single point resolution per layer: σ_{SP}~3 μm → pixel sizes <~25 μm2
- low material budget: ≲ 0.2% X_0 / layer → thin sensors, low-power ASICs for air cooling (~50 mW/cm²)

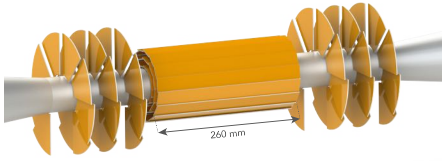
SiD vertex-detector



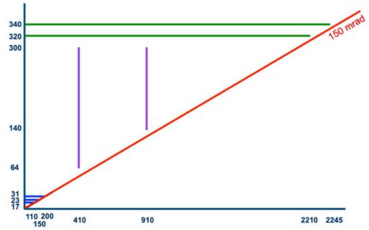
ILD vertex-detector



CLIC vertex-detector



IDEA vertex-detector



Vertex/tracking detector concepts

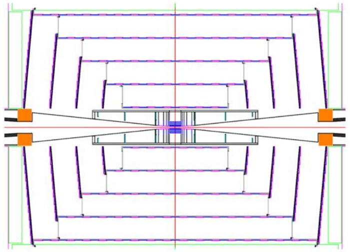
Collider	**ILC**		**CLIC**	**FCC-ee**			**CEPC**	
Detector Concept	SiD	ILD	CLICdet	CLD	FCC-ee IDEA	Noble LAr/LKr	CEPC baseline	CEPC IDEA
B-field [T]	5	4	4	2	2	2	3	2
Vertex inner radius [mm]	14	14	31	17 → 12	17 → 12	17 → 12	16	16
Tracker out. radius [m]	1.25	1.8	1.5	2.2	2.0	2.0	1.81	2.05
Vertex	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel
Tracker	Si-strips	TPC/ Si-strips	Si-pixel	Si-pixel	DC/ Si-strips	DC/Si-strips or Si-pixel	TPC/Si-strips or Si-strips	DC/ Si-strips

arXiv:1306.6329 *arXiv:1812.07337* *arXiv:1911.12230* *doi.org/10.1140/epjst/e2019-900045-4* *arXiv:1811.10545*

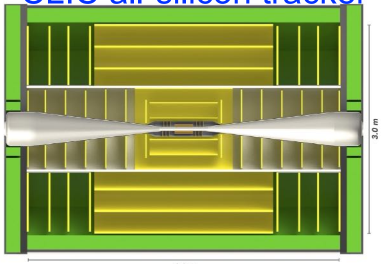
Silicon-based large-area trackers:

- many layers (barrel/endcap), large outer radius (scaling with B field)
- Large pixels or strip detectors
- ~7 μm single-point resolution in bending plane
  → ~25-50 μm Rφ pitch
- ~1-2% X0 per layer
  → low-mass supports + services,
  low power ~150 mW/cm²

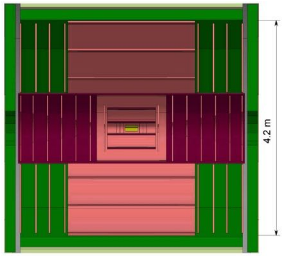
SiD all-silicon tracker



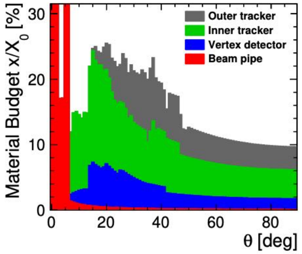
CLIC all-silicon tracker



CLD all-silicon tracker

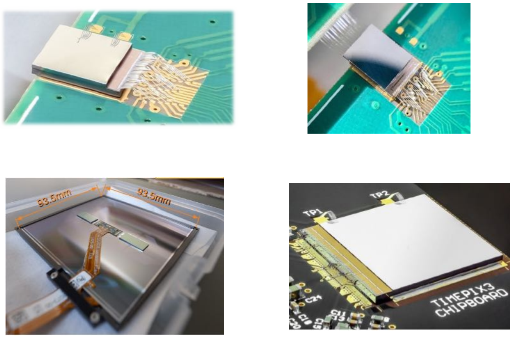


CLIC inner det. mat. budg.

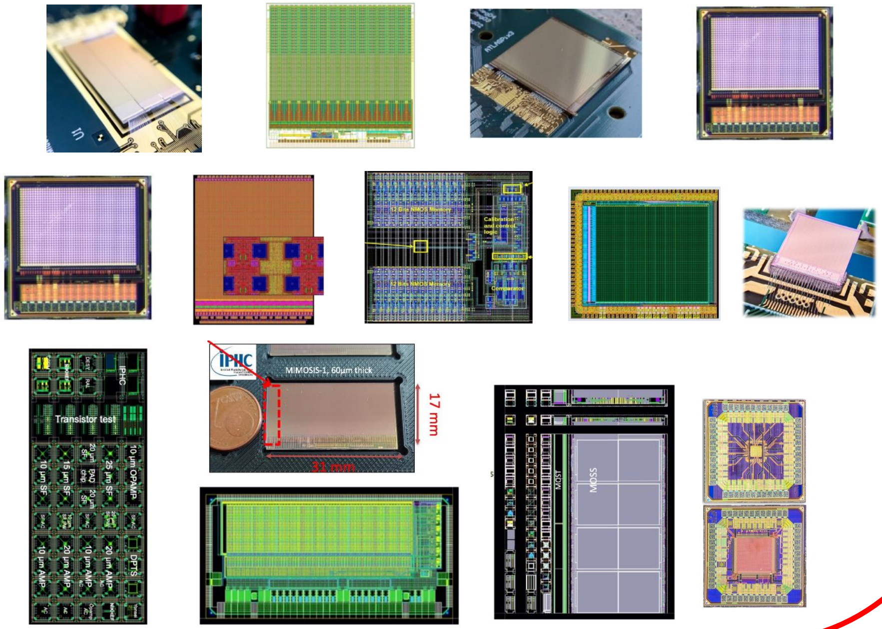


Silicon pixel-detector R&D examples

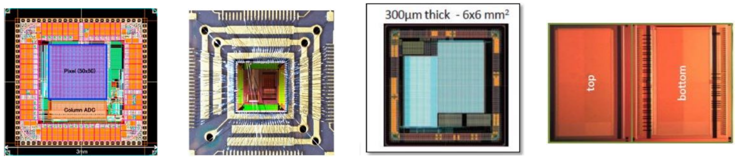
Hybrid detectors



Monolithic Sensors

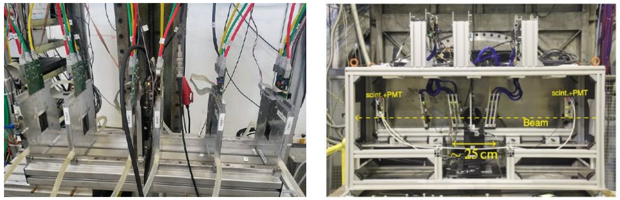


Silicon on Insulator

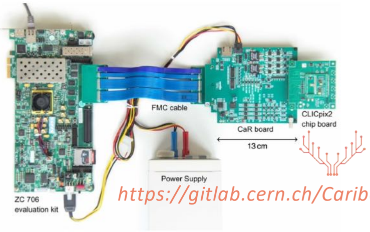


Tools

AIDA + CLICdp beam telescopes



Caribou readout system



https://gitlab.cern.ch/Caribou

MC Simulation framework: Allpix Squared

https://gitlab.cern.ch/allpix-squared/allpix-squared

NIM A 901 (2018) 164-172

Analysis & reconstruction framework: Corryvreckan

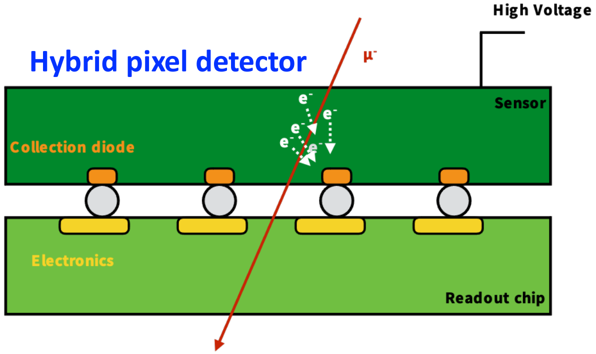
https://gitlab.cern.ch/corryvreckan/corryvreckan

2021 JINST 16 P03008

- Diverse R&D performed within various collaborative frameworks (ILD, SiD, CLICdp, IDEA, CERN EP R&D, AIDAinnova, …) and with strong links to other developments (HL-LHC, Belle II, Mu3e, CMB@FAIR, …)
- Mostly focusing on conceptual studies + technology demonstrators

→ Flexible tools developed, to support the R&D and exploit synergies between the various R&D lines

Hybrid pixel detectors



Hybrid pixel detectors

- Target applications: CLIC vertex detector, track-timing layers
- Separate interconnected sensor and readout ASIC layers

→ Factorise R&D on sensors and readout ASICs

- Develop new sensor concepts, e.g.:
  - Thin sensors (50 μm) with large fill factor (active edge)
  - Active / passive CMOS sensors
  - Sensors with enhanced lateral drift (ELAD) for optimal position resolution
  - Sensors with charge amplification (LGAD) for picosecond timing
- Profit from advanced industry technologies for highest ASIC performance (rate, timing)
- Profit from synergy with (HL)-LHC developments, medical imaging, gaseous detector r/o (GridPix)
- Refine and develop new interconnect technologies
- Challenges: material budget, interconnect: cost, minimum pitch

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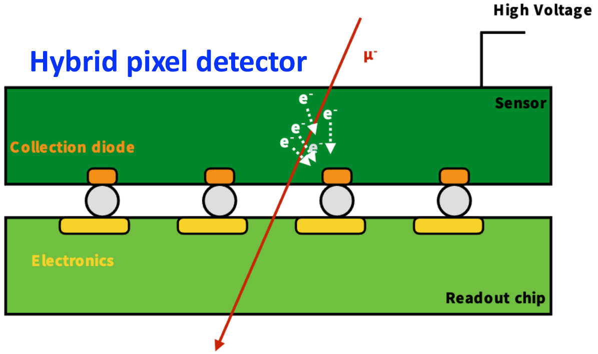
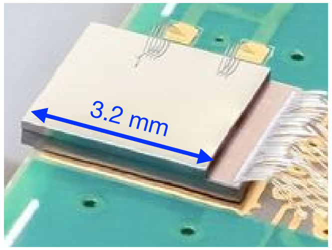
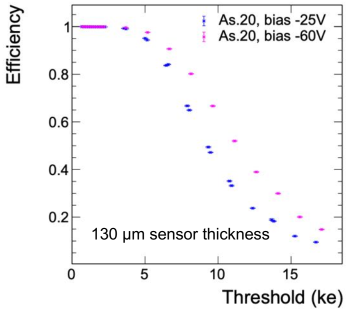


Test-beam studies for 65 nm CLICpix2 with thin active-edge sensors (25 µm pitch)

CLICpix2 hybrid assembly

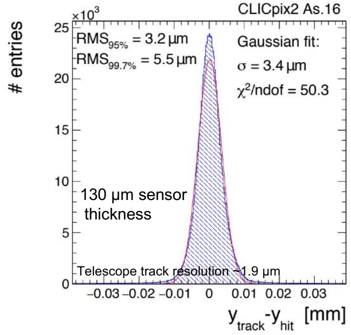


Efficiency

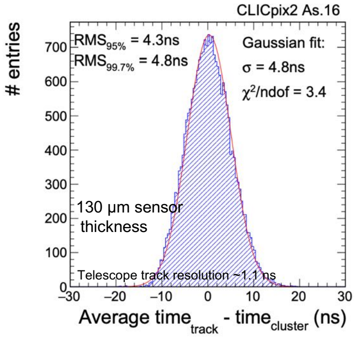


CERN-THESIS-2020-338

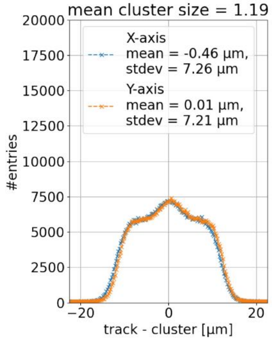
Spatial residuals



Timing residuals



Spatial residuals for 50 um thick sensor



arXiv:2210.02132

- Efficiency, spatial and timing resolution targets are achieved, but not yet simultaneously with material budget target
→ need advanced sensors / smaller pitch (28 nm ASICs, also considered for HL-LHC)

Fine-pitch hybridization

- Sensor/ASIC interconnect is one of the main challenges for hybrid pixel-detectors:
    - Cost / complexity, material budget, minimum pitch, single-die processing during R&D phase
- Different interconnect technologies are under study for future collider detectors

Fine-pitch hybridization

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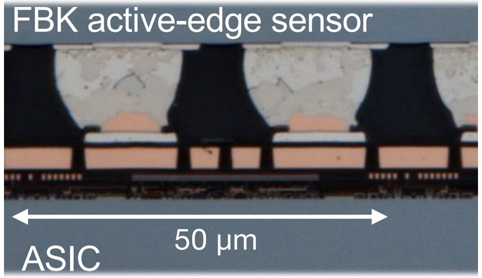
Single-die bump-bonding process developed by IZM:

- pitch 25 µm, sensor thickness down to 50 µm
- Support-wafer processing of CLICpix2 ASICs from MPW for UBM and SnAg bump deposition
- Excellent interconnect yield >99.7% observed in laboratory and test-beam measurements

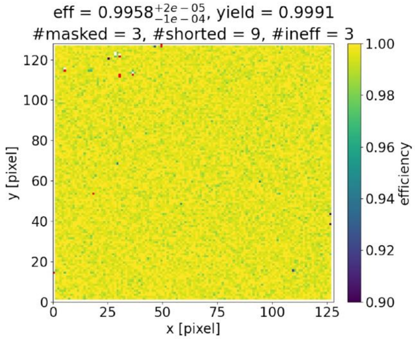
See also bonding + packaging talk by Thomas Fritzsch tomorrow

25 µm bump bonding @ IZM



https://arxiv.org/abs/2210.02132

TB pixel effic. 50 µm CLICpix2 ass.



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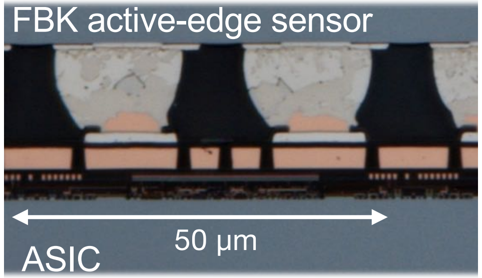
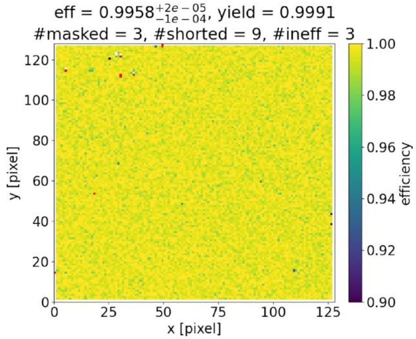


TB pixel effic. 50 µm CLICpix2 ass.

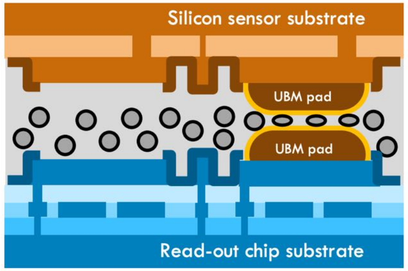


https://arxiv.org/abs/2210.02132

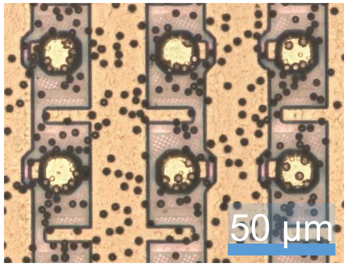
Hybridisation with **Anisotropic Conductive Films (ACF):**

- Adhesive epoxy film with embedded conductive micro-particles, electrical connection through thermo-mechanical compression
- Ongoing development / optimization of two single-die in-house processes:
    - Chemical Electroless Nickel Immersion Gold (ENIG) deposition for Under Bump Metallization (UBM)
      → uniformity, thickness, edge effects
    - Semi-automatic flip-chip bonding with ACF layer
      → ACF material (particle diameter and density), epoxy thickness, bonding profile
- Proof-of-principle results for Timepix3 hybrid assemblies
  → high interconnect yield in regions with good UBM
  → ongoing optimization of UBM process for single dies
- ACF also under study for module integration
  → 'easier' use case (large-pitch interconnect)

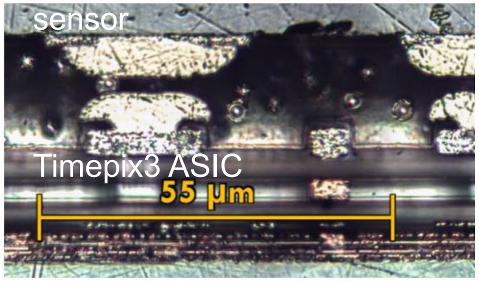
ACF bonding w/ conductive micro-particles



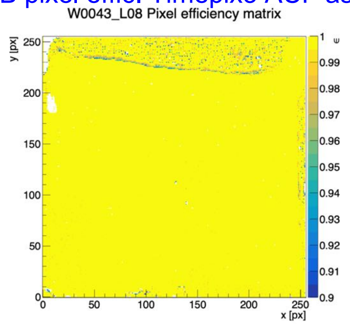
ACF on Timepix3



55 um ACF interconnect



TB pixel effic. Timepix3 ACF ass.



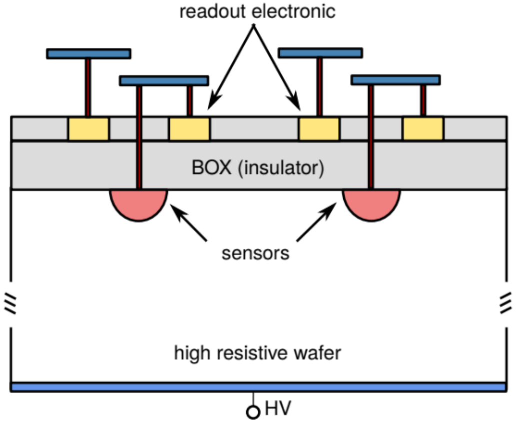
https://arxiv.org/abs/2210.13046

Silicon-on-Insulator (SOI) / 3D integration

- Silicon-On-Insulator (SOI): r/o electronics on thin low-resistivity electronics wafer, separated from high-resistivity sensor wafer by buried insulation oxide layer

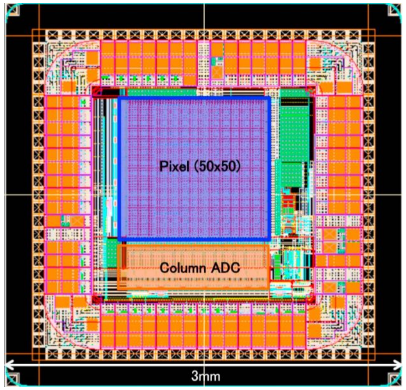
- Thin + fast (fully depleted) ”monolithic” sensors
- Challenge: specialized + complex production process (wafer bonding)
- Various developments targeting LC vertex and tracking detectors, e.g.:
  - SOFIST V1 in 200 nm LAPIS SOI
    20x20 μm^2 pitch, 200 µm thickness → σ_{SP}~1.4 µm
  - Cracow SOI test chip in 200 nm LAPIS SOI process
    30x30 μm^2 pitch, 500 µm thickness → σ_{SP}~1.5 µm
  - IPHC LAPIS SOI test chip (with KEK)
  - 3D developments @ IPHC (with TJ, T-Micro)
- Precision timing not yet demonstrated

SOI pixel detector



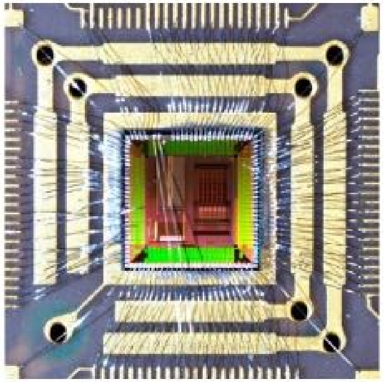
See also the talks in the SOI session of this morning

SOFIST v1



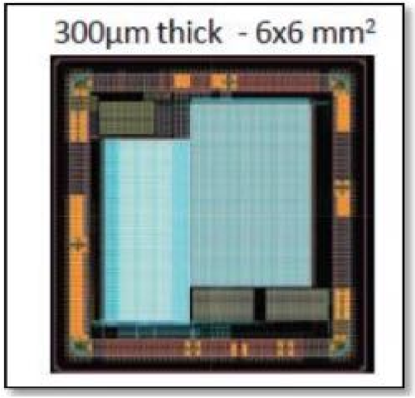
https://doi.org/10.1016/j.nima.2018.06.075

Cracow SOI test chip



Nucl. Instrum. Methods Phys. Res., A 988 (2021) 164897

IPHC/KEK SOI test chip



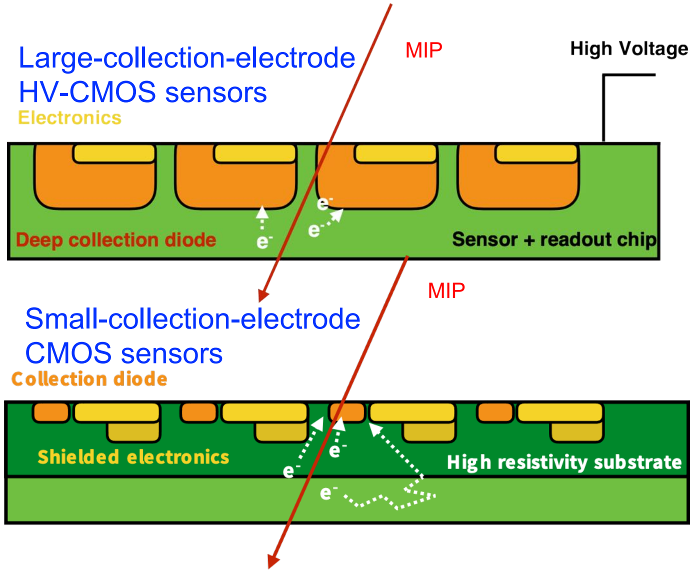
IPHC double-tier 3D TJ 180

https://indico.cern.ch/event/995633/contributions/4259377/attachments/2208714/3738410/LCWS2021_BESSON_vf.pdf

Monolithic CMOS sensors

Monolithic CMOS sensors using (adapted) industry technologies:

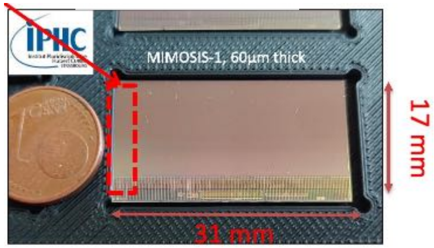
- Sensor and readout electronics fully integrated
- Different concepts:
  - Large-collection electrode High-Voltage (HV-CMOS) for large + fast signals, radiation hardness
  - Small-collection-electrode designs for low capacitance, high signal/noise, low power
- Simplified construction (no bonding)
- Challenges: complex non-uniform sensor structures (simulation), interplay sensor/readout, process modifications are foundry dependent / parameters not publicly available
- Many ongoing developments, exploiting progress in semiconductor industry and synergies (HL-LHC, Mu3e, Belle II, CMB@FAIR, …)
- Trend towards smaller feature sizes (180 nm → 65 nm) for improved performance
- Target: vertex/tracker of all Higgs-Factory detectors


Large-collection-electrode HV-CMOS sensors

Small-collection-electrode CMOS sensors

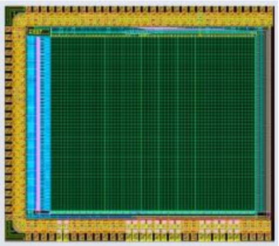
See also the talk by Jerome Baudot and other talks in the CMOS session

MIMOSIS-1
180 nm CMOS

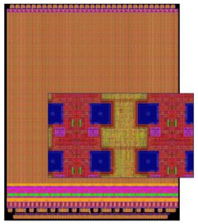


CLICTD
180 nm CMOS

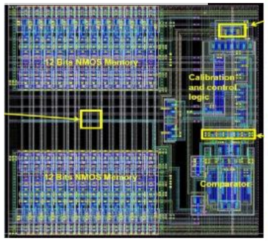
JadePix2
180 nm HV-CMOS



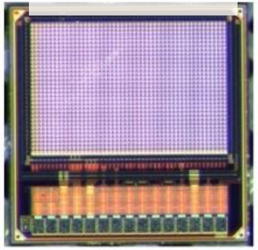
ARCADIA MD1
110 nm CMOS



Chronopix
90 nm CMOS

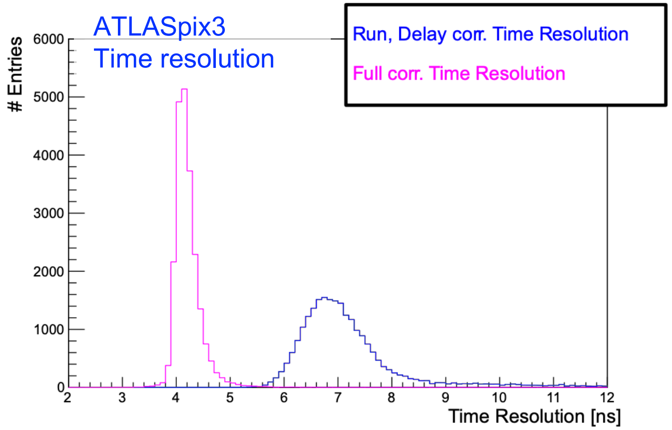


CE-65
65 nm CMOS

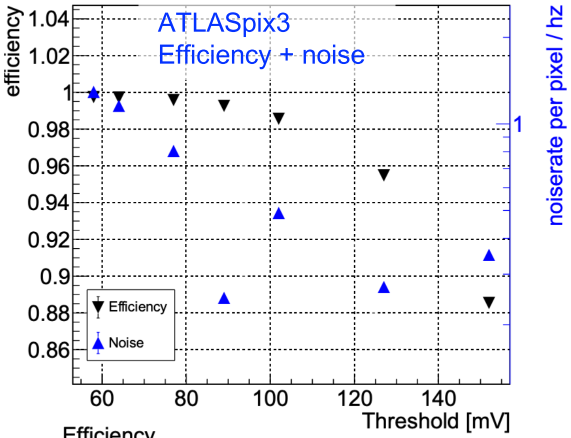


180 nm High-Voltage CMOS

- Active depleted HV-CMOS sensors with fully integrated readout
- Under study for CLIC tracker + IDEA outer vertex / tracker
- Same technology initially considered for ATLAS outer tracker and chosen for Mu3e tracker (MuPix8), under study also for LHCb Mighty Tracker
- Depleted thin sensors (high-resistivity substrates, >100 V bias), fast frontend → large signal (dE/dx), fast, radiation hard
- Very good performance observed in test beam:
  - >99.7% efficiency (ATLASpix3)
  - Timing precision ~4 ns (ATLASpix3)
  - Spatial resolution <10 µm (Telepix, 25 µm pitch in R/phi)
  - Power consumption down to 140 mW/cm² (ATLASpix3)
- Plans for dedicated CEPC design in 55 nm HV-CMOS process
- Other HV-CMOS developments for CEPC: JadePix, TaichuPix



Time resolution (RMS) for every pixel
Uncorrected 6.7ns +- 0.5ns
ToT corrected 4.1ns +- 0.1



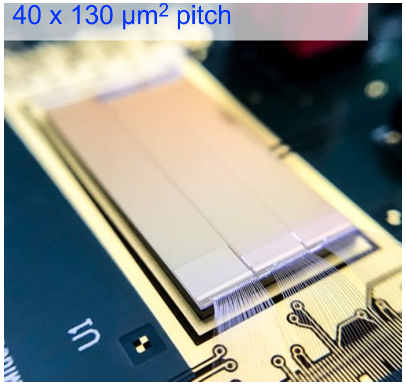
Efficiency

I. Peric et al.

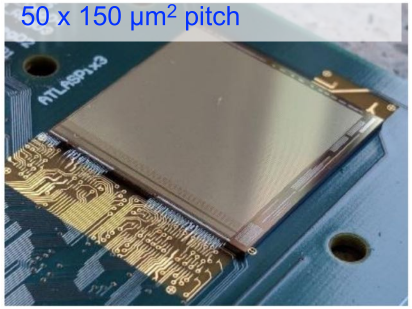
https://agenda.linearcollider.org/event/9211/contributions/49477/attachments/37547/58841/ILC_HVCMOS_Oct21.pdf

See also the talks by Klaas Padeken and Riccardo Zanzottera in this session

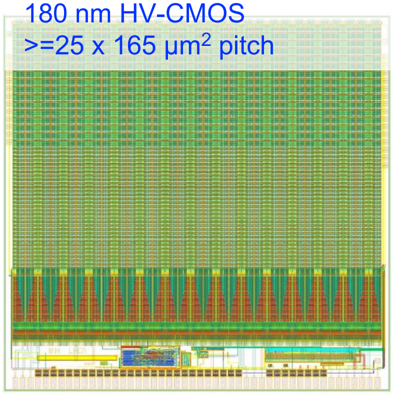
ATLASpix
180 nm HV-CMOS sensor
40 x 130 µm² pitch



ATLASpix3
180 nm HV-CMOS
50 x 150 µm² pitch



LHCb/CLIC/Telepix
180 nm HV-CMOS
>=25 x 165 µm² pitch

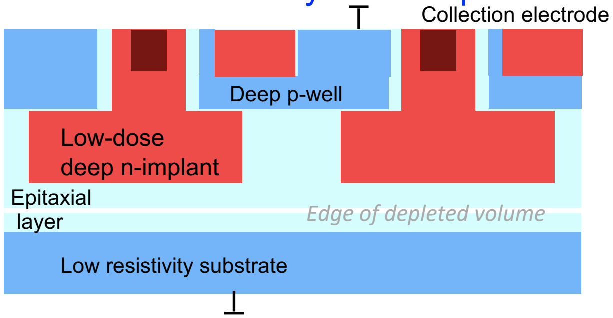


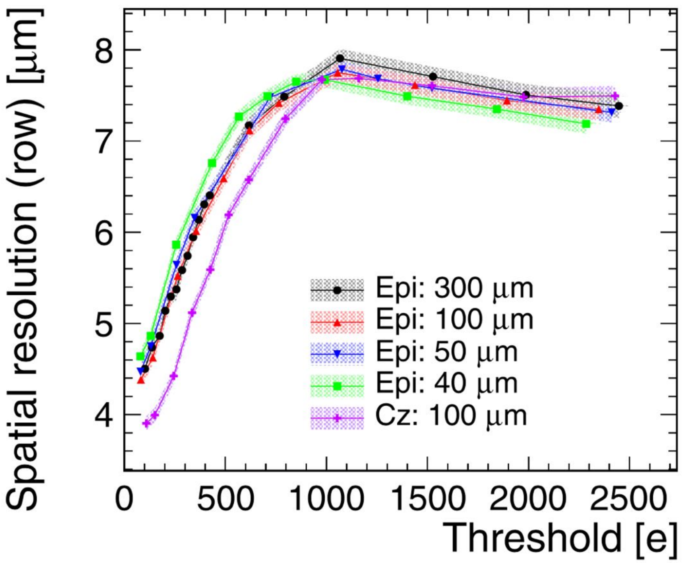
180 nm monolithic CMOS example: CLICTD

CLICTD 180 nm monolithic sensor

- Modified 180 nm CMOS imaging process with small-collection electrode
- Target: CLIC tracker
- Innovative sub-pixel segmentation, Channel pitch: (8 x 37.5) µm x 30 µm
- Simultaneous time and energy measurement per channel
- Exploring large parameter space of sensor-design modifications, substrate materials (epitaxial, high-resistivity Cz) and thicknesses (40-300 µm), in collaboration with ATLAS MALTA / STREAM
- Detailed TCAD/Geant4-based simulation studies (AllPix²) to optimize sensor design

CLICTD sensor layout example




Segmented n-implant

See AllPix2 talk by S. Spannagel

IEEE TNS 67.10 (2020): 2263-2272
NIM A 1006 (2021) 0165396
NIM A 1041 (2022) 167413

	Required (CLIC tracker)	Epi	Cz*
Spatial resolution (transv.)	< 7 µm	4.6 µm	4.3 µm
Time resolution*	~ 5 ns	5.2 ns*	4.4 ns*
Efficiency	> 99.7 %	> 99.7 %	> 99.7 %
Material content	< 200 µm	40 - 100 µm	100 µm

*limited by front-end

- Excellent performance observed in test-beam measurements and reproduced by simulations
- Results have served as input to sensor optimization, also for 65 nm process (see talk by W. Snoeys)

65 nm monolithic CMOS

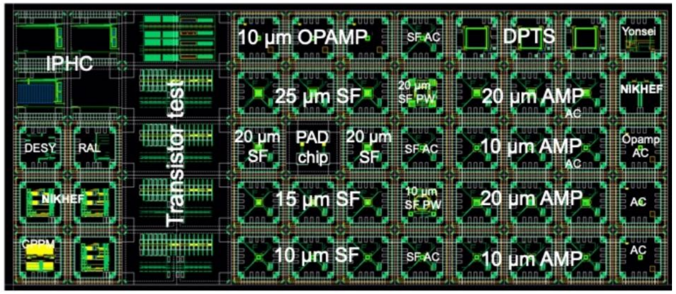
EP R&D

TPSCo 65 nm ISC CMOS imaging process currently being validated for HEP:

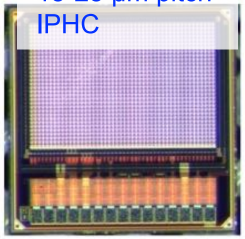
- Collaboration CERN EP R&D, ALICE ITS3 upgrade, many institutes and other projects
- Smaller feature size → smaller pixels (~10-35 µm), enhanced performance
- Candidate technology for Higgs-factory vertex/tracker developments
- Encouraging results from first MLR1 test-chip production in 2021:
  - Process modifications and sensor-design optimizations proven to work as expected
  - Full efficiency + nanosecond sensor timing achieved for optimized designs
- Next submission in stitched engineering run ER1 with new developments, e.g.: wafer-scale MOST/MOSS (ITS3), H2M test-chip (hybrid architecture in monolithic process)
- More focused developments for Higgs factories proposed for future submissions, e.g. test chips from UK LC Silicon Pixel Tracker (SPT) project, optimized for LC duty cycle

See also the ALICE talks in Tuesday's upgrade session

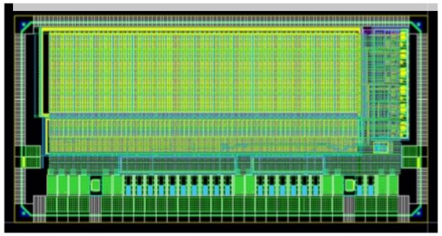
MLR1 reticle 2021



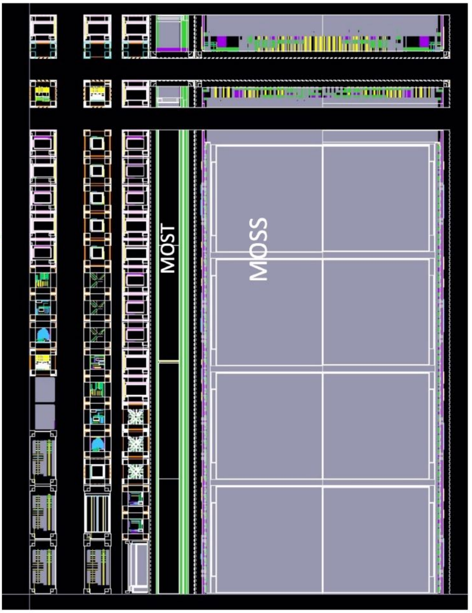
CE-65,
15-25 µm pitch
IPHC



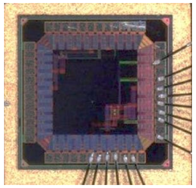
H2M (new in ER1), 35 µm pitch
DESY, CERN, IFAE



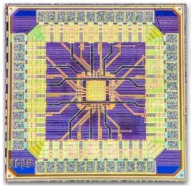
ER1 reticle (2022/23)



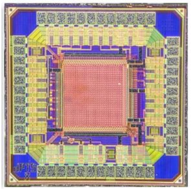
TANGERINE
CSA1 2x2,
16 µm pitch
DESY



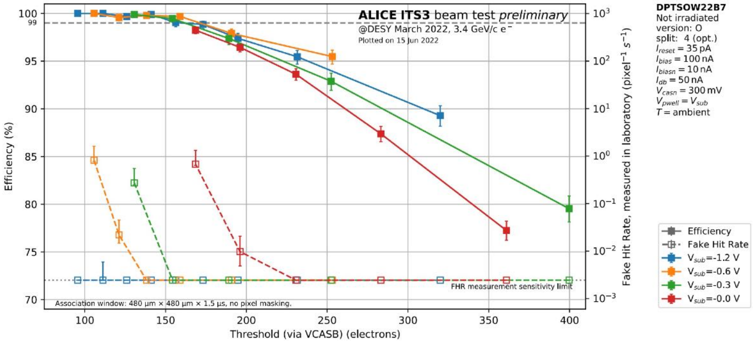
Analog pixel test
structure (APTS)
10-25 µm pitch
CERN



Digital pixel test
structure (DPTS)
15 µm pitch
CERN



DPTS efficiency + fake-hit rate in test beam



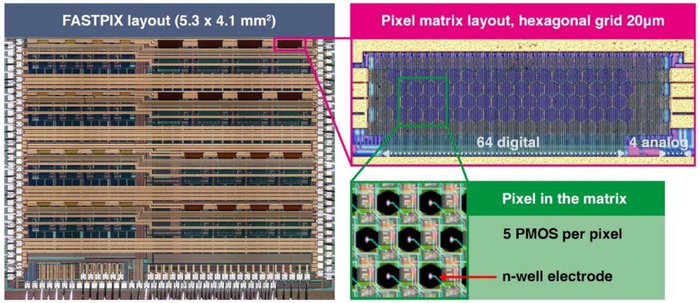
Silicon track-timing detectors

- Several developments targeting ~20-100 ps pixelated timing for MIPs
- Dedicated timing layer or integrated in tracker
- Use cases: 4D tracking, enhanced background rejection, particle ID by ToF (<30 ps / 2m for K/pi/p separation up to 3 GeV)

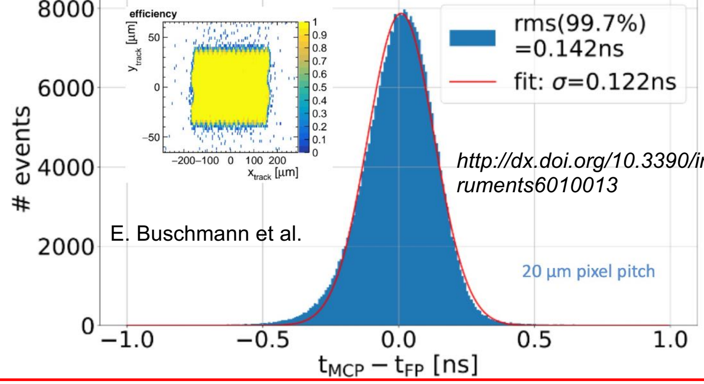
Many more R&D examples in talks from Monday's fast timing session

FASTPIX technology demonstrator for sub-ns timing

- Modified 180 nm CMOS imaging process, design optimisations for fast charge collection
- Small hexagonal pixels (8.66 to 20 µm pitch)
- Time resolution of ~140 ps achieved in test beam



FASTPIX efficiency and time resolution in test beam



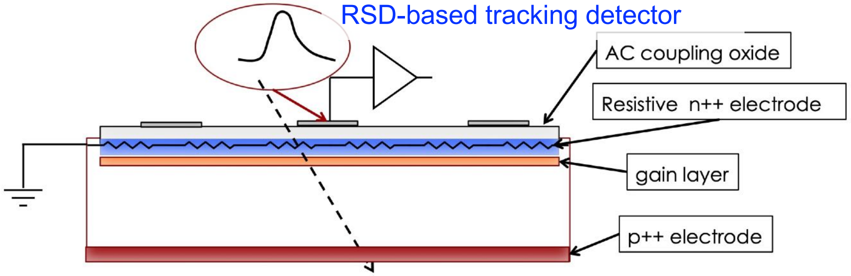
http://dx.doi.org/10.3390/instruments6010013

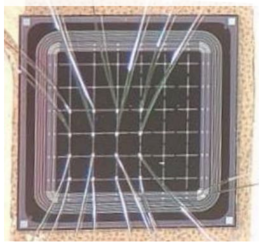
E. Buschmann et al.

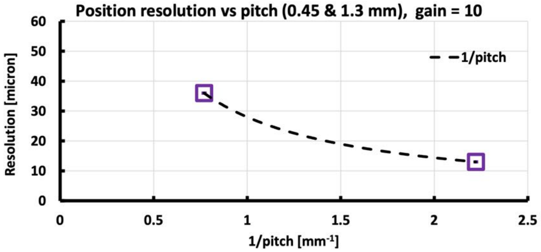
Resistive (AC-coupled) LGAD

N. Cartiglia et al.

- LGAD sensors with internal gain + hybrid r/o ASIC
- Resistive (AC-coupled) LGADs (RSD): enhanced position resolution @ large r/o pitch through amplitude interpolation
  → suitable as timing layer in low-occupance regions
- Time resolution of ~25-30 ps achieved
- Position resolution of 15 µm for 450 µm r/o pitch


RSD-based tracking detector

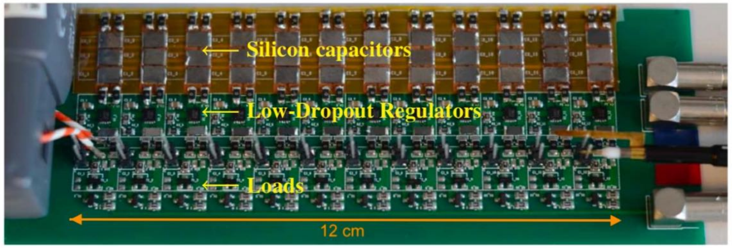

RSD prototype, 450 µm pitch



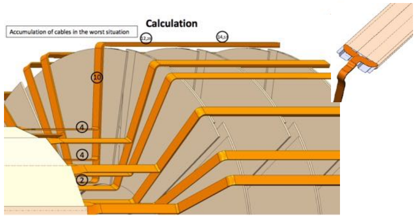
http://dx.doi.org/10.1016/j.nima.2022.167228

Silicon detector integration

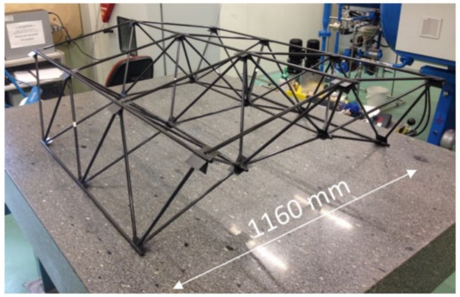
Power-pulsing mockup



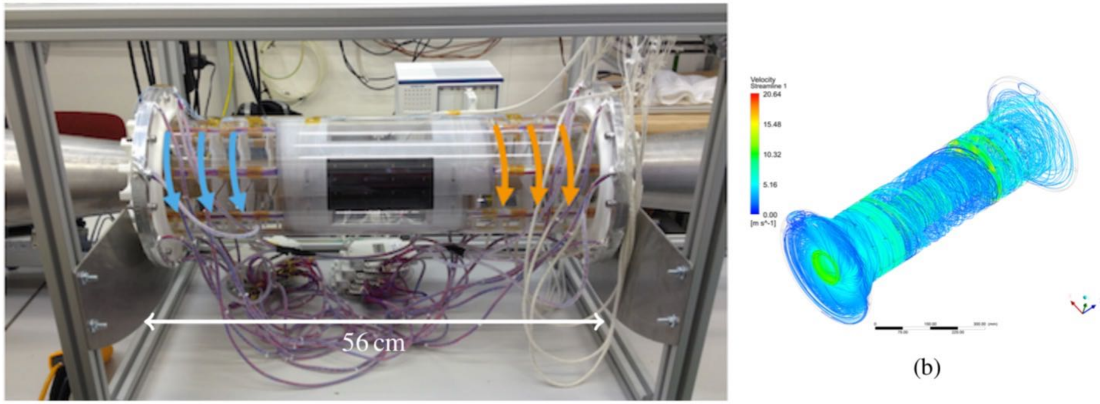
Vertex-detector services



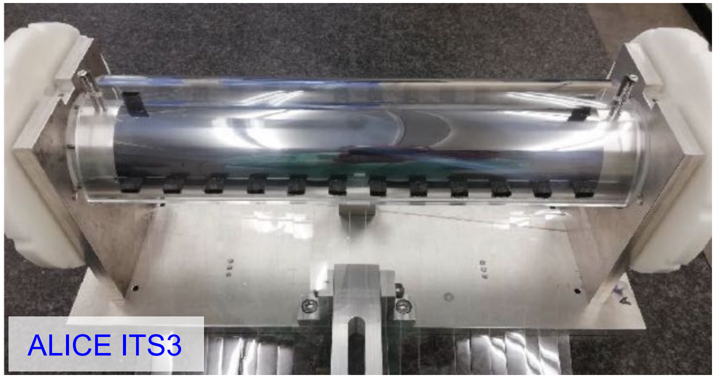
Outer barrel tracker support structure



Air-flow cooling mockup and simulation



Bent wafer-scale dummy sensor on foam support



- Engineering studies based on calculations, simulations, prototyping
  → confirm feasibility of detector concepts + provide input for realistic performance simulation
- Profit from recent developments in approved projects (Belle II, ALICE ITS3, CMB@FAIR)
- However: not all critical Lepton Collider requirements are fulfilled by these developments (e.g. barrel/endcap geometries, combination of low material budget and precise timing)
- Re-enforcement of engineering studies required to stay in line with detector-technology R&D

Conclusions

- Stringent requirements for Lepton-Collider vertex and tracking detectors:
  - Precision physics needs
  - Environmental conditions
- Several optimized detector concepts with different technology choices are proposed
- Broad silicon-pixel R&D program is pursued, profiting from advancements in semiconductor industry and from synergies with approved projects

- Fulfilling all Lepton-Collider requirements simultaneously remains challenging
- Further progress would benefit from an integrated focused effort, combining optimization + physics studies, technology R&D and detector-integration studies

Thanks to everyone who provided material for this talk!

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under GA no 101004761.
Some of the measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

Additional Material

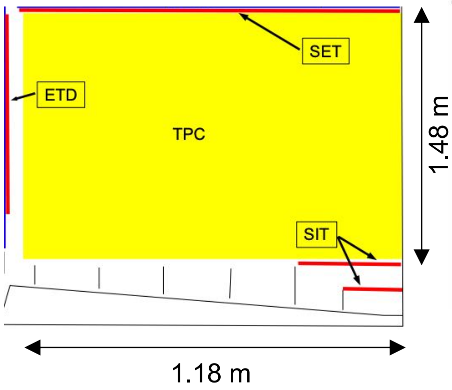
Vertex/tracking detector concepts

Collider	**ILC**		**CLIC**	**FCC-ee**			**CEPC**	
Detector Concept	SiD	ILD	CLICdet	CLD	FCC-ee IDEA	Noble LAr/LCr	CEPC baseline	CEPC IDEA
B-field [T]	5	4	4	2	2	2	3	2
Vertex inner radius [mm]	14	14	31	17 → 12	17 → 12	17 → 12	16	16
Tracker out. radius [m]	1.25	1.8	1.5	2.2	2.0	2.0	1.81	2.05
Vertex	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel
Tracker	Si-strips	TPC/ Si-strips	Si-pixel	Si-pixel	DC/ Si-strips	DC/Si-strips or Si-pixel	TPC/Si-strips or Si-strips	DC/ Si-strips

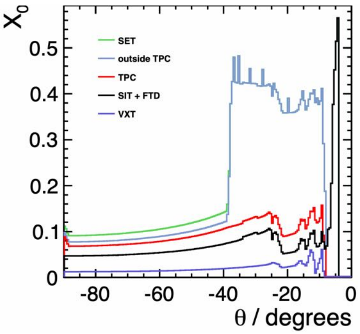
Time Projection Chamber as main tracker:

- Low material budget (5% X0 in barrel region incl. field cage)
- Continuous tracking → superior pattern recognition, dE/dx
- Rate limited
  → discarded for CLIC because of pileup
  → challenging for CC: low B field, up to 100 kHz physics rate
  → R&D for pixelated r/o to increase rate capability
- Silicon envelope to increase acceptance for dileptons, improve forward angular and overall momentum resolutions

ILD main tracker quadr.



ILD inner det. mat. budg.



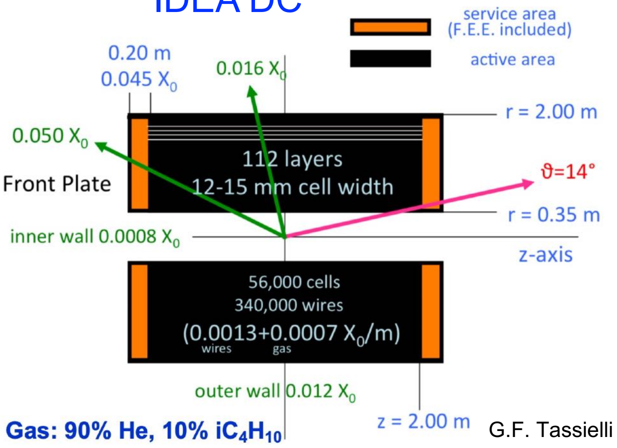
Vertex/tracking detector concepts

Collider	ILC		CLIC	FCC-ee			CEPC	
Detector Concept	SiD	ILD	CLICdet	CLD	FCC-ee IDEA	Noble LAr/LCr	CEPC baseline	CEPC IDEA
B-field [T]	5	4	4	2	2	2	3	2
Vertex inner radius [mm]	14	14	31	17 → 12	17 → 12	17 → 12	16	16
Tracker out. radius [m]	1.25	1.8	1.5	2.2	2.0	2.0	1.81	2.05
Vertex	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel
Tracker	Si-strips	TPC/ Si-strips	Si-pixel	Si-pixel	DC/ Si-strips	DC/Si-strips or Si-pixel	TPC/Si-strips or Si-strips	DC/ Si-strips

Drift Chamber as main tracker:

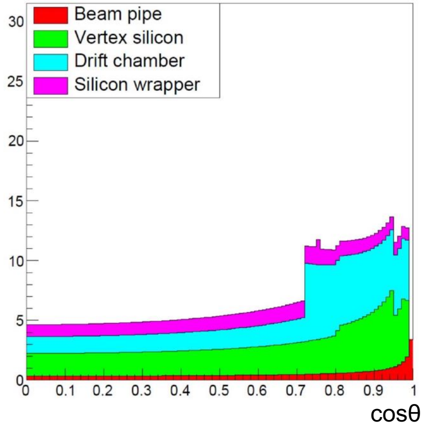
- Very low material budget (1.6% X0 in barrel region, dominated by wires)
- Continuous tracking, particle separation via cluster counting (dN/dx) or dE/dx → superior pattern recognition, particle ID (3σ K/p separation up to 35 GeV)
- Silicon envelope to increase acceptance for dileptons, improve forward angular and overall momentum resolutions

IDEA DC

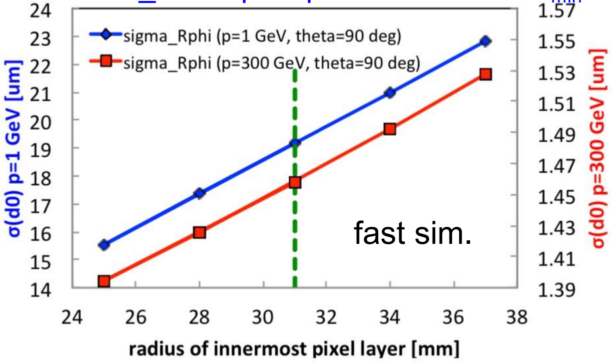


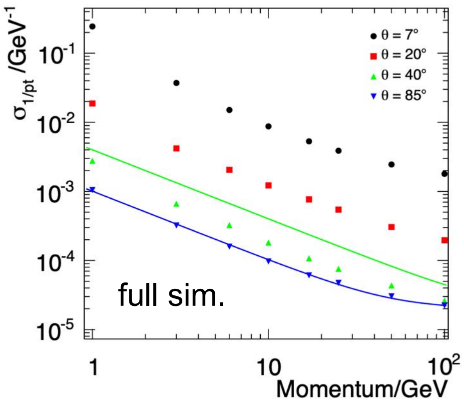
G.F. Tassielli

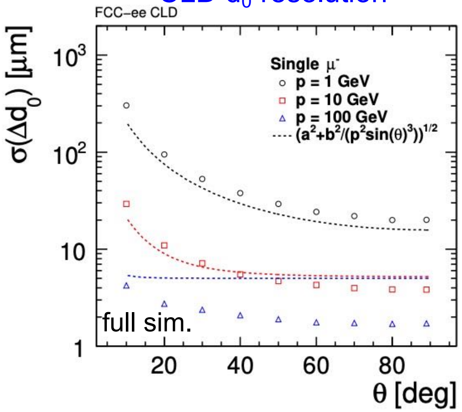
IDEA mat. budg.

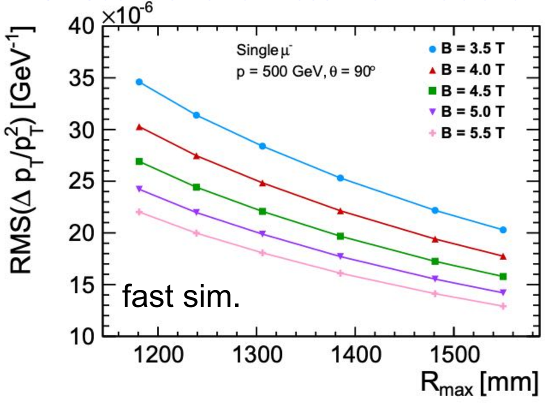


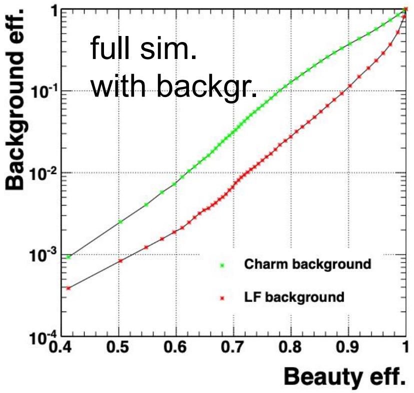
Detector concept optimization / validation

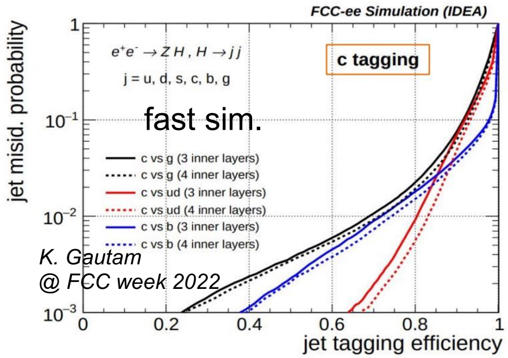

CLIC_ILD Impact-param. resol. vs. R_{min}


ILD momentum resolution


CLD d_0 resolution


CLICdet momentum resol. vs. B-field and R_{max}


SiD b-tagging performance

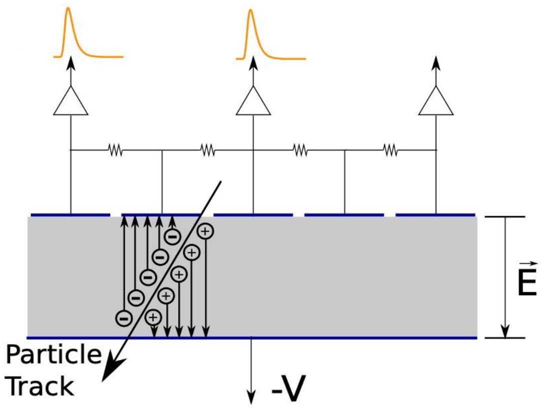

IDEA c-tagging performance

- Detecor concepts are optimised with fast parametric and full Geant-4 simulations;
- All detector concepts fulfil physics requirements in simulations;
  - So far: SiD,ILD,CLICdet,CLD validated in Geant4 based full-detector simulations
  - Other concepts validated in fast simulation, full simulation in progress
- Many studies pre-date recent R&D developments (e.g. monolithic trackers, pixelated TPC r/o)

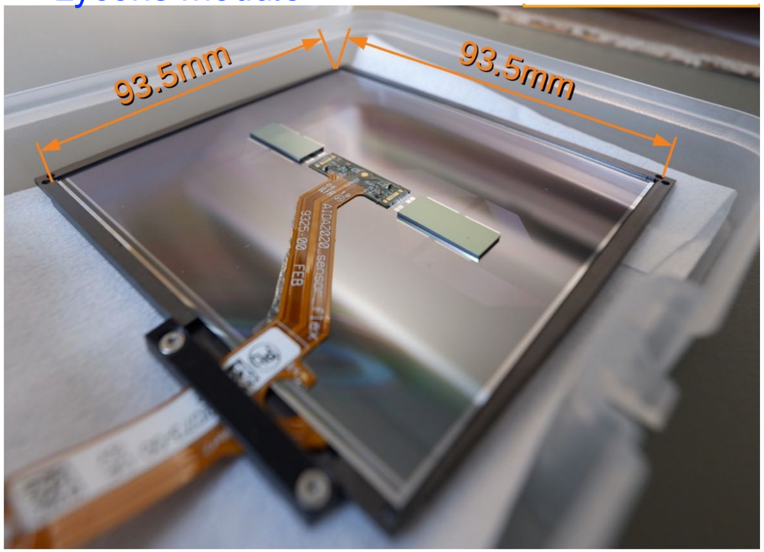
Hybrid strip detectors

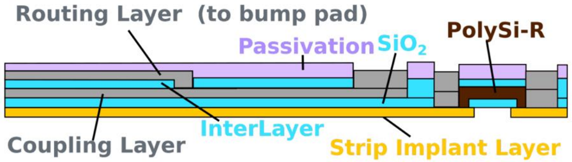
Hybrid strip detectors:

- baseline for ILC trackers (also suitable for CLIC outer layers)
- Well-established technology (e.g. HL-LHC)
  - low material + power (sparse readout)
  - large and fast signals (dE/dx)
  - high spatial resolution (charge interpolation) in R/phi direction
  - Allows for testing of advanced sensor concepts (e.g. stitched passive CMOS strip sensors)
  - Challenges: not for high occupancy regions; complex interconnect



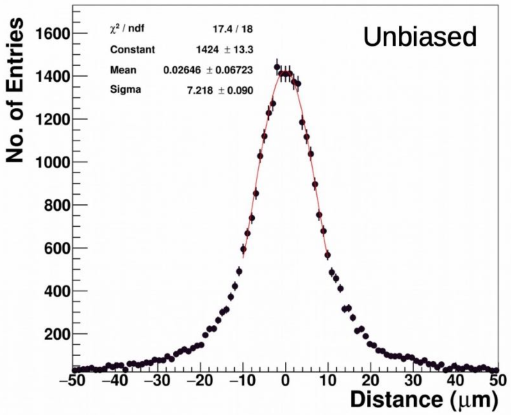
Lycoris module



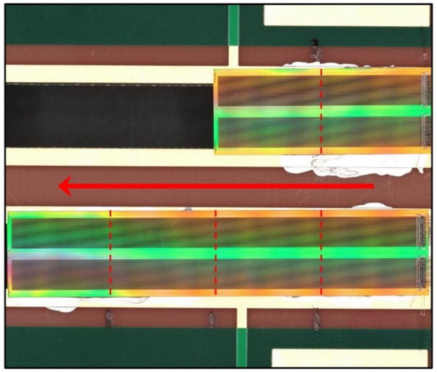


https://indico.cern.ch/event/995633/contributions/4259345/attachments/2210031/3740113/LCWS_2021.pdf

- Lycoris development DESY / SLAC:
  - 320 µm thick SiD strip sensors, 25 µm pitch
  - KPiX r/o ASIC
  - Chip bump-bonded on-sensor → high fill factor
  - 7 µm single-point resolution achieved in test beam
  - Test-case: beam telescope for PCMAG@DESY



Stitched passive CMOS sensors



Freiburg, DESY, Bonn

https://indico.cern.ch/event/995633/contributions/4259384/attachments/2209268/3738710/Passive%20CMOS%20Strip%20Sensors.pdf

Small collection electrode monolithic CMOS

- Modified 180 nm CMOS imaging process with small collection electrode (O(fF) capacitance)

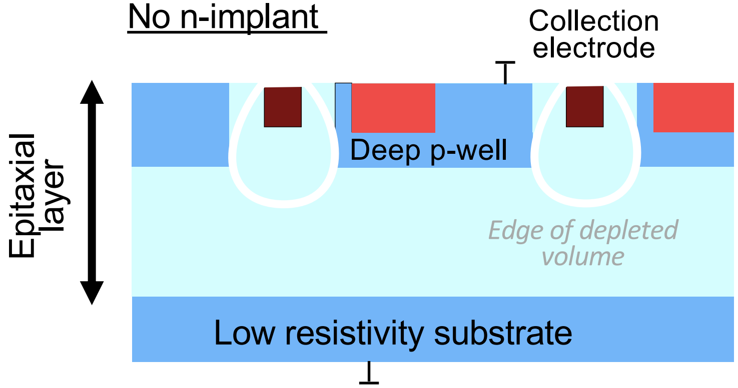
  (e.g. ALPIDE, (Mini-)MALTA, CLICTD, FASTPIX …)

- Deep low-dose n-implant for full lateral depletion

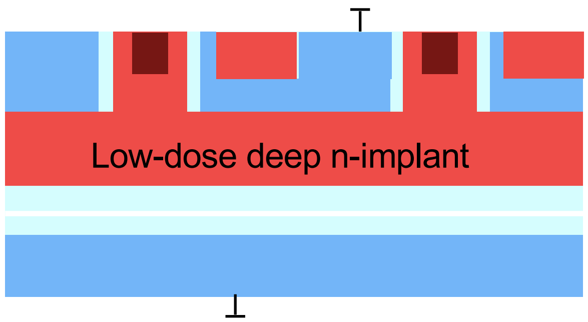
- Introduction of lateral doping gradient leads to accelerated charge collection
  - Comparison of various design modification in terms of detector performance

JINST 14 (2019) C05013

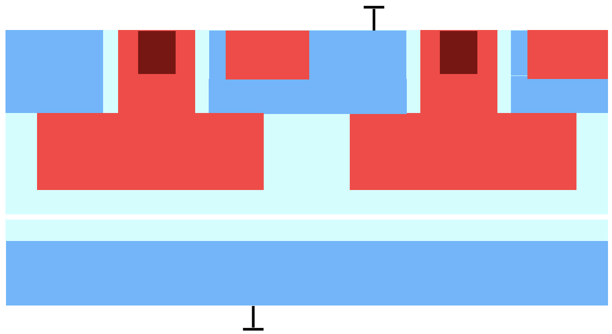
No n-implant



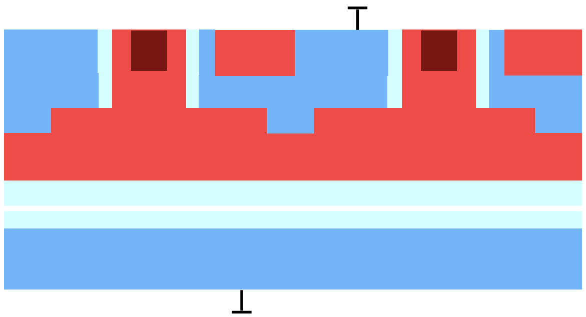
Continuous n-implant



Segmented n-implant



Extra deep p-well



Not to scale

Simulations

- Complex non-uniform field configurations in the small collection-electrode layout require sensor-design optimisations

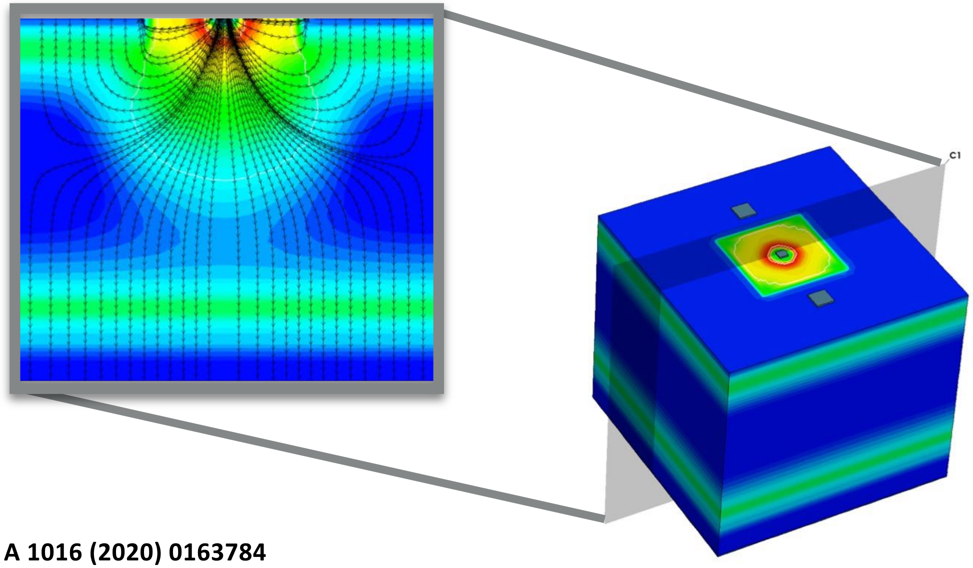
- Finite-element (3D TCAD) and Monte Carlo (Allpix Squared) simulation to combine accurate sensor modelling with high simulation rates

- Validated against transient 3D TCAD and data

https://gitlab.cern.ch/allpix-squared/allpix-squared

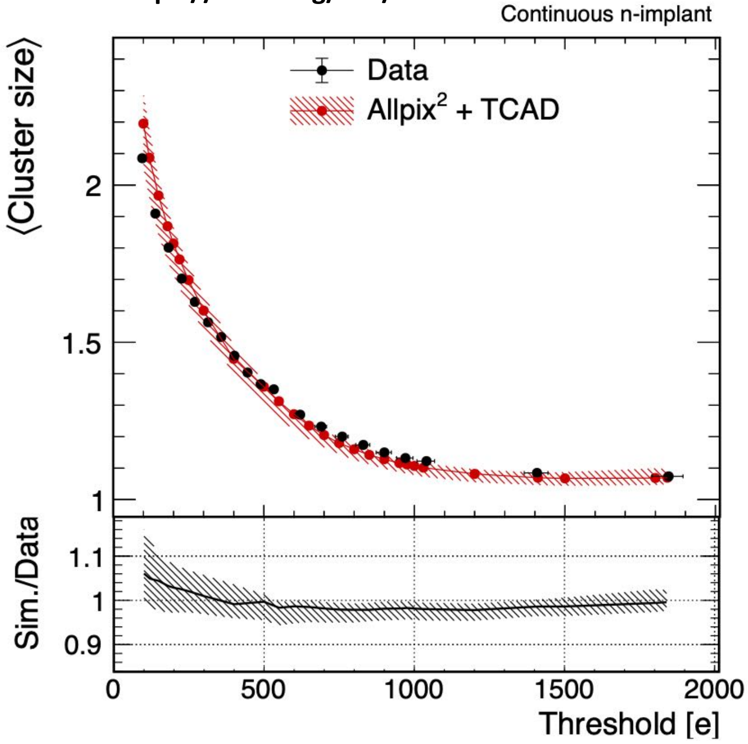
NIM A 901 (2018) 164172

Electrostatic potential + streamlines



NIM A 1016 (2020) 0163784

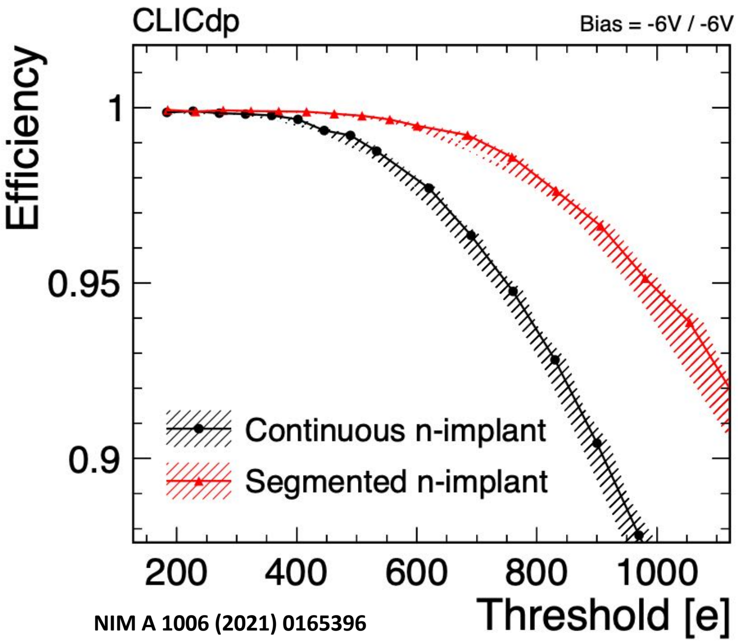
CLICdp-Pub-2021-003
https://arxiv.org/abs/2202.03221



CLICTD Technology Demonstrator

CLICTD 180nm monolithic sensor
- Channel pitch: 300 µm x 30 µm (16x128 channels)
- Sub-pixel pitch: 37.5 µm x 30.0 µm
- Analogue front-end of 8 sub-pixels grouped in one digital front-end (= readout channel)
- 8-bit ToA (10 ns ToA bins) + 5-bit ToT (combined ToA/ToT for every 8 sub-pixels in 300µm dimension)
- Sensors produced with different substrate materials (epitaxial, high-resistivity Cz) and thicknesses (40-300 µm)

IEEE Trans Nucl. Science 67.10 (2020): 2263-2272.



NIM A 1006 (2021) 0165396

Excellent performance observed in test-beam measurements:
- Threshold: ~100 - 180 e (occupancy < 10^{-3} hits/sec)
- Single pixel noise : < 15 e
- Hit-detection efficiency : > 99.7 %
- Spatial resolution : 4.6 µm
- Time resolution : 5.2 ns (Limited by front-end time resolution)

- Reduced charge sharing for pixel flavour with segmented n-implant leads to higher concentration of charge in one pixel cell

→ Improved efficiency at high thresholds

ACF for module integration

ACF module integration

Larger bonding pads: 80 μm – few mm diam.

→ Similar to industrial ACF usage

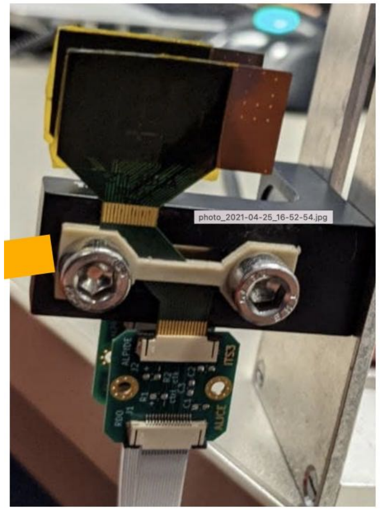
→ Good interconnect results

→ Topology / uniformity of UBM important

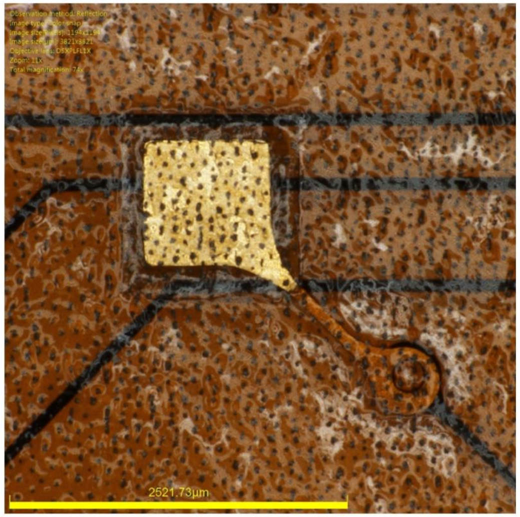
Various proof-of-concept projects:

- Beam tests of ALPIDE ACF modules
- Bonding tests with MALTA silicon bridges
- Tests with FCAL LUXE pad sensors

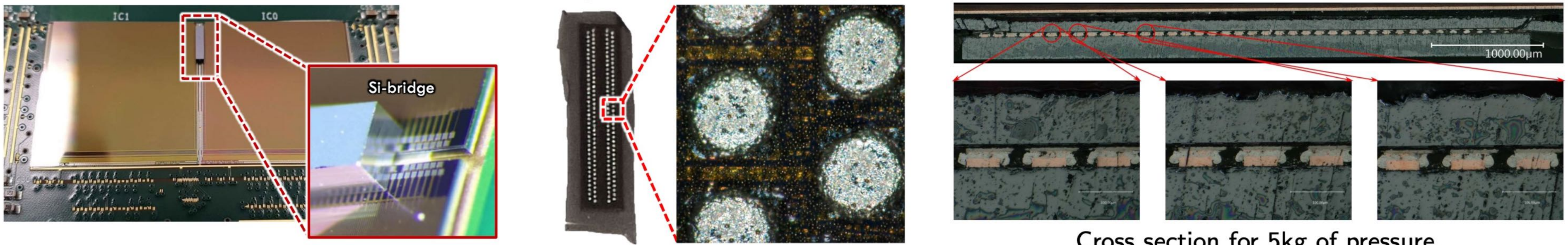
ALPIDE ACF module in DESY TB



ACF on LUXE pad



MALTA module building with silicon bridge and ACF bonding



MALTA double module with Si-bridge chip (images credit: Florian Dachs)

Si-bridge with ACF

ACF over Si-bridge pads

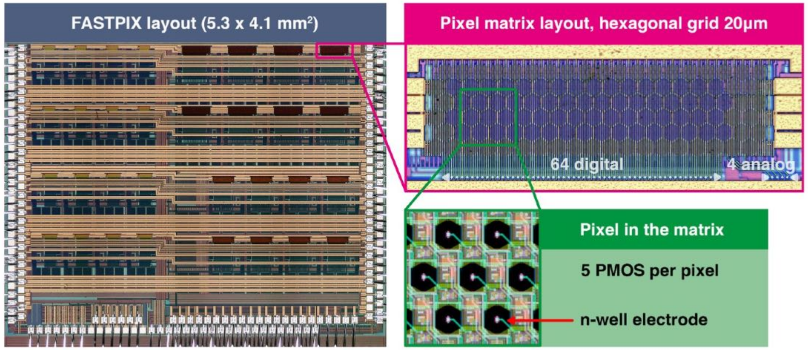
Cross section for 5kg of pressure.

M. Mager, F. Dachs, Y. Benhammou

ATTRACT FASTPIX

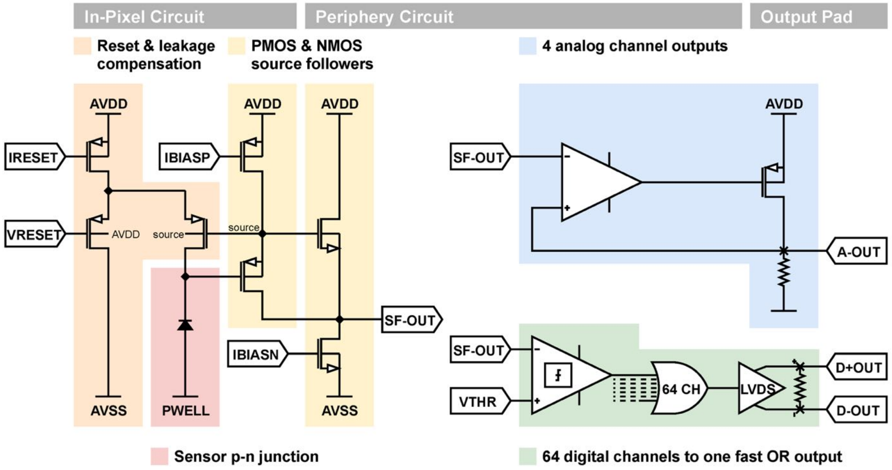
FASTPIX technology demonstrator for sub-ns timing

- Modified 180 nm CMOS imaging process
- 32 mini matrices of hexagonal pixels (8.66 to 20 µm pitch)
- 4 analogue outputs + 4x16 pixels with ToT/ToA
- Various sensor designs and process options
- Position and ToT encoding via delay lines (asynchr. r/o)



On-chip readout circuit

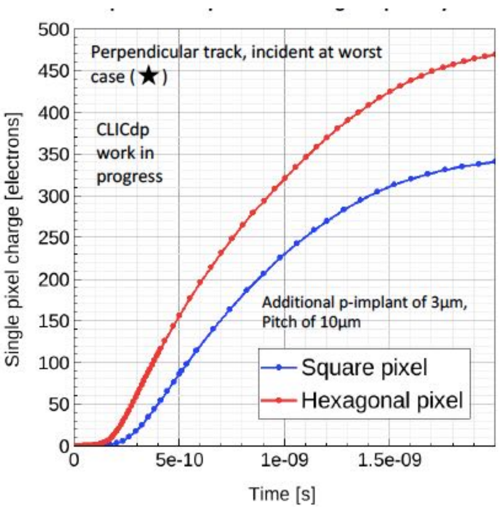
W. Snoeys, T. Kugathasan

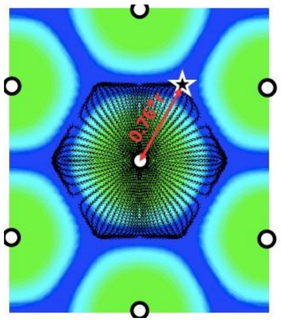


Simulated chip parameters:

Sensor capacitance		1 fF
Equivalent Noise Charge		11 e^-
Jitter (for Q_{in} = 1000 e^-)		20 ps
Power	In pixel source follower	18 µW
	Periphery discriminator	150 µW
	Analog monitoring buffer	20 mW

3D TCAD Simulation





T. Kugathasan et al: Monolithic CMOS sensors for sub-nanosecond timing, Hiroshima 2019

- Optimised for precise sensor timing in 3D TCAD simulation studies
- Hexagonal pixel layout:
  - Improved charge collection at pixel edges
  - Reduced number of neighbouring pixels → Less charge sharing

Caribou DAQ

Versatile data acquisition system based on programmable hardware

https://gitlab.cern.ch/Caribou

System-on-Chip (SoC) board

- Embedded CPU for DAQ, user interface, operating system (Linux)
- Field programmable gate array (FPGA) for detector control and data processing

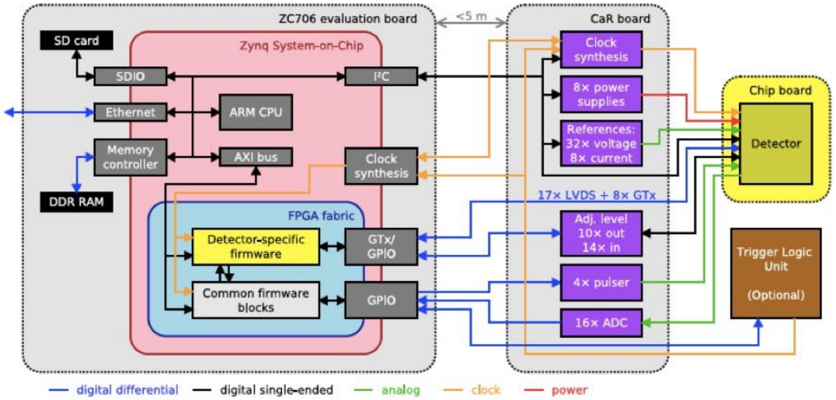
Control and Readout (CaR) interface board

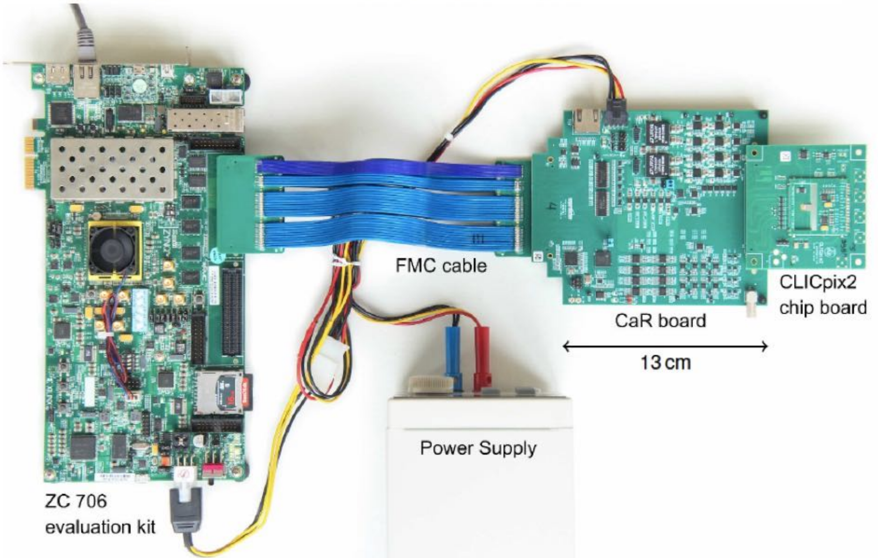
- Physical interface from SoC board to detector chip
- Voltage regulators, ADCs, pulse/clock generator

Application-specific detector carrier board

- Only detector chip and passiv components

- Successfully used for ATLASPix, ATLASPix2, ATLASPix3, CLICpix2/C3PD, H35Demo/FEI4, RD50-MPW1





https://iopscience.iop.org/article/10.1088/1748-0221/12/01/P01008

Allpix-Squared simulation toolkit

Selected Applications

- **Detectors for HEP**
  - MAPS (CLICTD, ALICE, ARCADIA,…), RD53, ATLAS ITk Strips, …
- **NASA / Space Radiation Analysis**
- **ISS radiation monitor simulations**
- **Germanium X-ray detector (Synchrotron SOLEIL)**
- **Education / Outreach activities**
  - EDIT Detector School, Beamline for Schools 2019,…

Publications

NIM A 901 (2018) 164-172

NIM A 964 (2020) 163784

Website

https://cern.ch/allpix-squared

Repository

https://gitlab.cern.ch/allpix-squared/allpix-squared

User Forum

https://cern.ch/allpix-squared-forum/

User Manual

https://cern.ch/allpix-squared/usermanual/allpix-manual.pdf

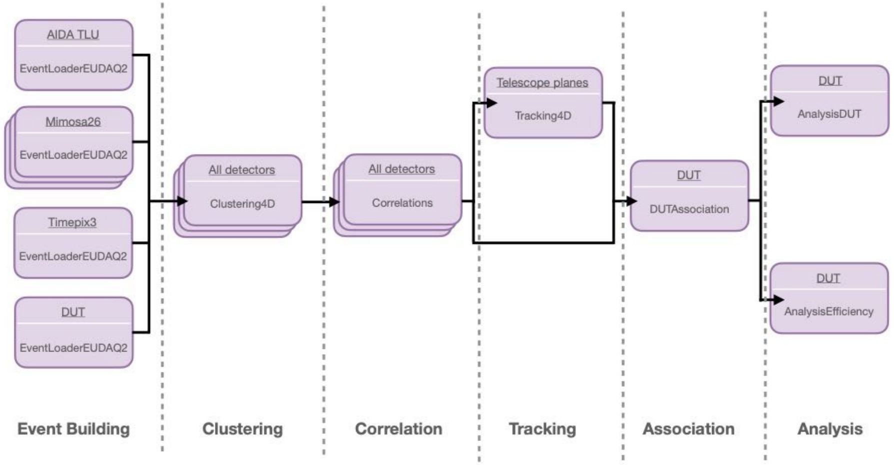
Mailing list

https://e-groups.cern.ch/e-groups/Egroup.do?egroupId=10262858

Corryvreckan test-beam analysis framework

Reconstruction and analysis software for test-beam data

- Highly flexible/configurable by using separate modules for each reconstruction/analysis step



- Wide user base e.g.

  CLICdp, ALICE ITS3, ATLAS ITk,
  LHCb Ib/II, Mu3e, etc.

Corryvreckan

2021 JINST 16 P03008

- Visit the website for the manual, tutorials and more

  https://cern.ch/corryvreckan

- Check out the repository

  https://gitlab.cern.ch/corryvreckan/corryvreckan

- Join the discussion in the forum

  https://corryvreckan-forum.web.cern.ch/

- Contact us

  corryvreckan.info@cern.ch

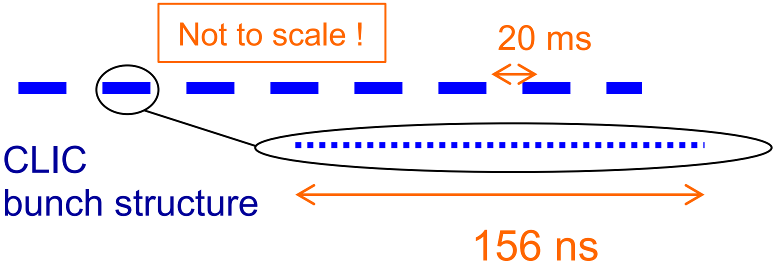
Experimental conditions at CLIC

- CLIC operates with bunch trains, 50 Hz repetition rate

→ Low duty cycle

→ Trigger-less readout between trains

→ Allows for power-pulsed operation of detector, to reduce average power consumption

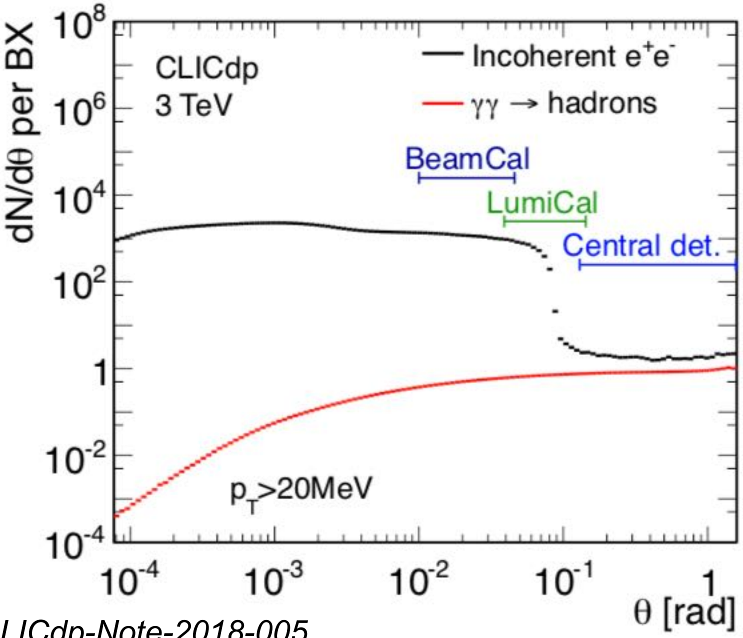


- Collisions within 156 ns bunch trains
- High E-fields lead to Beamstrahlung

→ High rates of beam-induced background particles

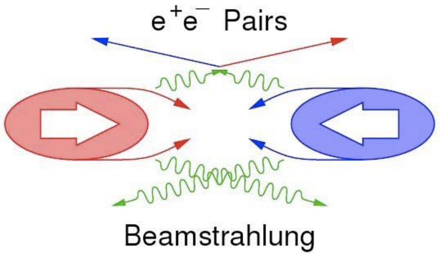
→ Drives detector design (layout, granularity, timing)

Very small bunches:
40 nm (x) x 1 nm (y) x 44 µm (z)
(at 3 TeV)



CLICdp-Note-2018-005

Main backgrounds in detector



- **Incoherent e+e- pairs**
  - 19k particles / bunch train at 3 TeV
  - Constrains beam pipe radius, granularity
- $\gamma\,\gamma \rightarrow$hadrons events
  - 17k particles / bunch train at 3 TeV
  - Constrains granularity, layout, impacts physics

High instantaneous hit rates (up to 6 GHz/cm²), however: very low readout rate (50 Hz)