X-CHIP-04, a novel monolithic pixel detector for X-ray imaging

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Introduction

- X-CHIP-04 is a monolithic active pixel sensor developed for soft X-ray imaging and advanced dosimetry designed in 180 nm high voltage (HV) partially depleted (PD) silicon on insulator (SOI) CMOS technology.
- A novel feature of this sensor is the capability to operate in two modes:
  - Hit counting mode (X-ray imaging)
  - ADC mode (advanced dosimetry)
- The hit counting mode is primarily designed for radiation imaging and the ADC mode is intended for measurement of energy deposited in each pixel.

Pixel design

- Signal range: 1 ke^- - 10 ke^-
- Energy range: 3.6 keV - 36 keV
- Sensor diode in handle wafer
- Charge Sensitive Amplifier (CSA)
- Peak detector hold (PDH)
- Discriminator
- 16-bit counter used in hit counting mode

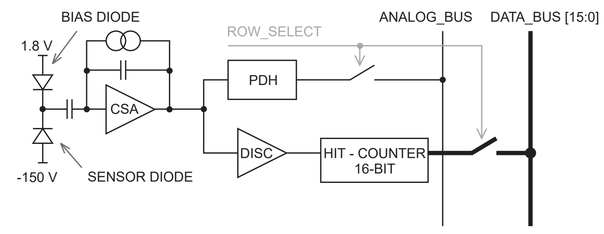

Figure 4: Pixel block diagram.

SOI Technology

- The sensitive diodes are formed by the N-type implants in the P-type handle wafer with resistivity of 100 Ωcm and thickness of 300 µm.
- Typical bias voltage is 150 V, depleting the handle wafer by approximately 37 µm (computed from handle wafer resistivity).
- Typical leakage current of the entire sensor is 20 nA at room temperature.
- The pixel electronics is integrated in epitaxial layer separated from the handle wafer by BOX.
- The handle wafer is partially depleted.

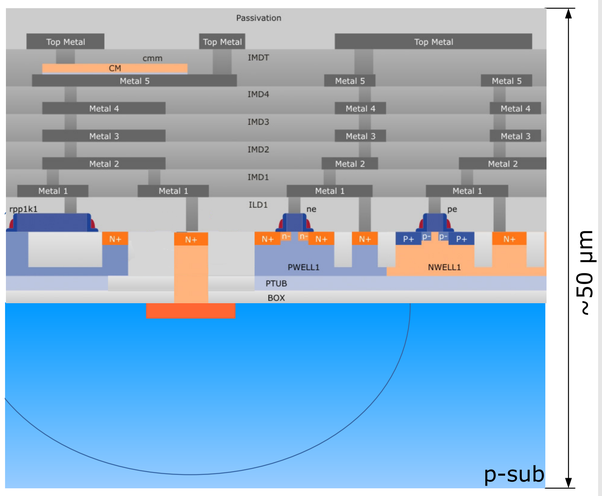

Figure 1: Cross section of an SOI monolithic detector (not to scale).

Spectrum measurement in ADC mode

Spectral performance of the ADC mode was demonstrated with radioactive sources ^{55}Fe and ^{238}Pu. Spectral lines of various elements originating from X-ray fluorescence were also measured. X-CHIP-04 spectral capabilities are shown in Fig. 5.

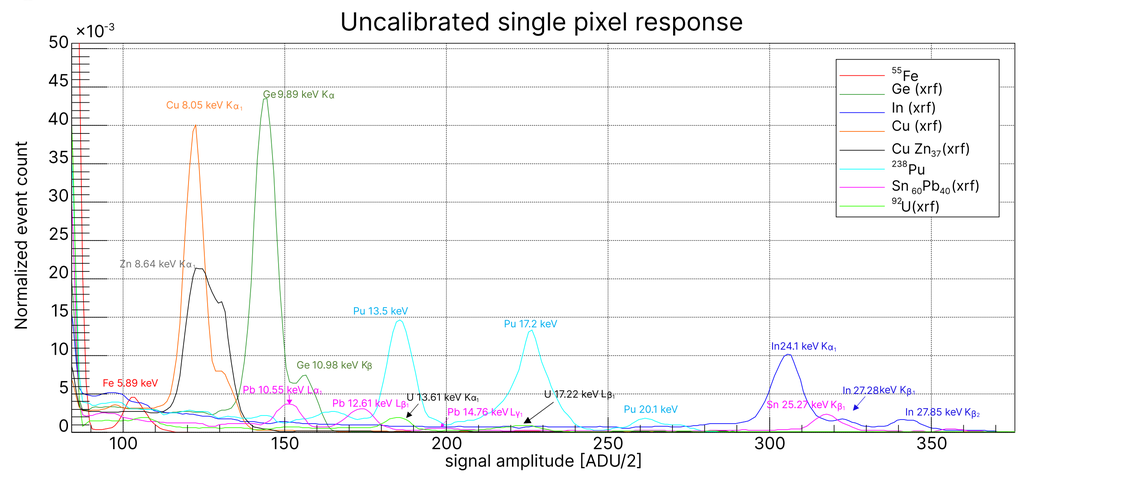

Figure 5: An uncalibrated X-CHIP-03 single-pixel response in ADC mode to soft X-rays.

X-CHIP-04 features

- Monolithic Active Pixel Sensor (MAPS) ASIC
- X-CHIP-04 is an improved version of the previous X-CHIP-03 [1]
- 64 × 64 pixel matrix
- 60 µm pixel pitch
- 4 × 4.8 mm^2 chip dimensions
- 64 column-parallel 10-bit SAR ADCs
- Hit counting range 16-bits
- Bandgap reference on chip
- LVDS (400 MHz), SPI (50 MHz) readout modes
- Maximum frame rate 634 frames/s at readout frequency of 50 MHz and with exposition time of 10 µs.
- Sensor bias -150 V
- Power supply 1.8 V
- Max. total current consumption 30 mA
- Complexity: 3.5 M transistors

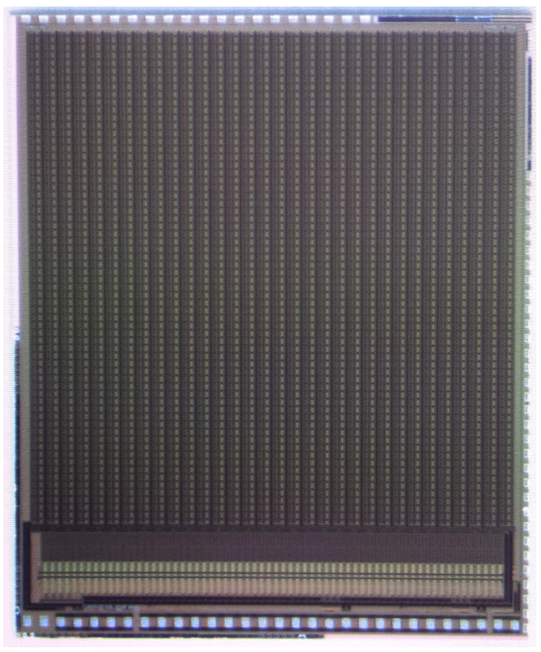

Figure 2: X-CHIP-04 ASIC.

Results in hit counting mode

- Fig. 6 and Fig. 7 demonstrate the X-ray imaging capabilities of the used technology. The small sensitive area of the sensor was extended by mounting the detector module on a moving platform which allows scanning of larger objects.

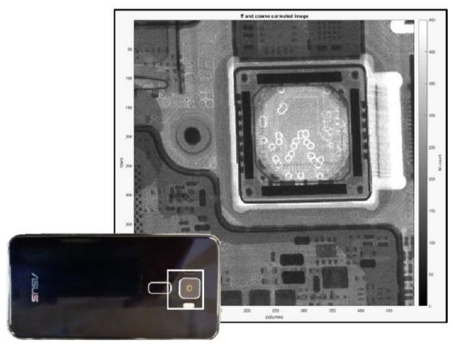

Figure 6: X-ray image of a cell phone.

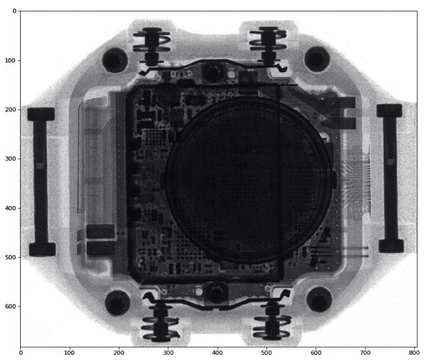

Figure 7: X-ray image of a wristwatch.

Conclusions

A novel SOI CMOS MAPS sensor, supporting hit-counting mode and ADC mode, was designed and evaluated. Presented results demonstrate good spectrometric capability and the ability of X-ray imaging in hit counting mode. X-CHIP-04 ASICs are available free of charge for non-commercial R&D purposes.

ASIC architecture

- Impelemented feature of inject for calibration of each pixel and ADCs.
- Chip is cofigurable with global and local configuration.
- Radiation tolerant technology [2]:
  - Bit flip cross section was found to be low compared to the bulk CMOS.
  - Threshold for TID effect is 2 kGy @ 15 Gy/min.

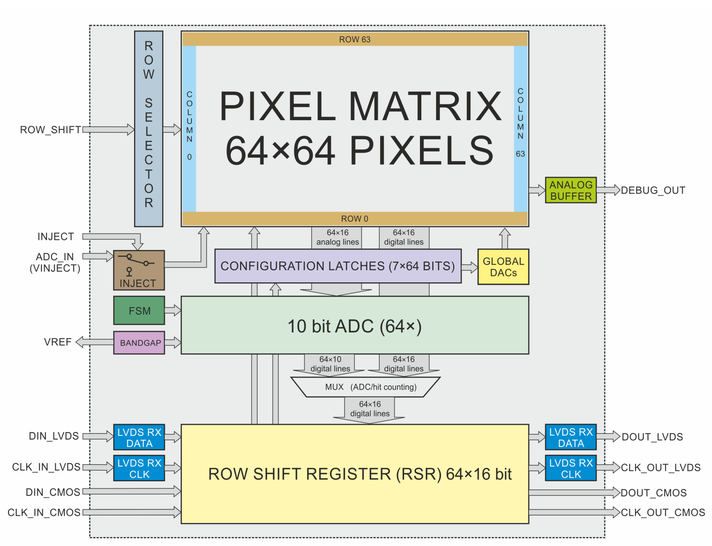

Figure 3: X-CHIP-04 ASIC architecture.

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