ColorPix - a front-end ASIC for color imaging

J. Jirsa[1,2], J. Gečnuk[1], Z. Janoška[1], J. Jakovenko[2], V. Kafka[1], M. Marčišovská[1], M. Marčišovský[1], P. Staněk[1], L. Tomášek[1], P. Vančura[1]

[1]Department of Physics, Faculty of Nuclear Sciences and Physical Engineering, Czech Technical University in Prague, Czech Republic
[2]Department of Microelectronics, Faculty of Electrical Engineering, Czech Technical University in Prague, Czech Republic

CAPADS FNSPE, CTU

Introduction

- X-ray color imaging is a promising method for medical imaging and non-destructive testing.
- It uses photon-counting hybrid detectors with multiple threshold levels.
- To enhance the spatial resolution of the detectors, a shrinking of pixel size is needed.
- With decreasing pixel pitch size, charge sharing and fluorescent photons cause the charge spread across the pixel matrix.
- Therefore, on-chip algorithms with inter-pixel communication are needed to compensate for these effects [1]
- This work introduce a ColorPix ASIC, with target to overcome these effects.

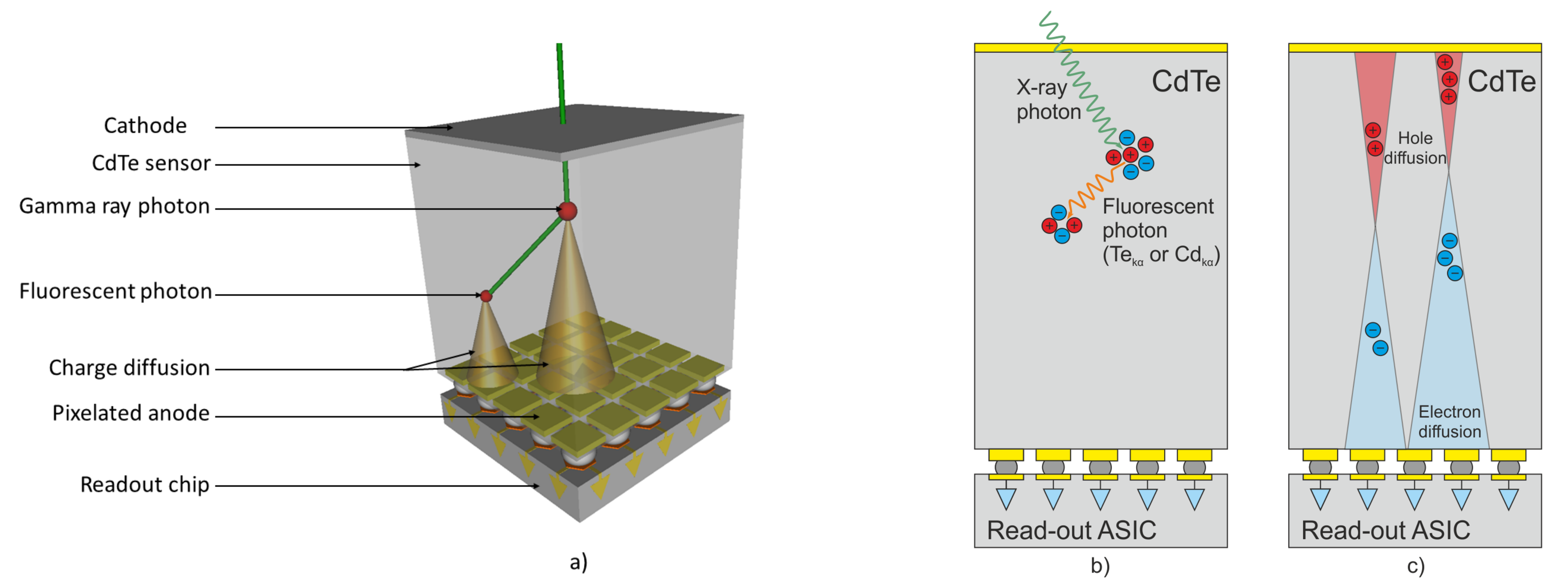

Figure 1: (a) - 3D model of CdTe sensor, (b) - Illustration of fluorescent photon generation and (c) - Charge diffusion.

ColorPix overview

- Hybrid pixel detector.
- Technology 65 nm CMOS.
- 32 × 32 pixel matrix.
- 70 µm pixel pitch.
- 2.2 × 2.2 mm^2 sensitive area.
- Integrated current reference.
- 3.2 Gbit serial readout.
- 50 MHz serial configuration.
- Inter-pixel communication.
- ten equidistant threshold levels.
- ten 12-bit counters.
- Multiple operation modes: Color, Mono, Custom color.
- Pixel inject.
- Charge summing mode.

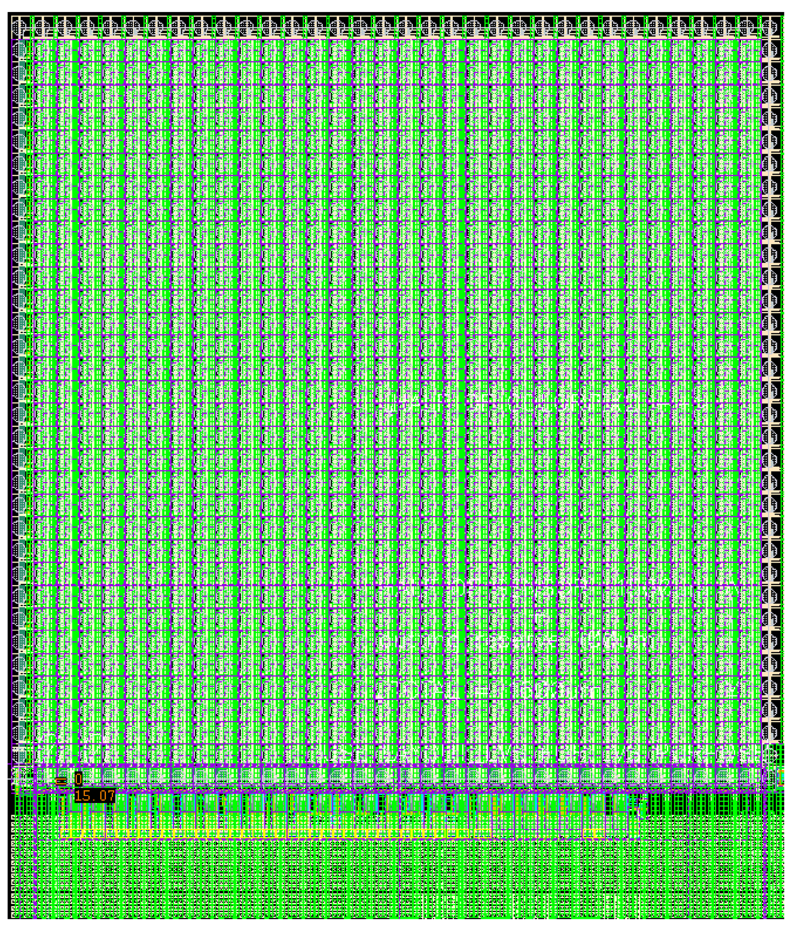

Figure 2: ColorPix ASIC layout.

Pixel design

- The signal produced by incoming photons is amplified using Charge Sensitive Amplifier (CSA).
- The output signal is then dived into two branches: Digital and Analog.
- The digital branch starts with a pixel discriminator, which signalizes whether the pixel collected some charge. The output of the pixel discriminator is connected to pixel digital logic.
- Digital logic is responsible for inter-pixel communication (cluster formation) and sampling.
- The Analog branch follows by the Peak detector and hold circuit (PDH), which memorizes the maximum value of CSA.
- Next is the Operational Transconductance amplifier, which converts the PDH output signal to current.
- Finally, the multi-threshold window discriminator performs digitization by selecting one counter that will be incremented.

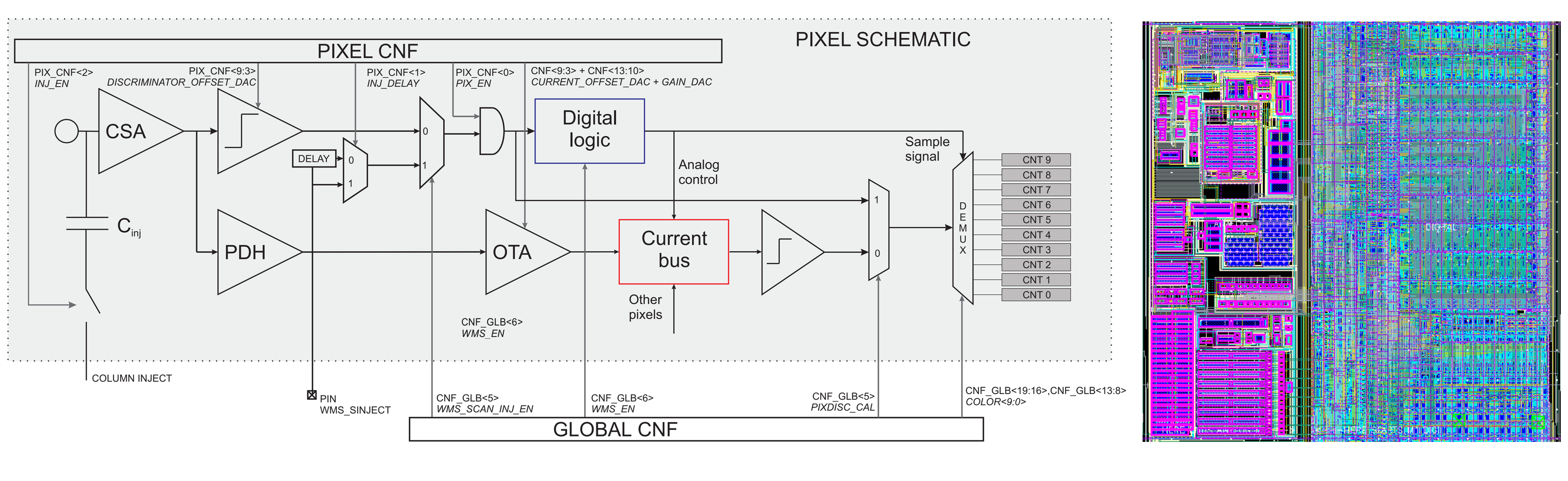

Figure 3: (Left) - pixel schematic diagram (Right) - pixel layout.

ColorPix architecture

- The pixel matrix consists of 32 x 32 pixels with 18-bit configuration latches.
- 1 µA current reference.
- Configurable bias block with 8-bit DACs, tunes analog circuit operation points.
- Gigabit block with integrated PLL using 100 MHz reference clock.
- Global configuration 768 bits.
- Configurable analog amplifier for debugging purposes.

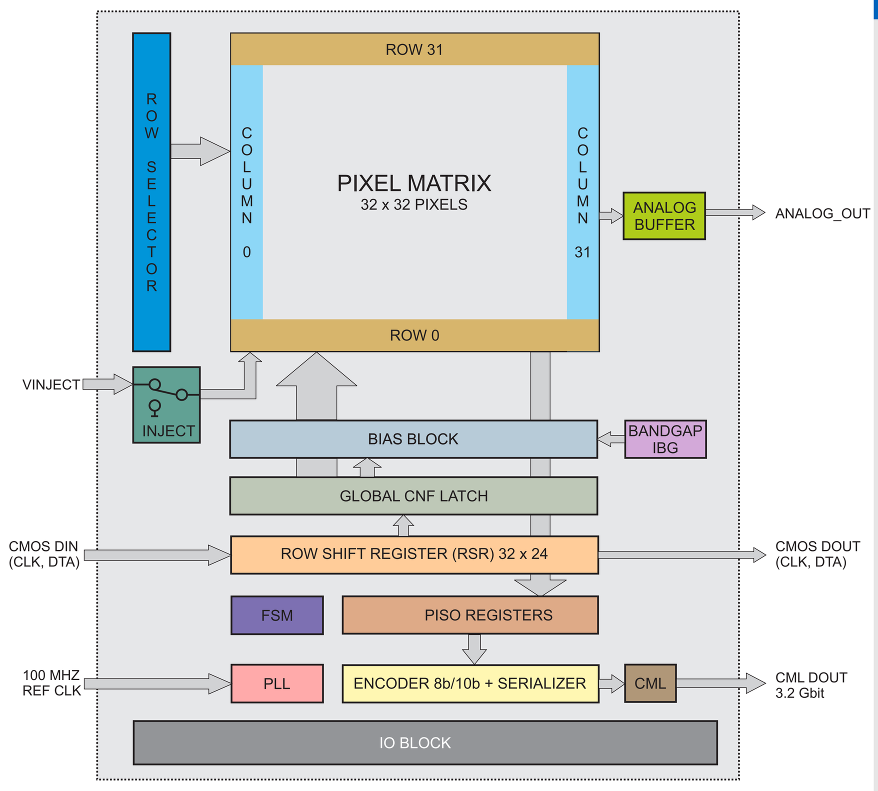

Figure 4: ColorPix block diagram

ColorPix - Monte-Carlo simulation

- We have performed a 3D Monte Carlo simulation with 10^4 photons to investigate the detector response to X-ray photons.
- The following procedure describes the MC simulation of 2 mm thick CdTe bonded to ColorPix ASIC biased at -1000 V:
  1. A monochromatic beam of 60 keV X-ray photons was aimed at one pixel with random position within the pixel.
  2. The depth of the interaction was computed randomly for each photon using mass absorption coefficient taken from NIST database.
  3. Once the position of interaction is known, a charge spread was modeled using the following equation: $\sigma = \sqrt{2Dt_d}$.
  4. Decide whether a fluorescent photon is generated. If yes, perform steps 2,3 for the fluorescent photon.
  5. After each photon interaction, the number of collected electrons for each pixel was calculated.
  6. Inject the collected charge to the pixel matrix.
- The MC simulation was done with two configuration: 1. charge summing algorithm turned on 2. charge summing algorithm turned off
- The plot in Figure 5. shows the charge summing algorithm capabilities compared to a single-pixel regime.

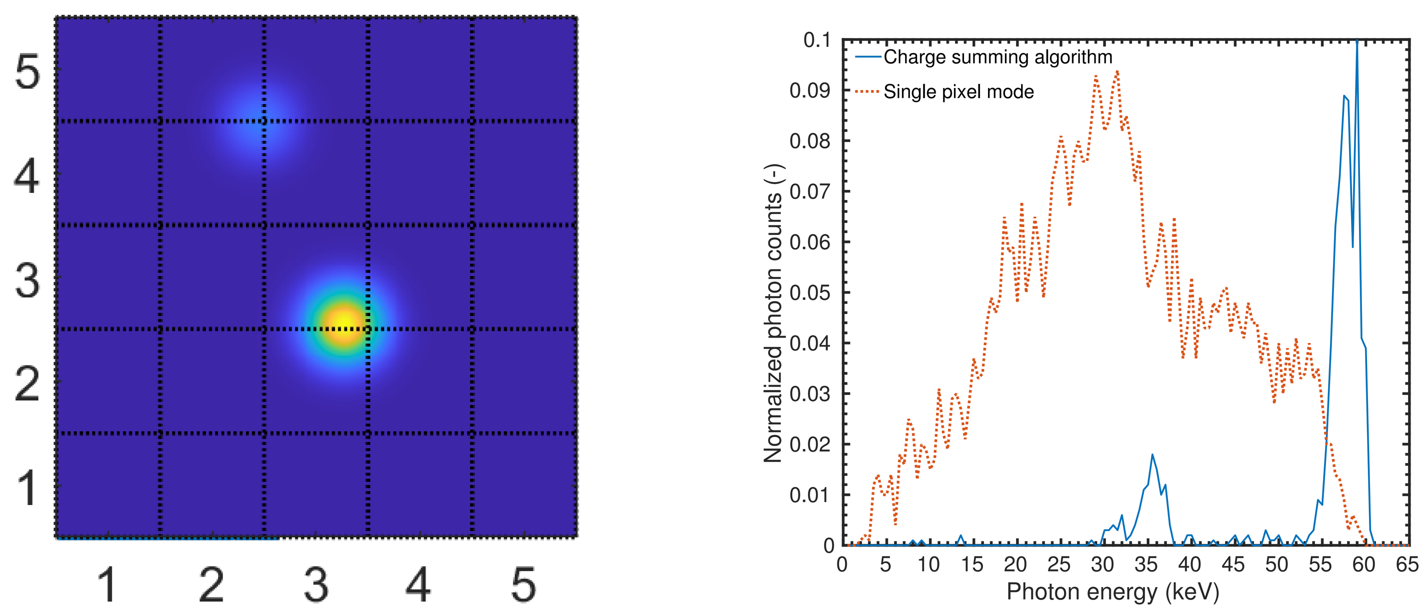

Figure 5: (Left) - e$^-$ density at collection electrodes after X-ray photon interaction (Right) - Normalized photon counts at central pixel in single pixel mode (red) and charge summing mode (blue).

Conclusions

This work has introduced a design of novel photon counting detector for X-ray imaging. The key features of the detector has been introduced. The ASIC has been send for fabrication in 9/2022. The testing will be done in 2023.

References

[1] Thomas Koenig, Elias Hamann, Simon Procz, Rafael Ballabriga, Angelica Cecilia, Marcus Zuber, Xavier Llopart, Michael Campbell, Alex Fauler, Tilo Baumbach, and Michael Fiederle.
Charge summing in spectroscopic X-ray detectors with high-Z sensors.
IEEE Transactions on Nuclear Science, 60(6):4713–4718, 2013.

Acknowledgements

The work was supported from European Regional Development Fund-Project "Center of Advanced Applied Science" No. CZ.02.1.01/0.0/0.0/16-019/0000778 and by the Grant Agency of the Czech Technical University in Prague, grant No. SGS20/175/OHK3/3T/13.

EUROPEAN UNION
European Structural and Investment Funds
Operational Programme Research, Development and Education

MINISTRY OF EDUCATION, YOUTH AND SPORTS