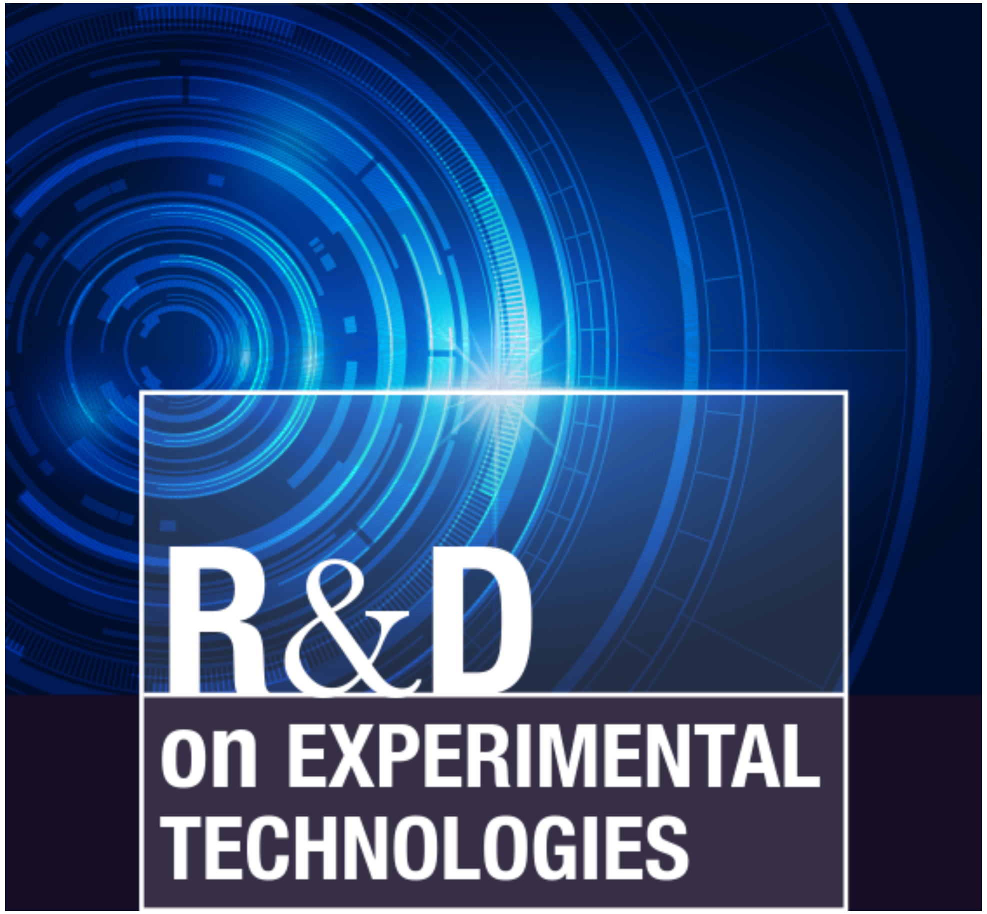
Optimization of a 65 nm CMOS imaging technology for monolithic sensors for high energy physics

CERN EP R&D

WP1.2 Monolithic Pixel Detectors

Many contributors, see next page



Optimization of a 65 nm CMOS imaging technology for monolithic sensors for high energy physics

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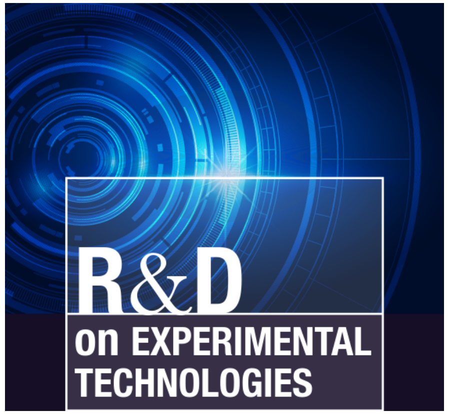
Strong synergy with ALICE ITS3 upgrade



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TPSCo: M. Suzuki**, Tower Semiconductor:** A. Fenigstein, and **Etesian Semiconductor:** A. Haim, E. Toledano

EP RD WP1.2 on monolithic CMOS sensors

Long term goal: develop CMOS sensors in sub 100nm technologies

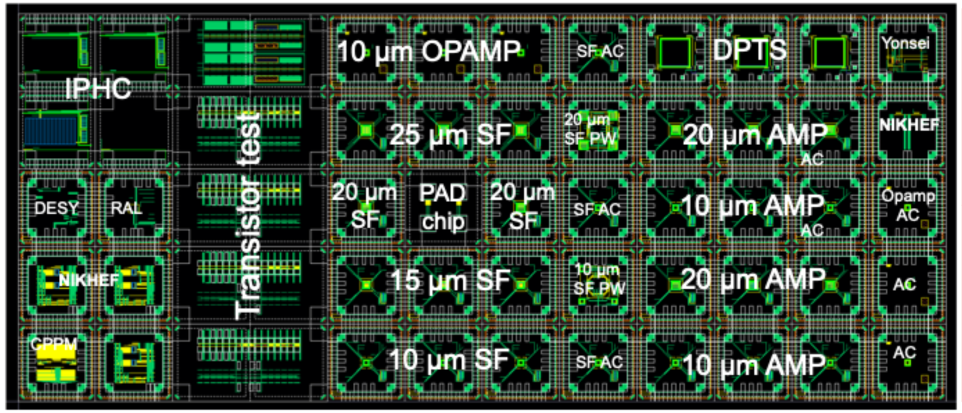
- Synergy with development of the stitched sensor in the ALICE ITS3 upgrade (see Lukas Lautner's presentation)

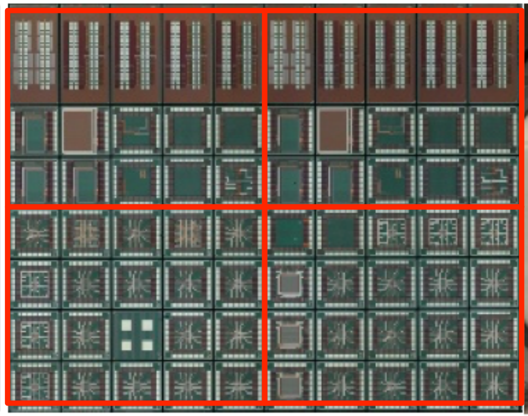
First technology selected: TPSCo 65 nm CMOS imaging technology

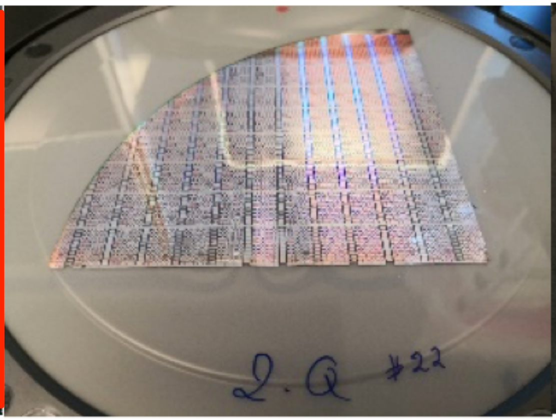
- TPSCo (joint venture TJ & Panasonic): several 65 nm flavors: high density logic, RF, and imaging (ISC)
- ISC preferred: 2D stitching experience, special sensor features, different starting materials, lower defect densities, etc
- Initially 5 metal layers, now 7 metals

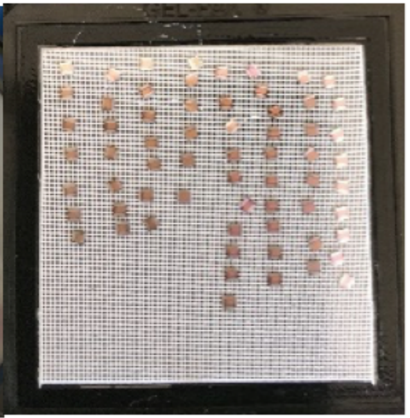
First submission: Multi Layer per Reticle MLR1

- Significant contribution from outside groups (from ALICE but not only) to design and test (!), also financially
- Many test chips of 1.5 x 1.5 cm^2 or twice that size.
- How to optimize sensor integrated with complex in-pixel circuitry ?
- GDS submitted Dec 1, 2020, released for manufacturing end of Feb 2021, chips ready to test, Sept, 2021



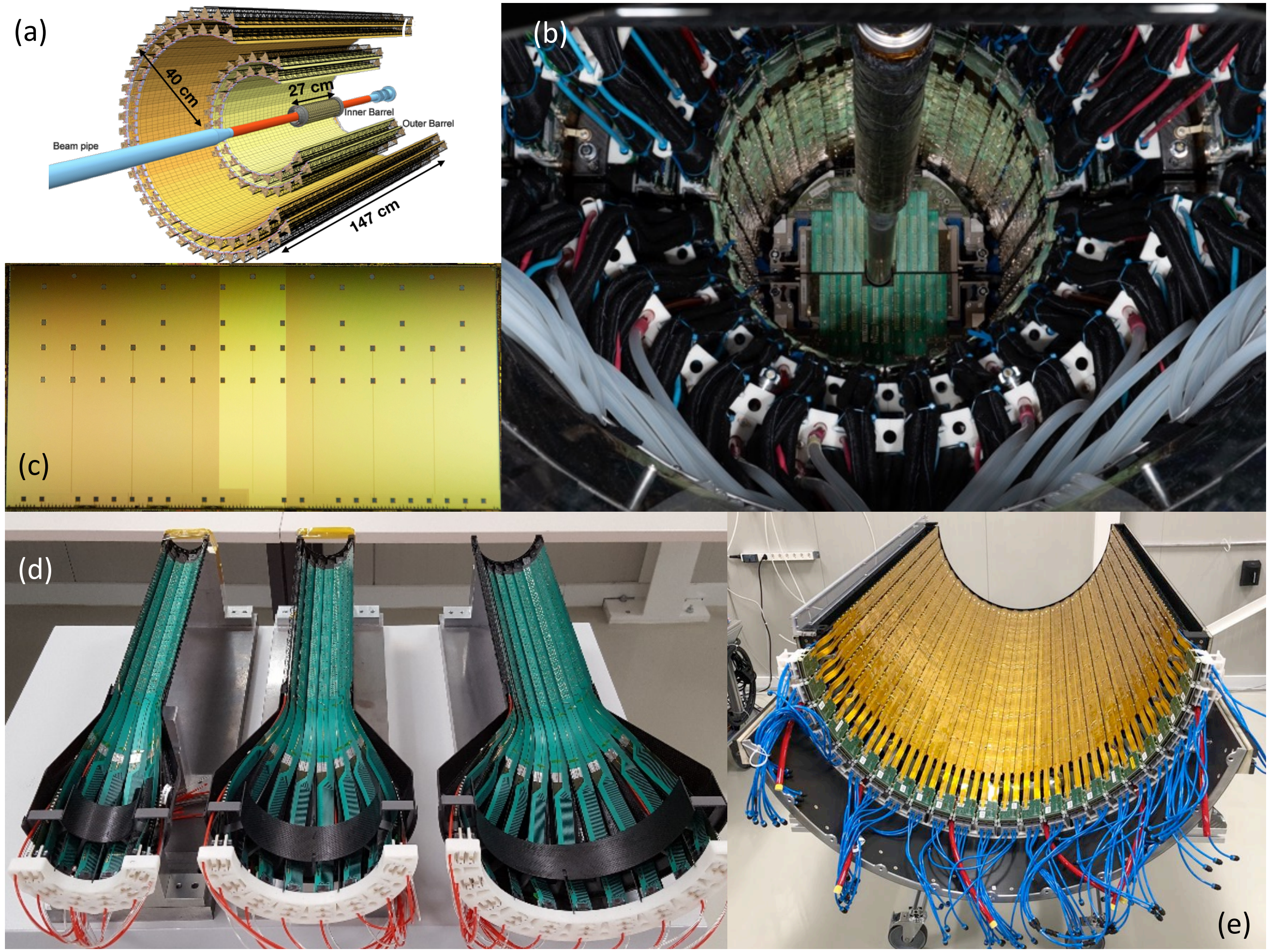


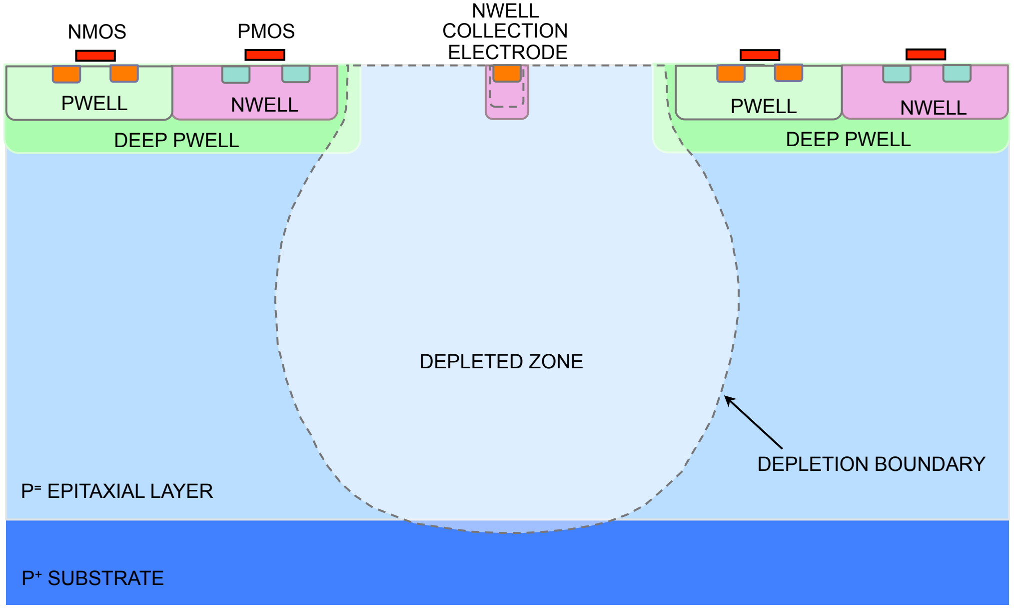




State of the art: ALICE Inner Tracking System 2 : 10 m^2 with 3x1.5 cm^2 ALPIDE chips

TowerJazz 180 nm imaging CMOS technology, development 2012-2016

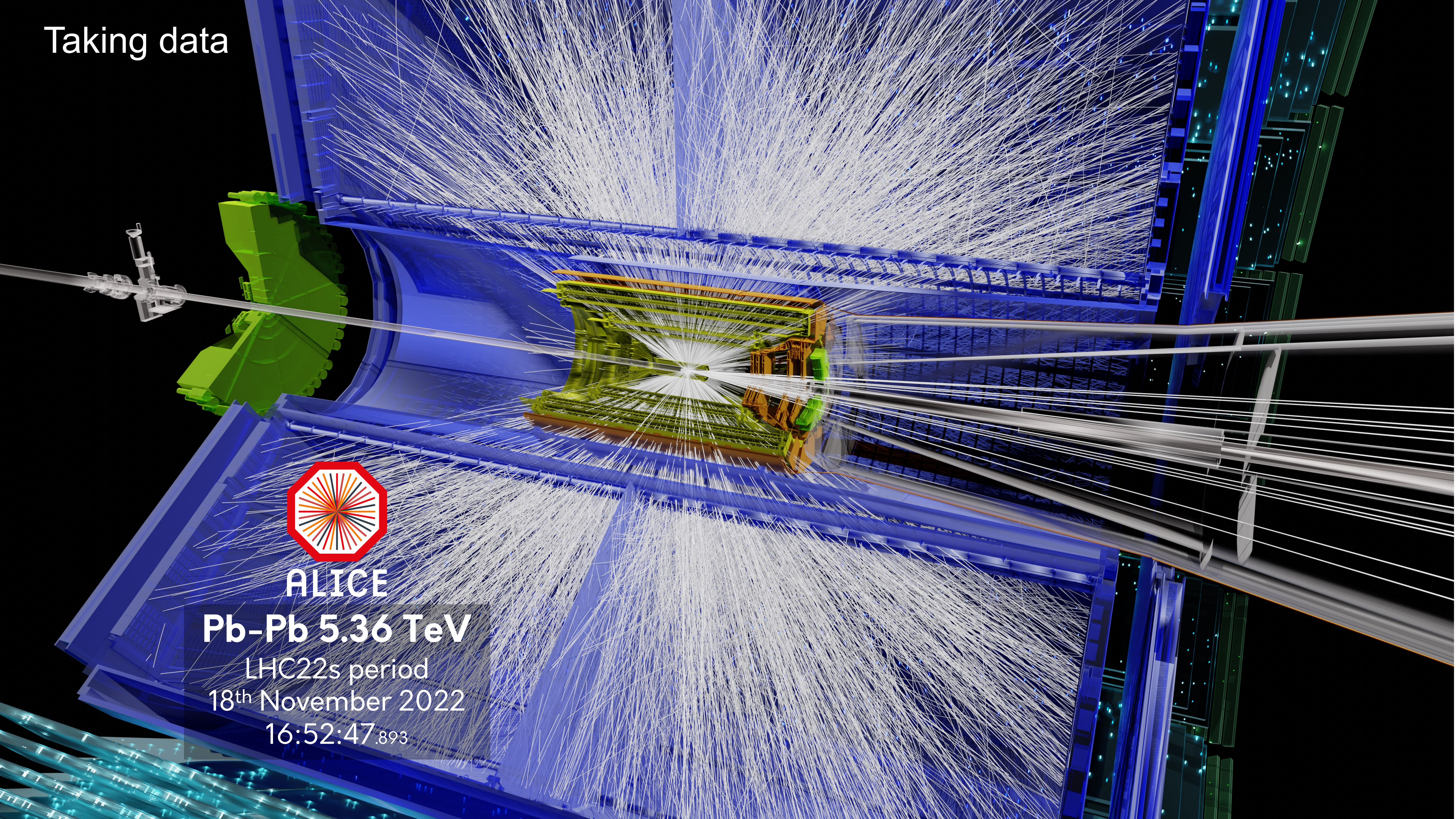




ALPIDE CHIP

- 512 x 1024 pixels of 28 x 28 µm^2
- Full CMOS in the pixel (deep pwell)
- 40 nW front end, sparse readout
- Matrix 6 mW/cm^2, up to 40 mW/cm^2 including periphery
- Standard process: sensitive epitaxial layer not depleted

Taking data

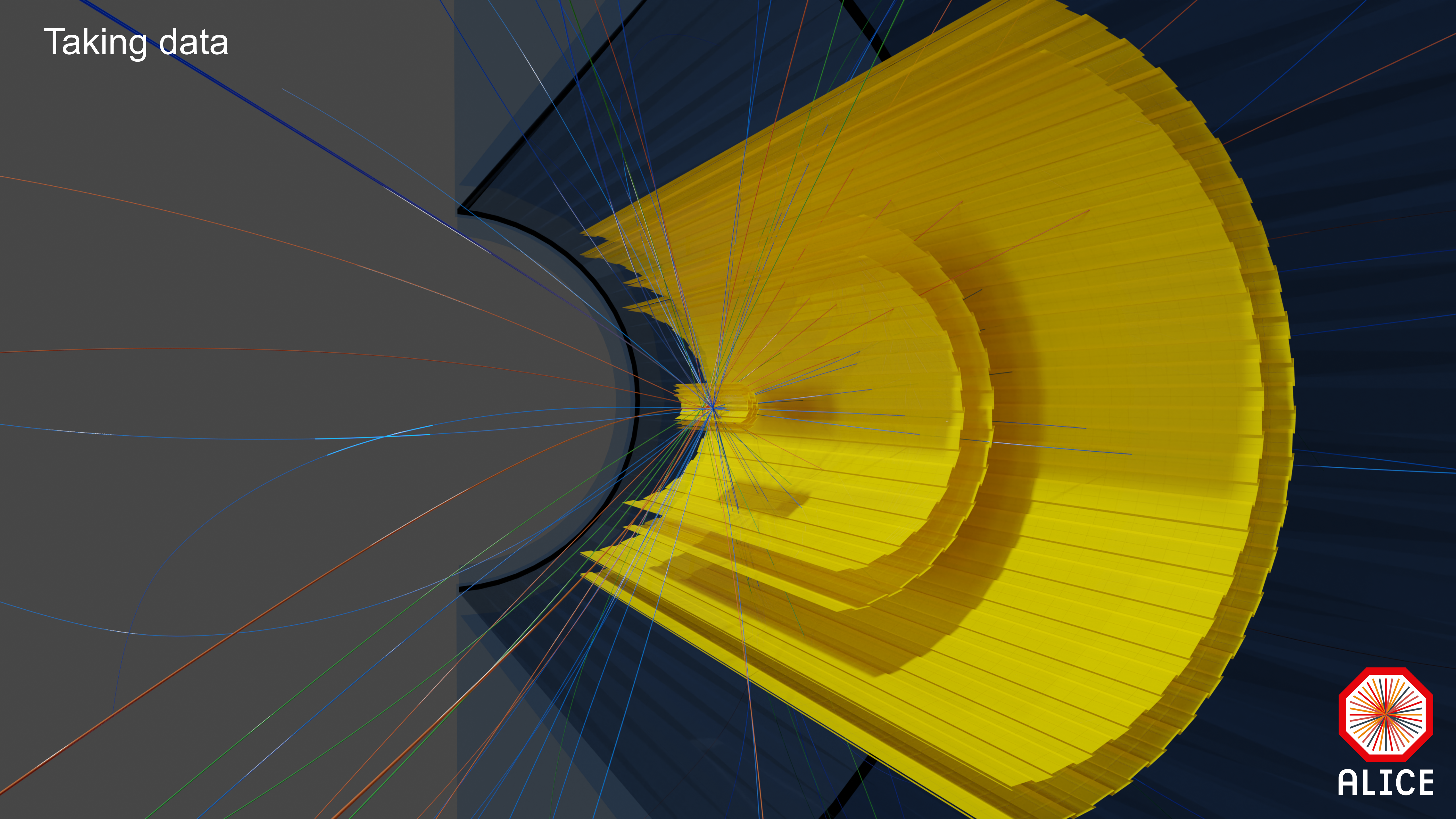


ALICE

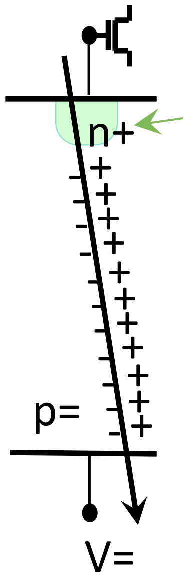
Pb-Pb 5.36 TeV

LHC22s period
18th November 2022
16:52:47.893

Taking data



The need for sensor optimization to obtain full depletion

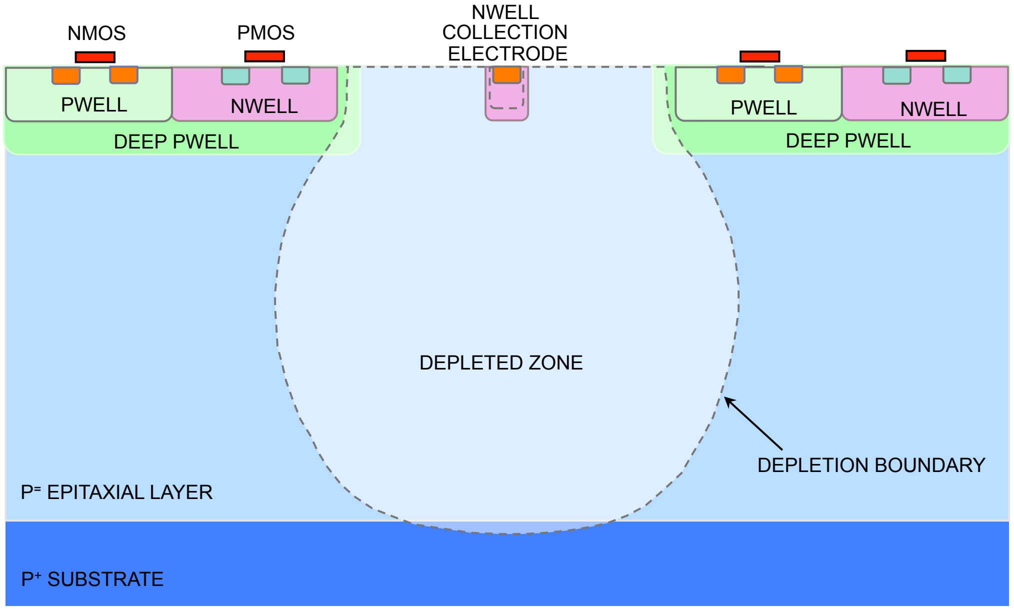


$$C_{spherical} = \frac{4\pi\varepsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\varepsilon R_1$$

Add connection & circuit

Planar junction
Depletion width $= \sqrt{\frac{2\varepsilon|V|}{qN_A}}$

Spherical junction
Outer depletion radius $= \sqrt[3]{\frac{2\varepsilon|V|}{qN_A}\frac{3R_1}{2}}$

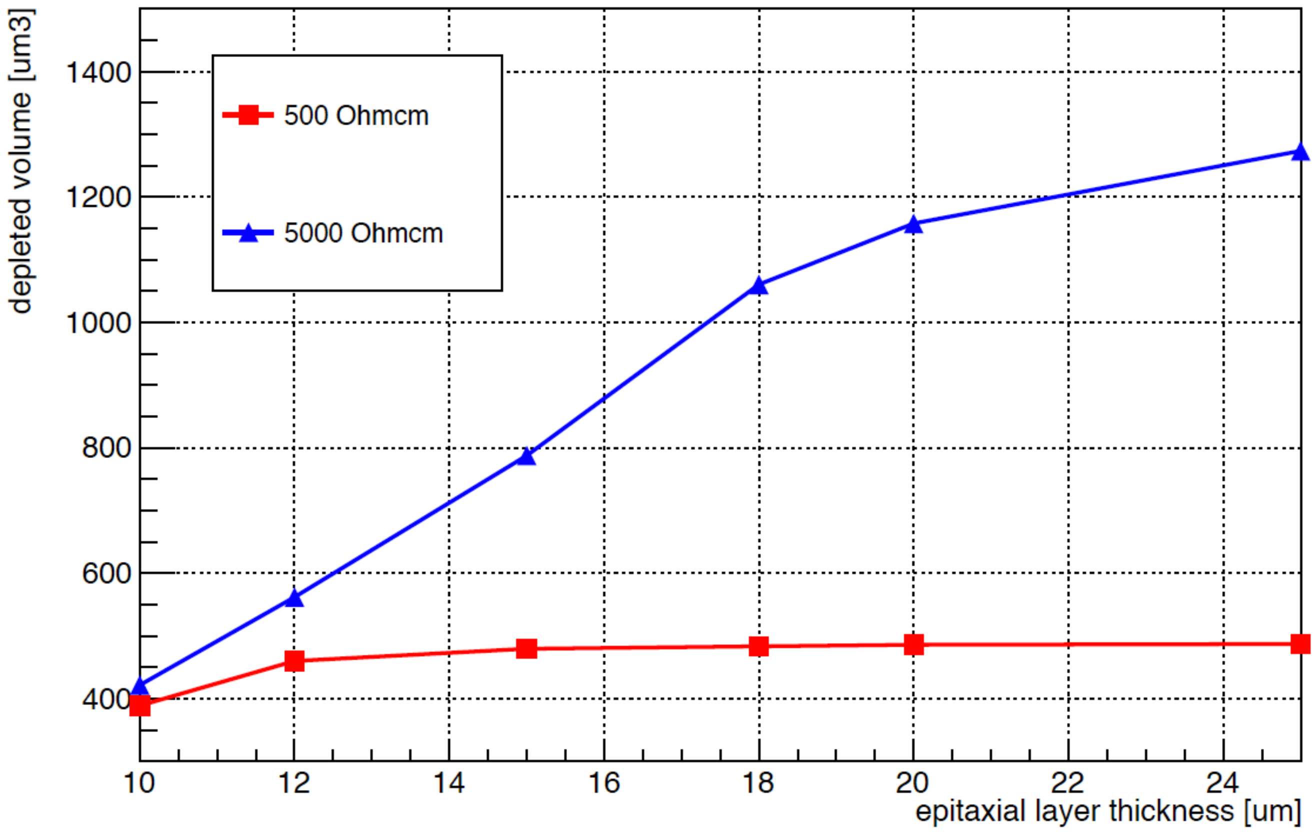


Signal charge is collected from the non-depleted layer, diffusion dominated and prone to trapping after irradiation

Planar vs spherical junction

- Planar junction: depletion thickness proportional to *square root* of reverse bias.
- Spherical junction : depletion thickness proportional only to *cubic root* of reverse bias, inner radius R1 to be kept small for low capacitance
- Deep pwell and substrate limit extension of the depletion layer -> see next slide

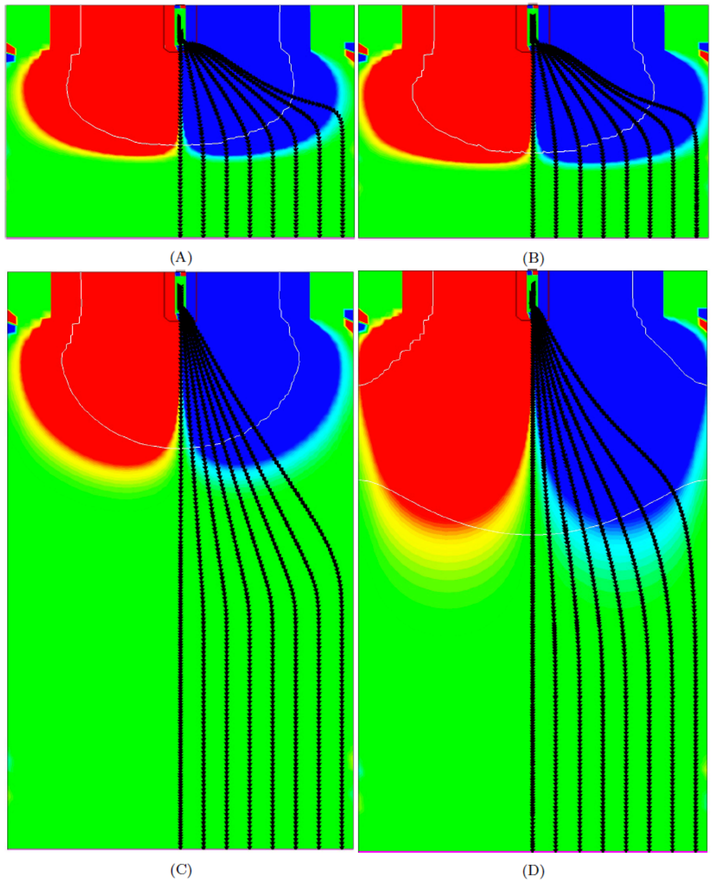
Sensor optimization: influence of the resistivity of the epitaxial layer



Lateral electric field

thin epitaxial layer

thick epitaxial layer



low resistivity

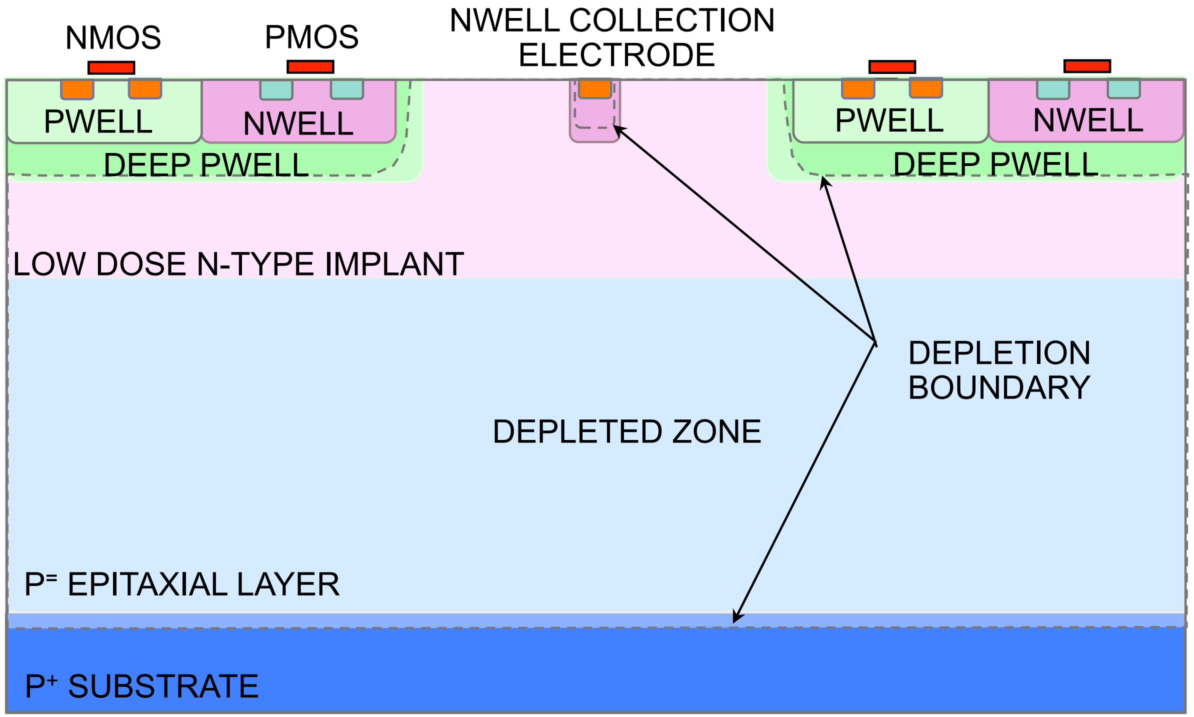
high resistivity

For thinner epitaxial layers, higher resistivity does not help for further depletion due to the proximity of the substrate

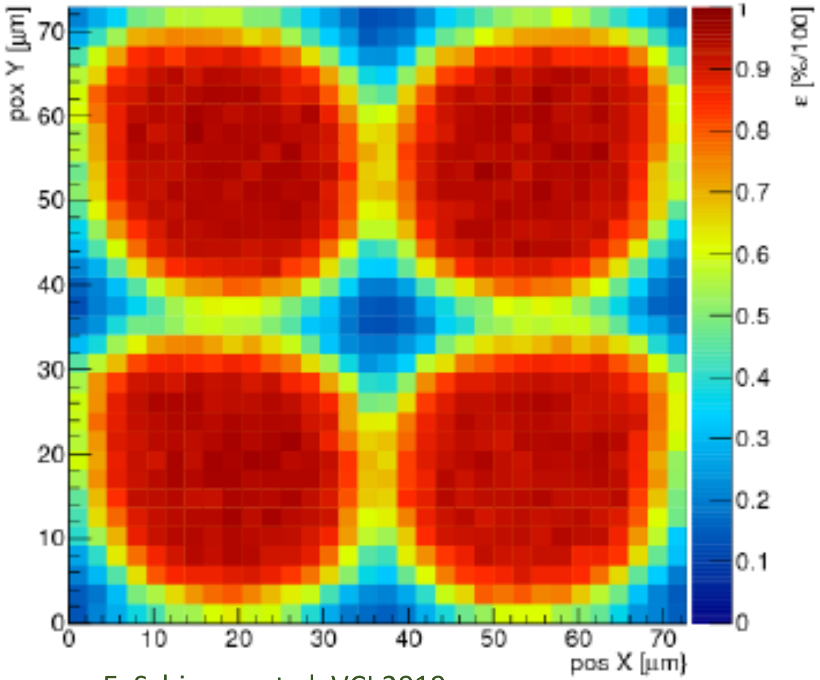
Depletion constrained by the substrate and surrounding pwells

Sensor optimization: create planar junction using deep low dose n-type implant

TowerJazz 180nm imaging CMOS technology



https://doi.org/10.1016/j.nima.2017.07.046 (180nm)

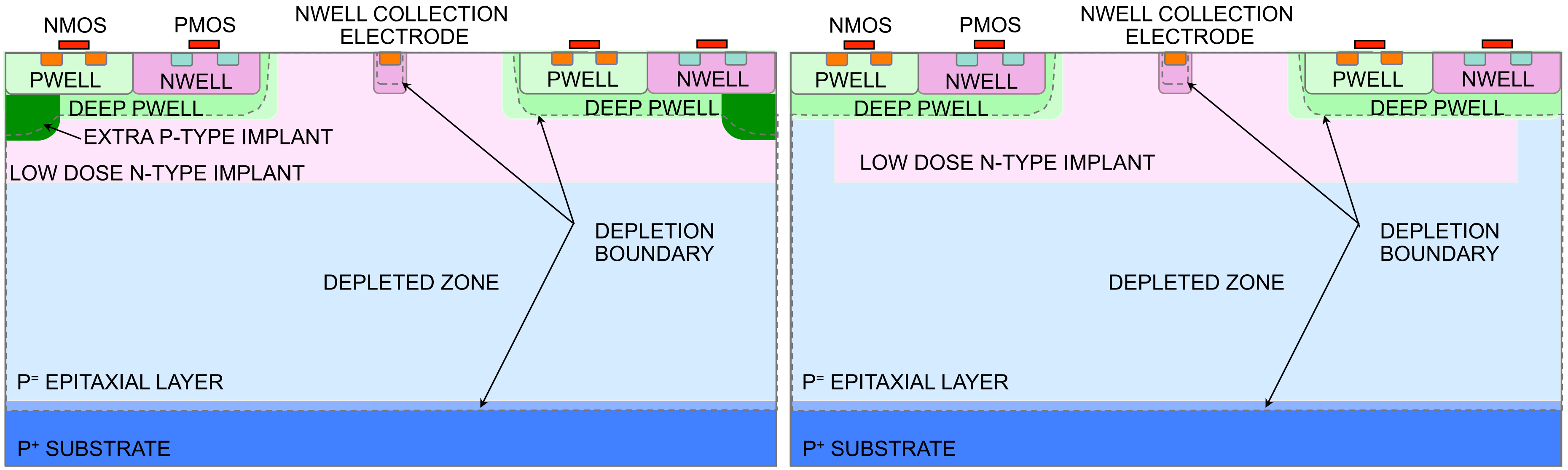


E. Schioppa et al, VCI 2019

- Side development in ALICE: move junction away from the collection electrode to create a planar junction and deplete the epitaxial layer
  - add deep low dose n-type implant -> radiation tolerance improved by an order of magnitude.
- After interest from ATLAS: MALTA/TJ MONOPIX development (Bonn, CPPM, IRFU and CERN)
- However, efficiency loss at ~ 10^{15} 1 MeV n_{eq}/cm^2 on the pixel edges and corners due to a too weak lateral field

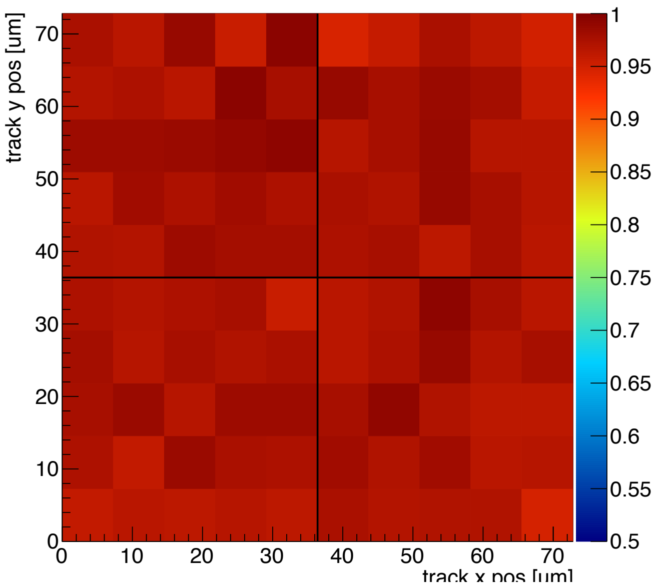
Sensor optimization: improvement of the lateral field

TowerJazz 180 nm imaging CMOS technology



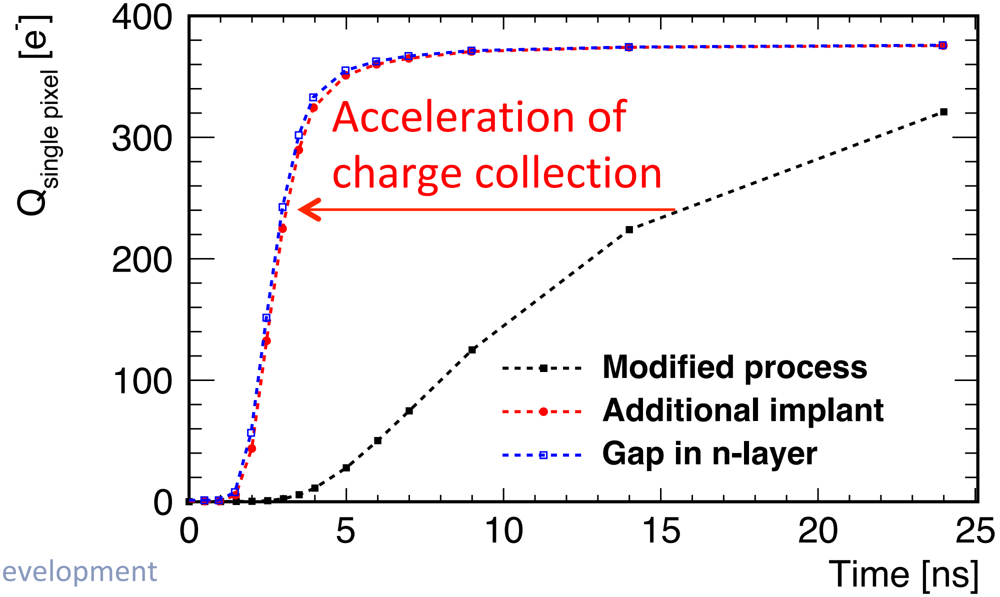
3D TCAD simulation M. Munker et al. PIXEL2018 https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

miniMalta in pixel efficiency, sector 1



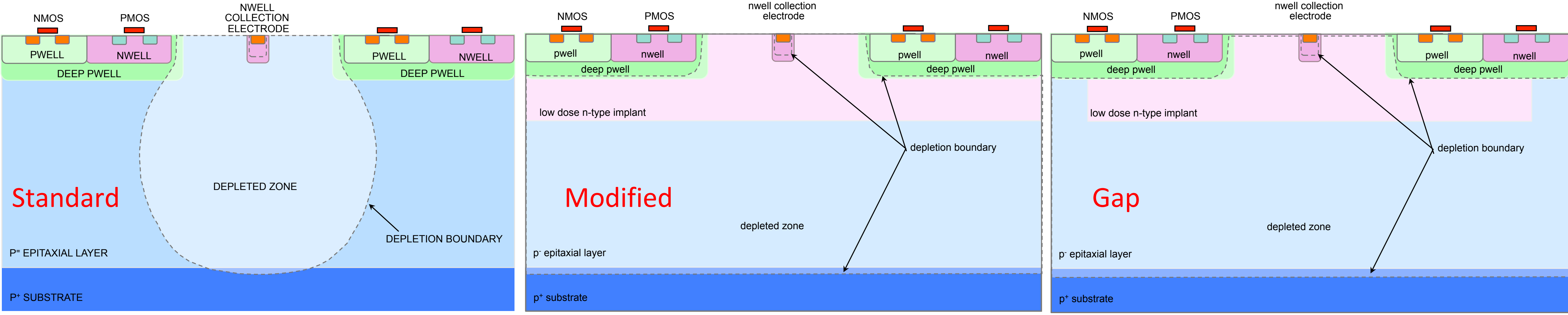
Additional deep p-type implant or gap in the low dose n-type implant improves lateral field near the pixel boundary and accelerates the signal charge to the collection electrode. This yields:

- Full detection efficiency at 10^{15} n_{eq}/cm^2
  H. Pernegger et al., Hiroshima 2019, M. Dyndal *et al* 2020 *JINST* **15** P0200
- more operating margin even before irradiation
- better sensor timing



Moving to 65 nm: apply same principles as in 180 nm

- Process optimization: more needed/beneficial in 65 nm due to a thinner epitaxial layer
  - Add and adjust the deep n-well implant in the pixel to obtain easier depletion
  - Adjust the deep p-well implant to improve the isolation between the circuit and the sensor, prevent punchthrough between deep n-type implant and circuitry, and prevent local potential wells retaining the signal charge.
- 4 process splits, 3 wafers each: moving gradually from default to optimized process
  - **Split 1: default process**
  - Split 2: **first deep pwell adjustment to prevent punchthrough**
  - Split 3: first deep pwell adjustment + **deep nwell adjustment**
  - **Split 4: optimized process:** first deep pwell adjustment + deep nwell adjustment + **second deep pwell adjustment against local potential wells**
- 3 main pixel designs implemented in all process splits



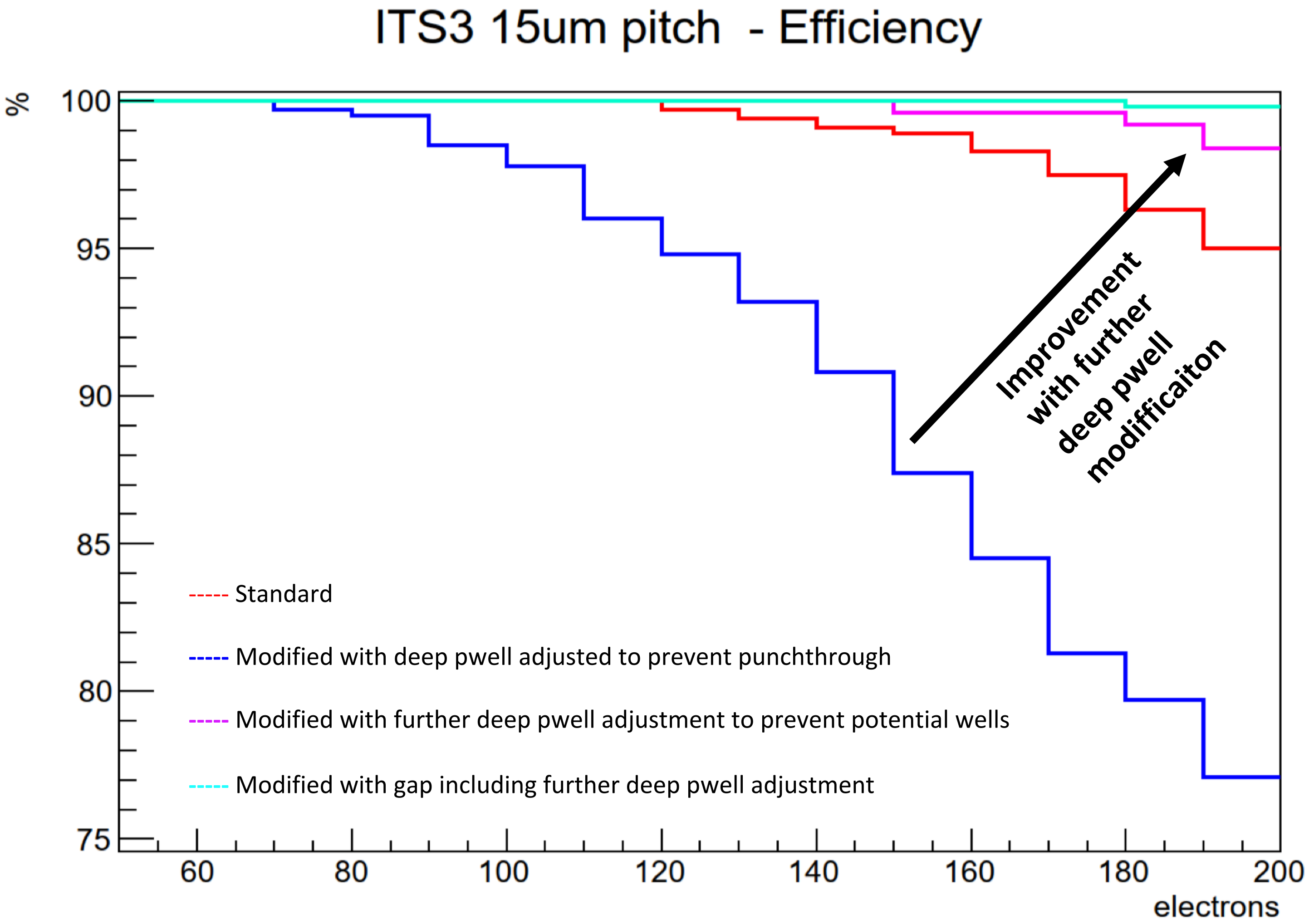
https://doi.org/10.1016/j.nima.2017.07.046 (180nm)

https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed →

← Charge sharing

Sensor optimization:
Mitigate local potential wells related to the in-pixel circuitry

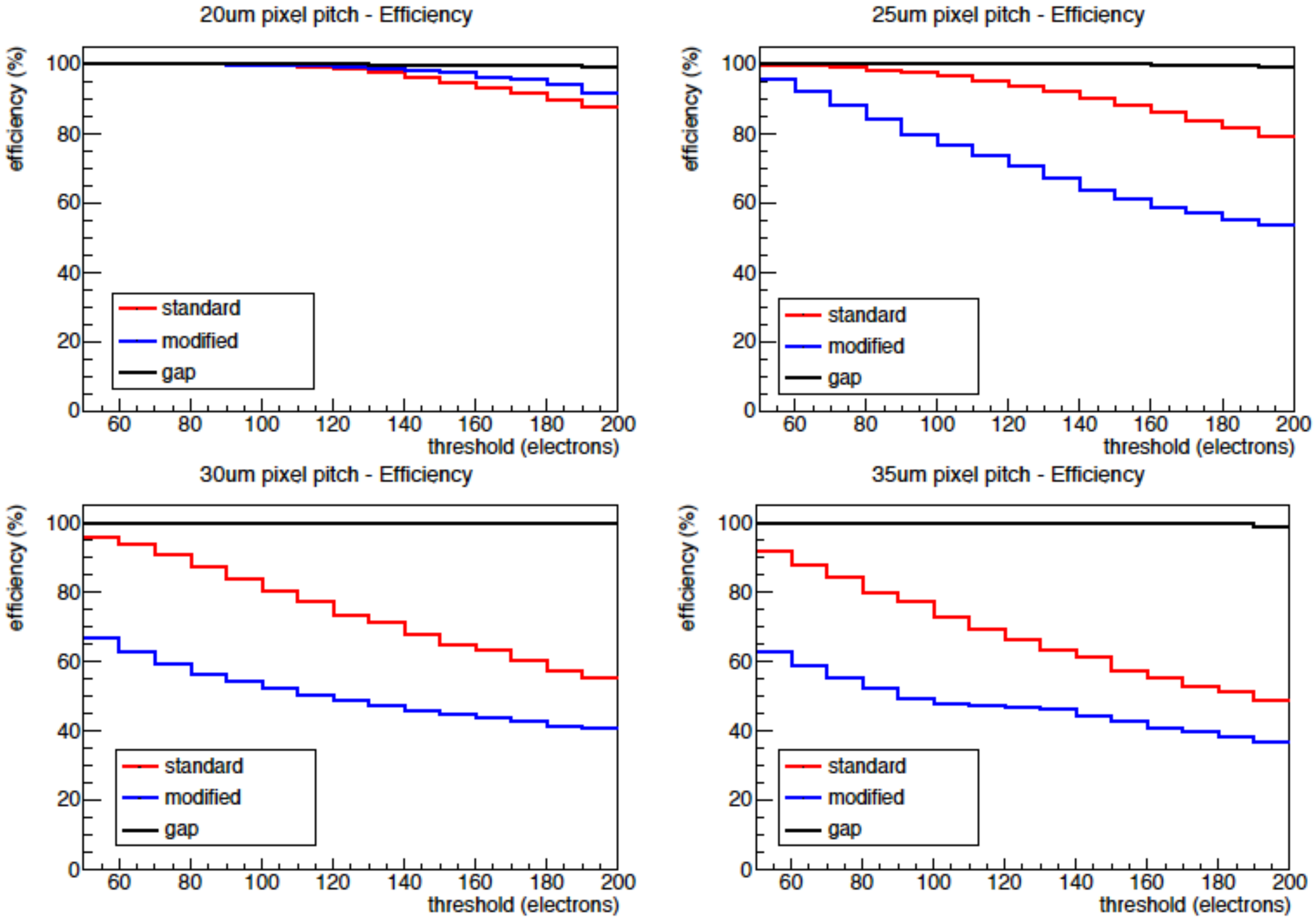


Simulation for MIPS:

Increasing the margin for punchthrough was not sufficient to eliminate potential wells under the deep pwell.

Lower lateral field for the modified version without gap enhances the effect of these potential wells and illustrates best the improvement

Different pixel flavors at larger pixel pitches



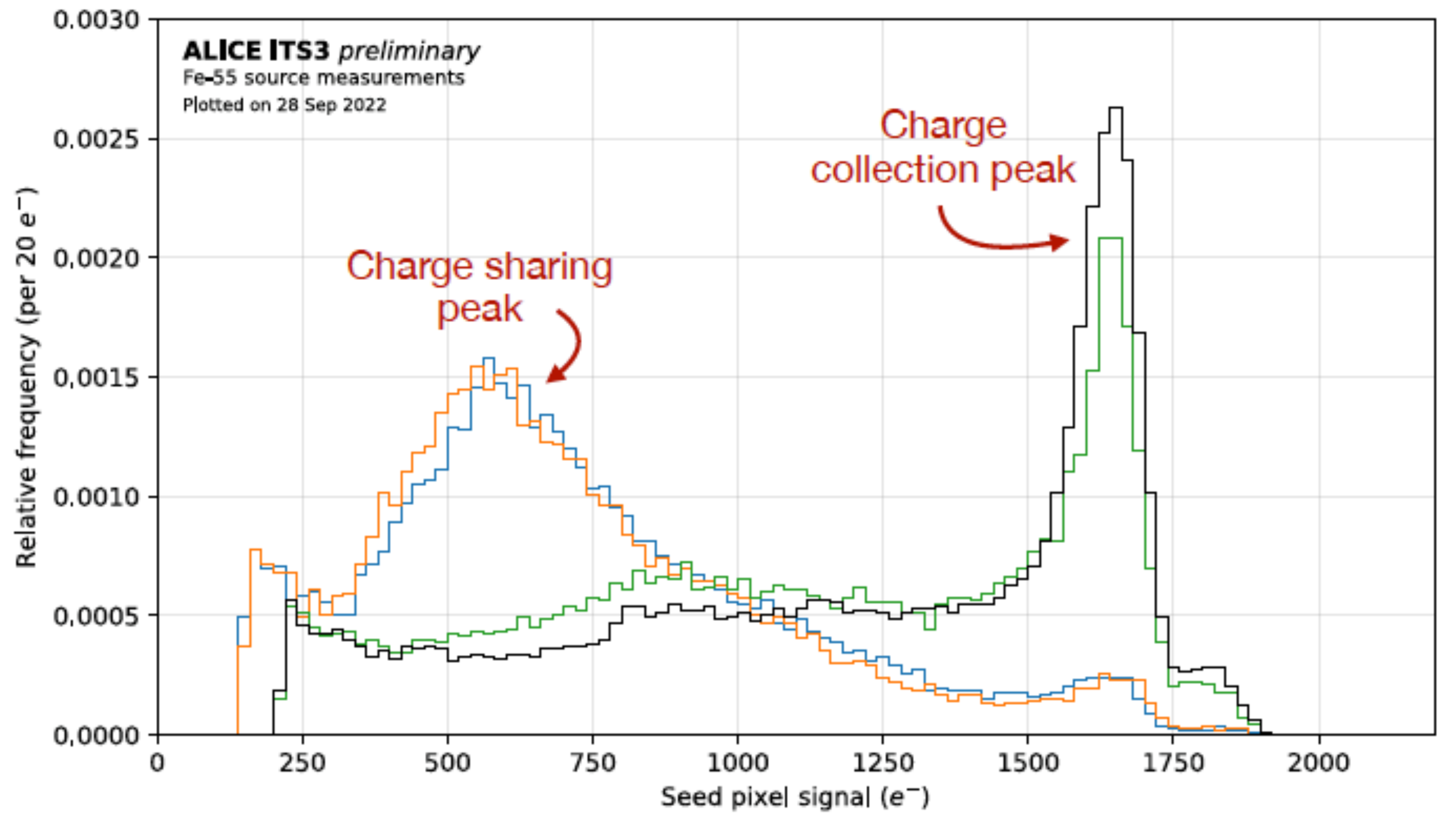
Simulations by J. Hasenbichler for MIPS

Charge sharing reduces the signal in a single pixel and reduces efficiency especially for larger thresholds.

Only the gap concentrates charge sufficiently to remain efficient for large pixel pitches

^{55}Fe measurements confirm influence on charge sharing

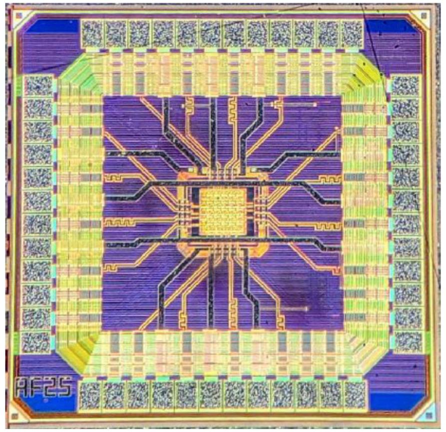
See also: I. Sanna IEEE NSS 2022



APTS SF
pitch: 15 µm
$V_{sub} = V_{pwell} = -1.2\,\mathrm{V}$
$I_{reset} = 100\,\mathrm{pA}$
$I_{biasn} = 5\,\mu\mathrm{A}$
$I_{biasp} = 0.5\,\mu\mathrm{A}$
$I_{bias4} = 150\,\mu\mathrm{A}$
$I_{bias3} = 200\,\mu\mathrm{A}$
$V_{reset} = 500\,\mathrm{mV}$

- 🟦 split 1, standard type
- 🟧 split 4, standard type
- 🟩 split 4, modified type
- ⬛ split 4, modified with gap type

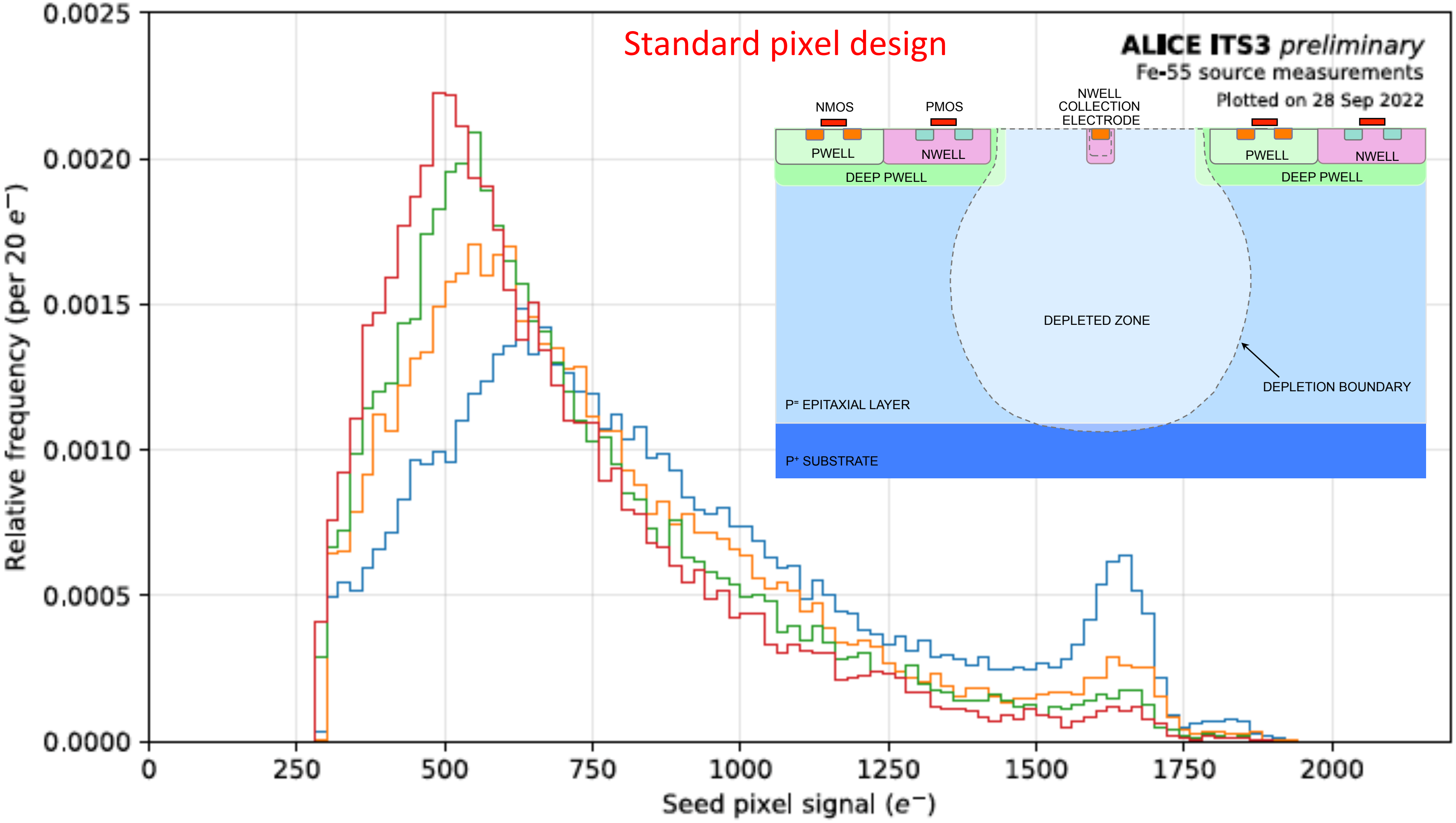
APTS SF



No experimental comparison between split 3 and split 4 available yet.

Pitch dependence for different variants

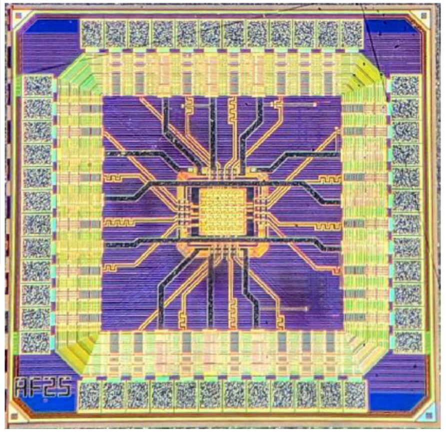
See also: I. Sanna IEEE NSS 2022



APTS SF
type: standard
split: 4
$V_{sub} = V_{pwell} = -1{,}2\,\mathrm{V}$
$I_{reset} = 100\,\mathrm{pA}$
$I_{biasn} = 5\,\mu\mathrm{A}$
$I_{biasp} = 0{,}5\,\mu\mathrm{A}$
$I_{bias4} = 150\,\mu\mathrm{A}$
$I_{bias3} = 200\,\mu\mathrm{A}$
$V_{reset} = 500\,\mathrm{mV}$

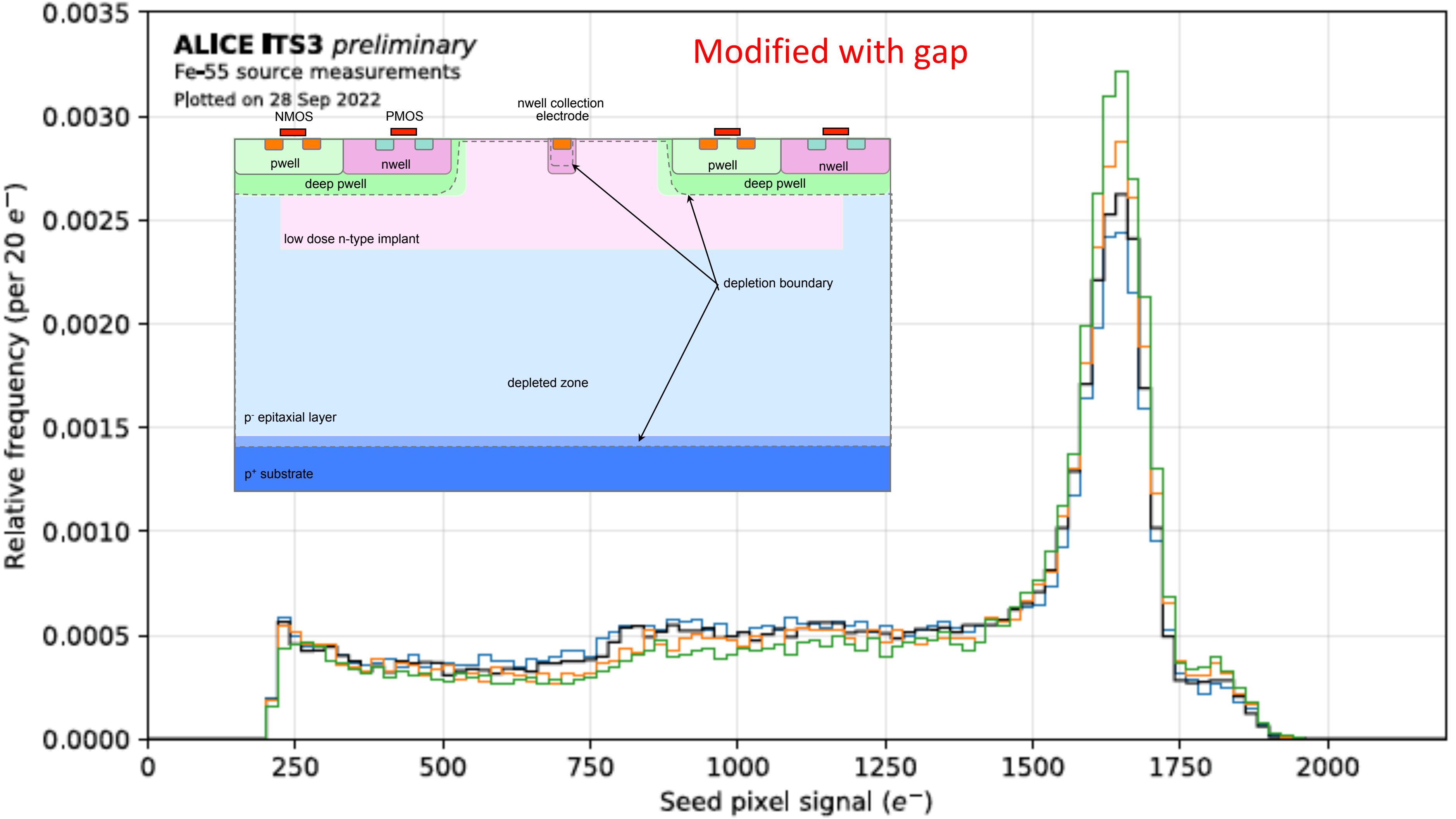
🟦 pitch = 10 µm
🟧 pitch = 15 µm
🟩 pitch = 20 µm
🟥 pitch = 25 µm

APTS SF



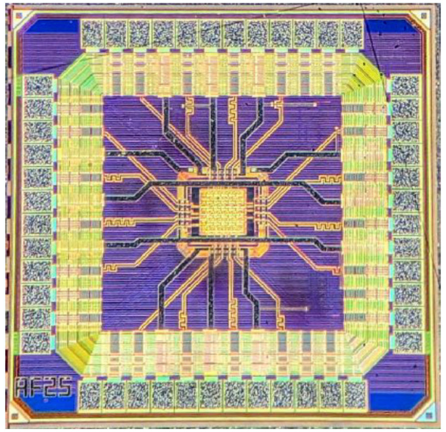
Pitch dependence for different variants

See also: I. Sanna IEEE NSS 2022

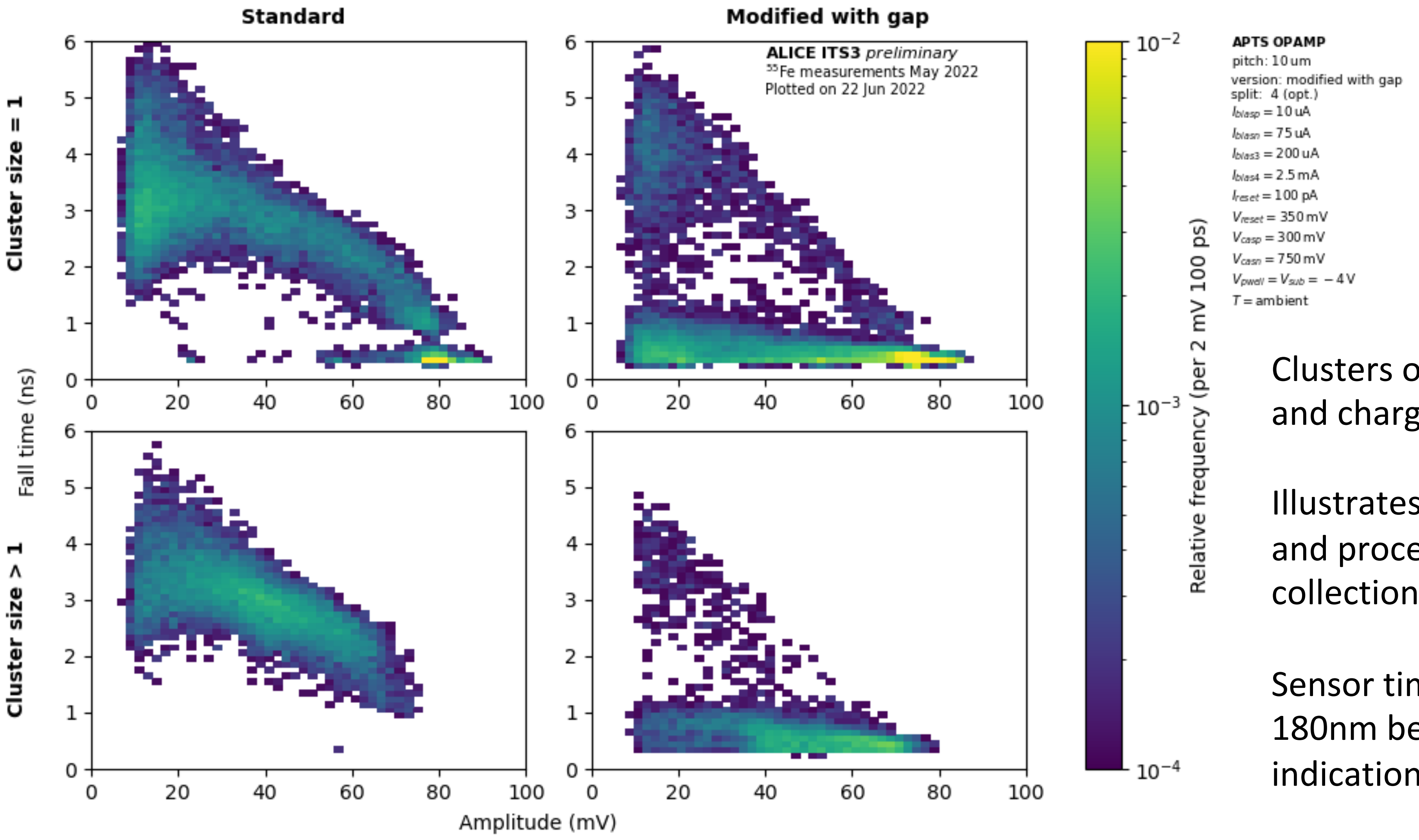


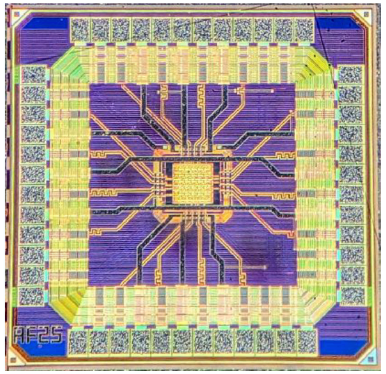
APTS SF
type: modified with gap
split: 4
$V_{sub} = V_{pwell} = -1.2\,V$
$I_{reset} = 100\,pA$
$I_{biasn} = 5\,\mu A$
$I_{biasp} = 0.5\,\mu A$
$I_{bias4} = 150\,\mu A$
$I_{bias3} = 200\,\mu A$
$V_{reset} = 500\,mV$

APTS SF



^{55}Fe measurements on Analog Pixel Test Structure Opamp





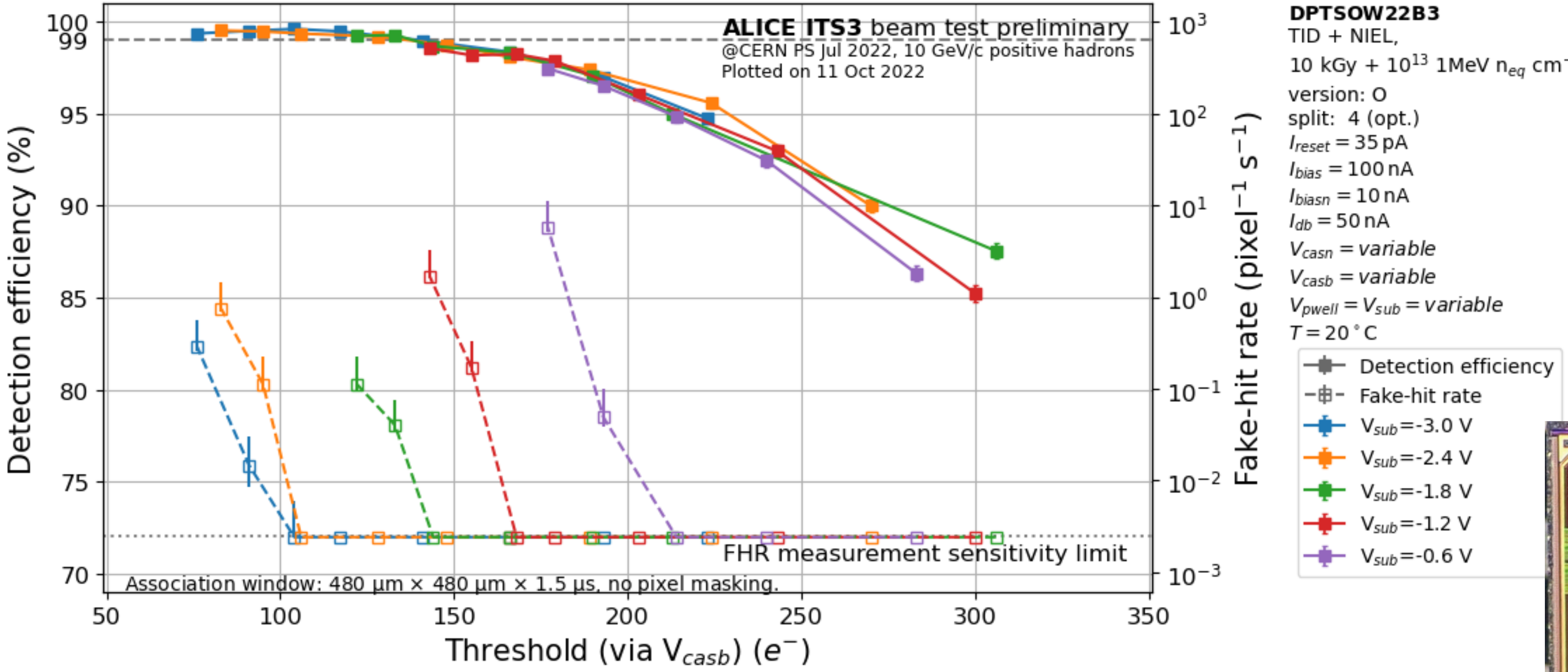
Clusters of various sizes show distinct time and charge distributions

Illustrates the impact of the pixel design and process modifications on the charge collection

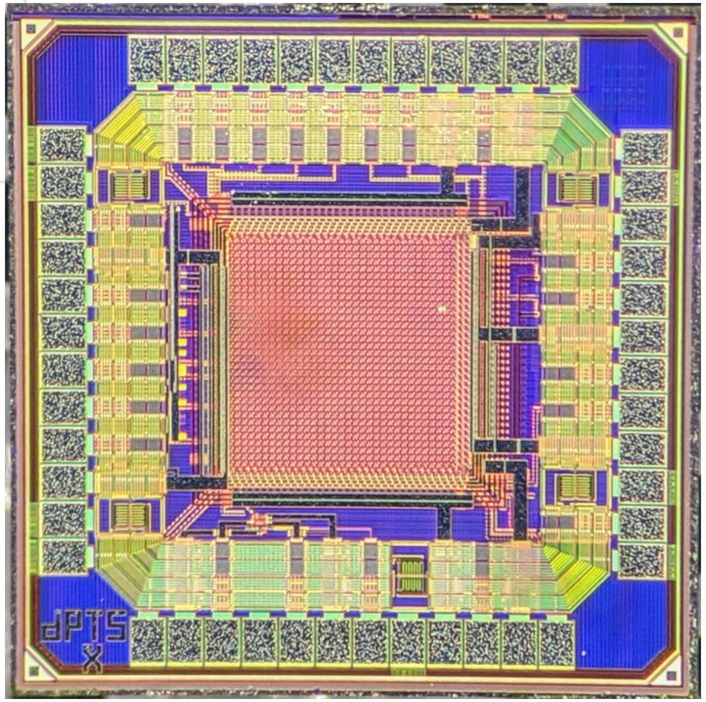
Sensor timing is at present under study, in 180nm better than 150 ps*, first indications this may improve in 65 nm.

*Fastpix :https://www.mdpi.com/2410-390X/6/1/13
J. Braach, E. Buschmann, D. Dannheim et al.

Detection efficiency/Fake hits



DPTS

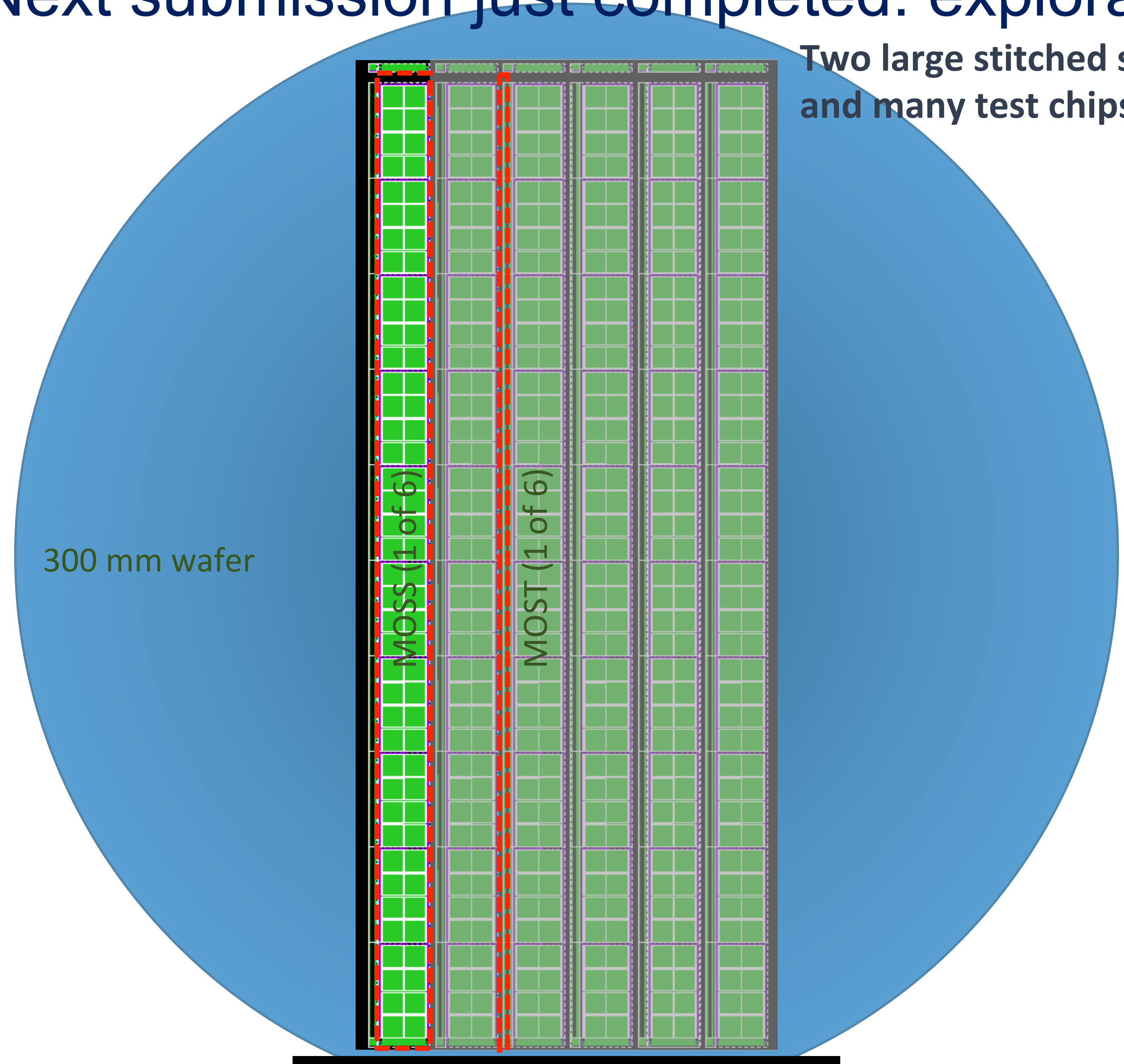


- Fully efficient sensor, analog front end, digital readout chain in 15 x 15 µm^2 pixel (DPTS) including sensor optimization
- Large operating margin before irradiation
- After 1E15 n_{eq}/cm^2 efficiency > 99% maintained at room temperature
- Higher fluencies under investigation

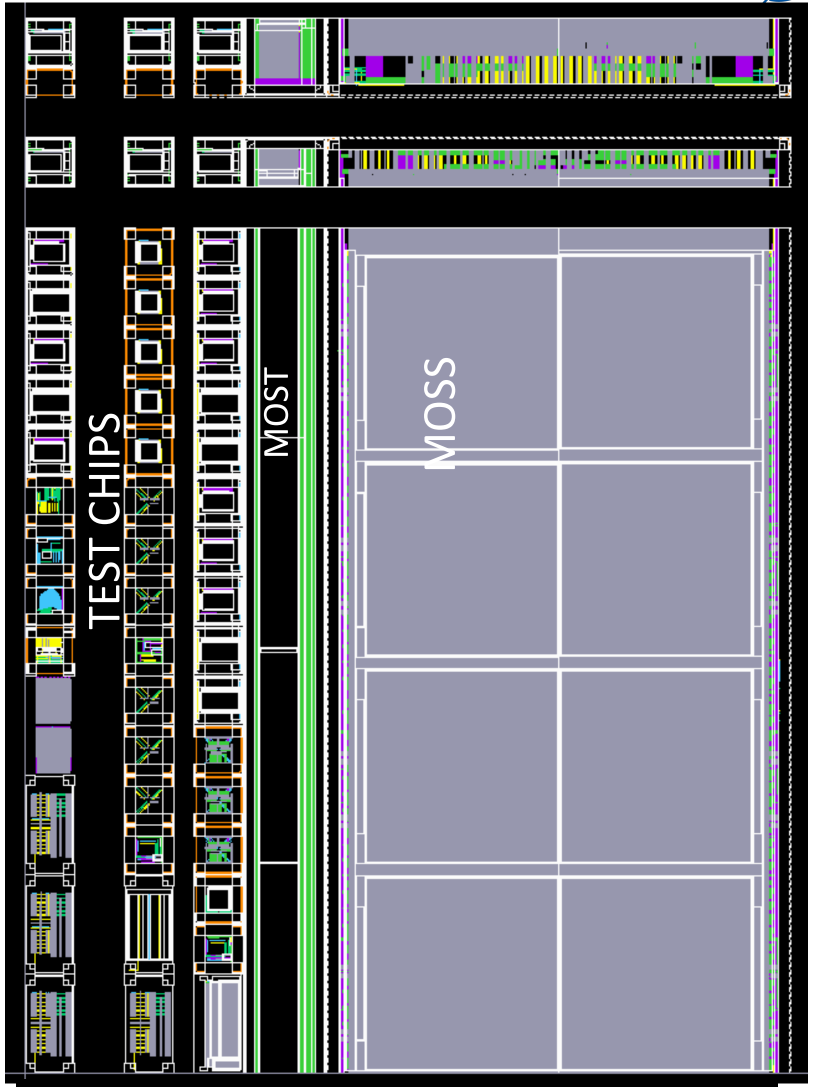
(see also Lukas Lautner's presentation)

Next submission just completed: exploration of large stitched sensors

Two large stitched sensors (MOSS and MOST) and many test chips



6 MOSS and 6 MOST per Wafer



51 instances of Test Chips per Reticle

MOSS : see Geun Hee Hong's presentation

SUMMARY AND OUTLOOK

First technology selected in WP1.2 is the TPSCo 65 nm CMOS imaging technology

- Fully efficient optimized sensor, analog front end, digital readout chain in 15 x 15 μm^2 pixel (DPTS)
- Sensor optimization following general principles now also proven in 65 nm
- More margin before irradiation, better time resolution and radiation tolerance
- Technology specific special transistors and sensor structures still to be exploited

Radiation effects

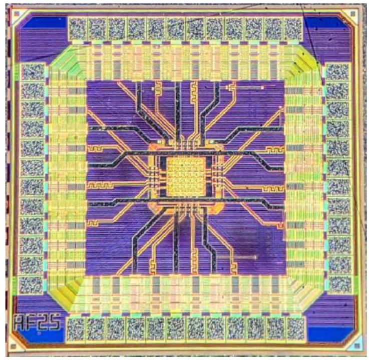
- Circuit radiation tolerance TID in line with other 65 nm technologies*
- Sensor radiation tolerance NIEL:
  - ~ 99% efficiency after 1e15 n_{eq}/cm^2 at room temperature
  - higher fluencies to be investigated, also at lower temperature
- Single event upset cross-section according to expectations

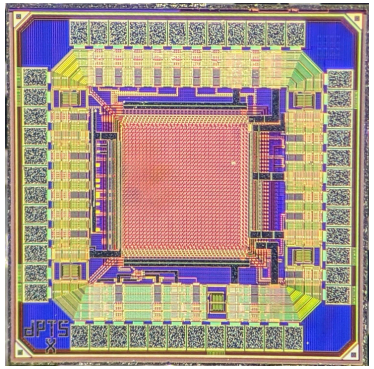
Building knowledge about this technology for general interest

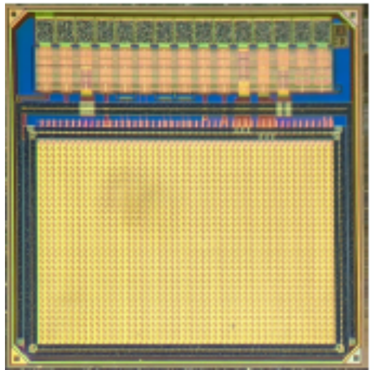
- Very significant contribution from the ALICE experiment
- Towards full technology validation for our applications

Next submission Stitched Engineering Run ER1

- Learning about stitching and continue learning about the technology


APTS


DPTS


CE65

(see J. Baudot's presentation)

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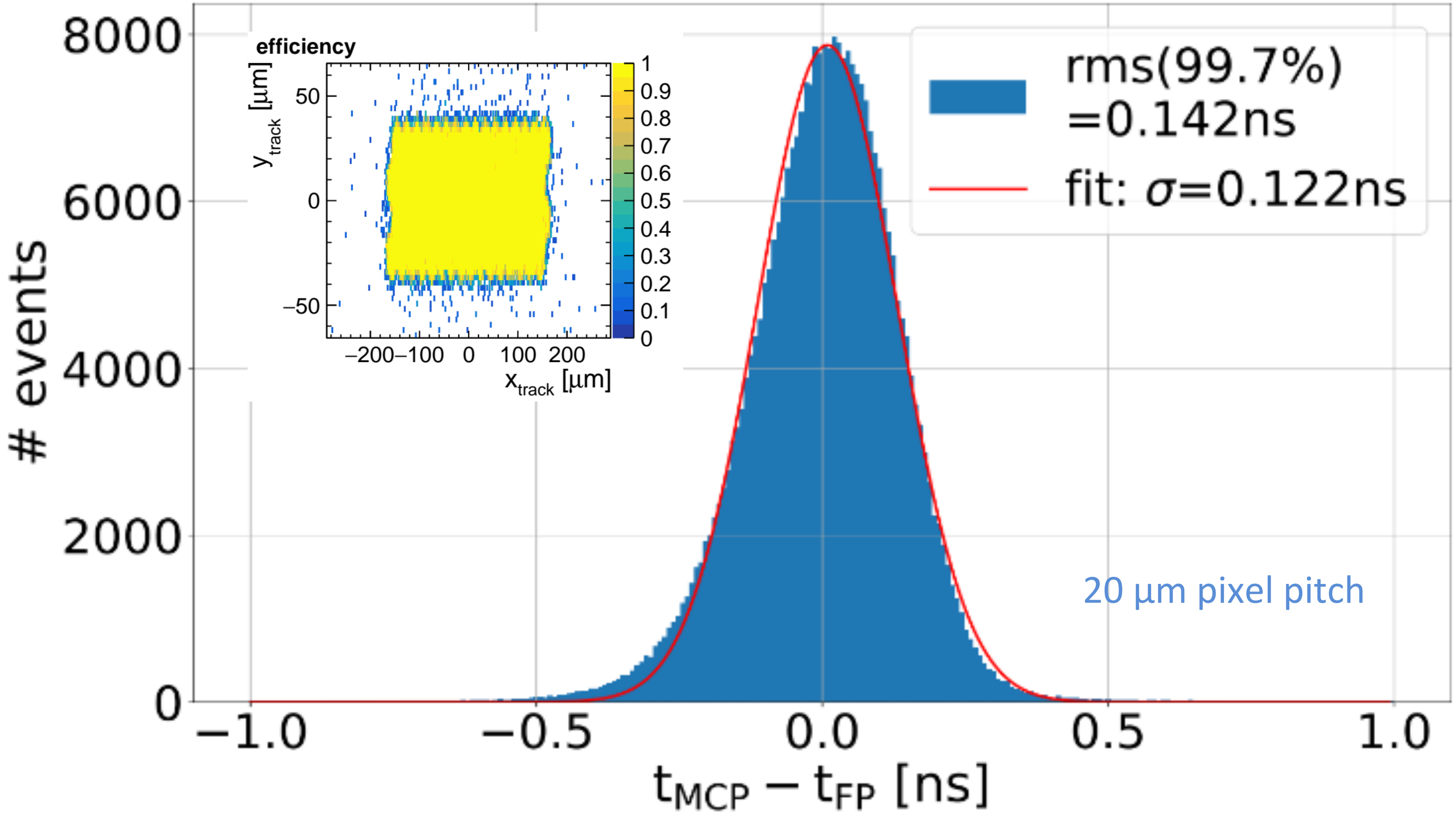
*P. Barrillon et al, A. Dorda et al. Twepp 2022

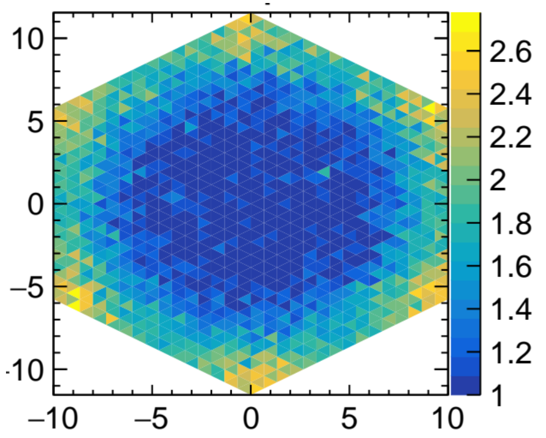
THANK YOU TO ALL CONTRIBUTING PEOPLE, GROUPS AND INSITUTES

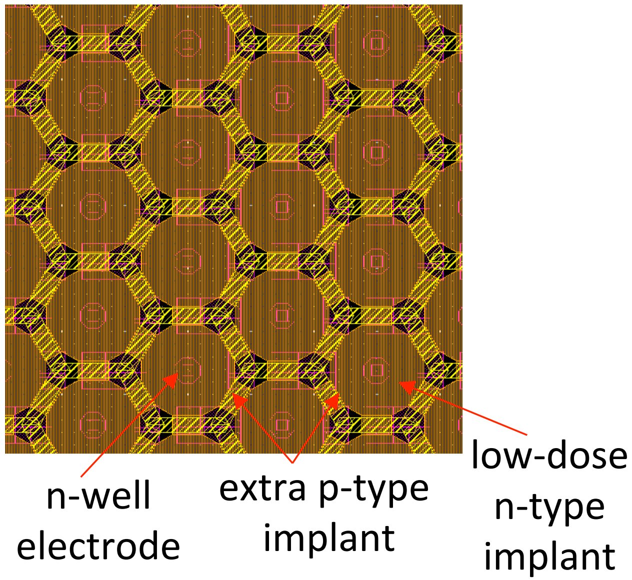
SPARE

FASTPIX: sensor optimization for hexagonal pixels



Cluster size





- 8.66, 10, 15 and 20 µm pixel pitch
- Time resolution better than 150 ps at full efficiency, TOT corrected

https://www.mdpi.com/2410-390X/6/1/13

J. Braach, E. Buschmann, D. Dannheim, K. Dort, T. Kugathasan, M. Munker, M. Vicente

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