Serial Powering for ATLAS ITk Pixel Modules

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For the ATLAS ITk Collaboration
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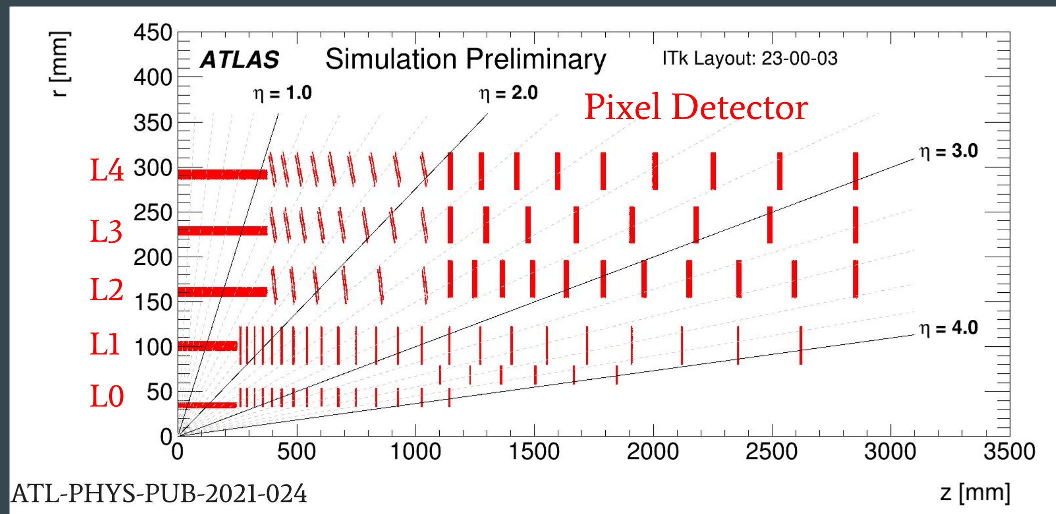
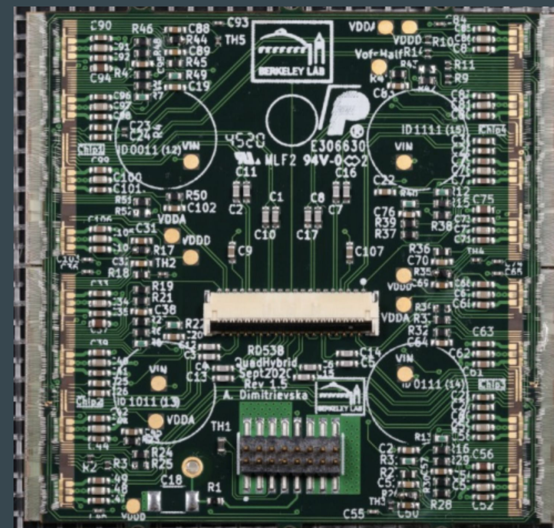
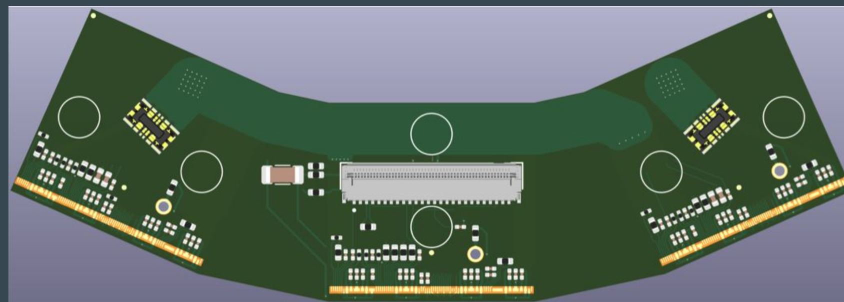
ATLAS ITk pixel modules



Pre-production (ITkPixV1) quad module



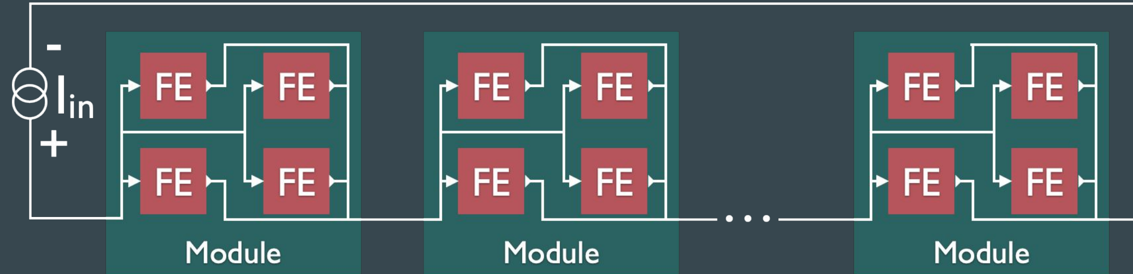
Pre-production (ITkPixV1) R0.5 triplet hybrid



- ATLAS ITk pixel detector contains 8372 modules
  - 396 triplets (3 FE chips) used for L0
  - 7976 quad modules (4 FE chips) used for L1~L4

See Craig Buttar's talk about ATLAS pixel upgrade
Dimitris Varouchas' talk about ATLAS pixel module

Module Serial Powering



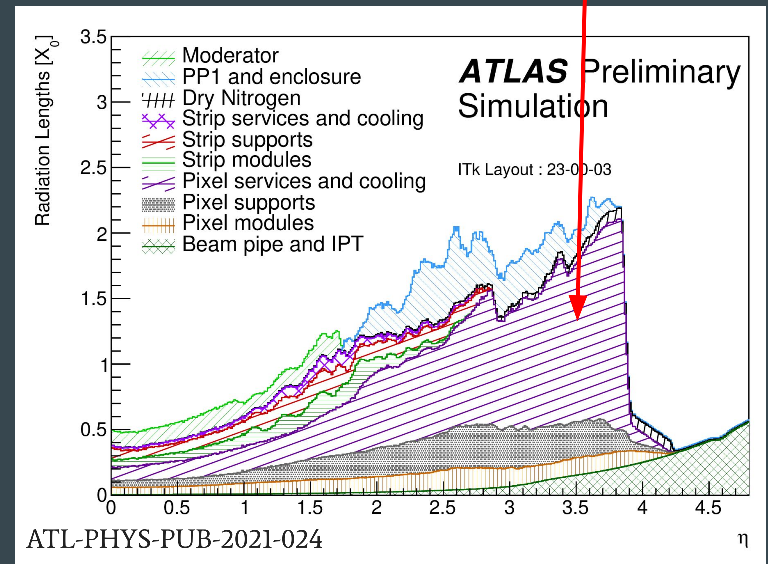
Mass dominated by pixel services (e.g. cables)

Large volume of powering cable materials affects detector performance

Novel power scheme: groups of modules powered in series to reduce cable materials!

Requirements/challenges:

- Constant-current power supply with load regulation
- Over-voltage protection
- Over-current protection
- Fault condition handling (response to chip faults!)



ITkPixV1.1 chips

ITkPixV1.1 chip is the preproduction ATLAS ITk pixel FE chip designed by RD53 collaboration

Turn the serial powering from an R&D activity into a “professional grade” powering technology!

- Shunt-LDO operation: the combination of low dropout regulators (LDO) and shunt circuits gives ohmic behavior and allows for constant current operation
- Over-voltage and over-current (under-shunt) protection provide good response to chip faults
- Low power mode allows non-standard operation during testing stage

Novel power scheme with no operational experience: need to build confidence with test setups!

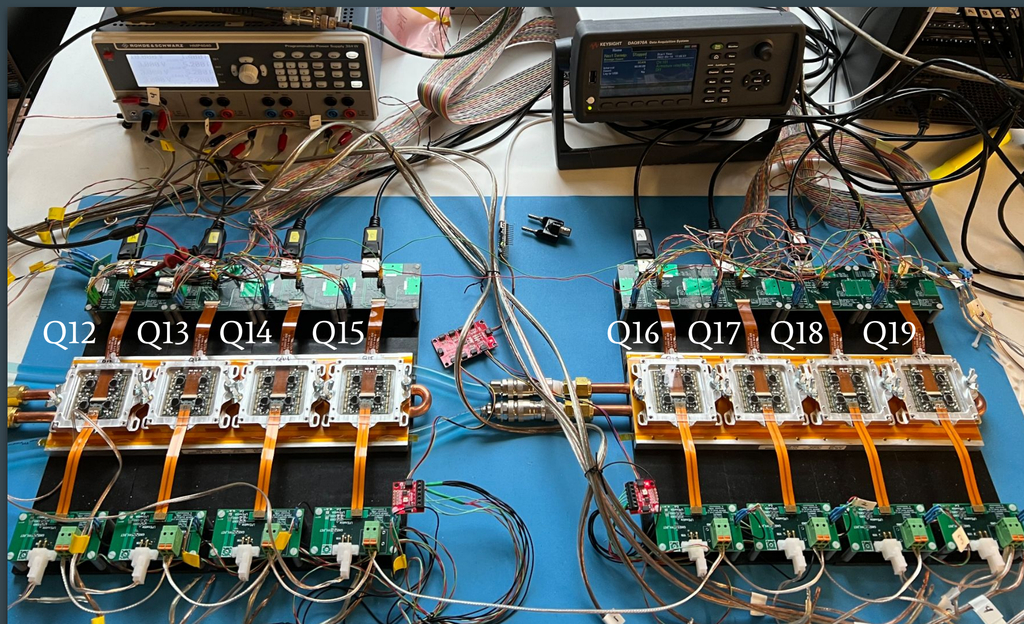
20mm
400 pixels

20.7mm
382 pixels

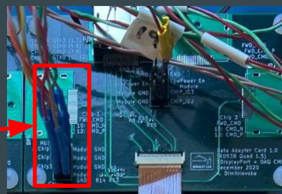
Pre-production (ITkPixV1.1) chip

Serial power testing (@ LBNL)

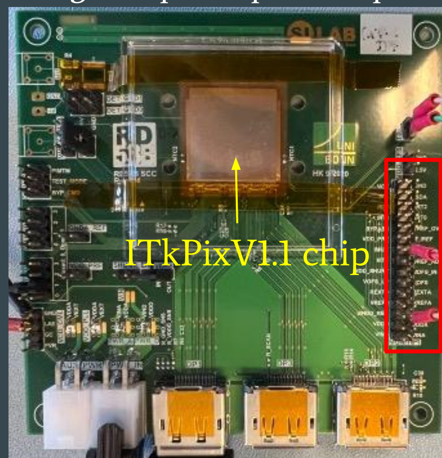
Up to 8 quad modules powered in series with constant current



Internal voltages/currents of quad modules measured through multiplexers routed to the data adaptor card



Single-chip card provides pure chip information



Chip internal voltages/currents measured through probe pins

Extensive electrical tests on pre-production (ITkPixV1.1) modules have been performed to verify that modules work as designed

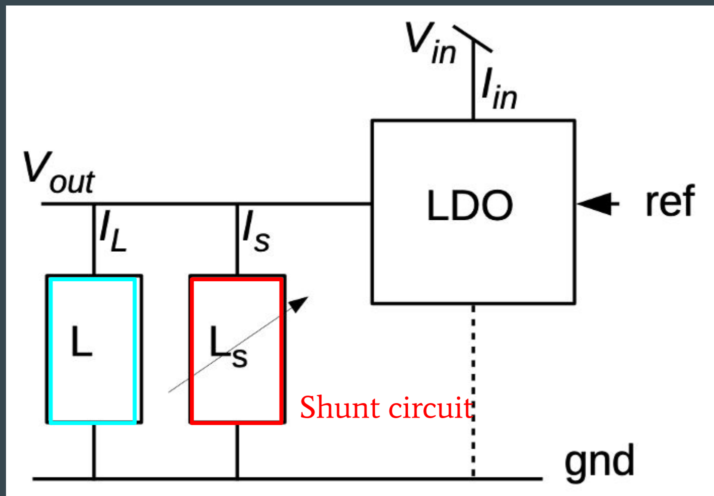
Powering tests highlighted in the following:

- Shunt-LDO voltage-current (VI) test
- Low-power (LP) mode enabling
- Test of under-shunt condition

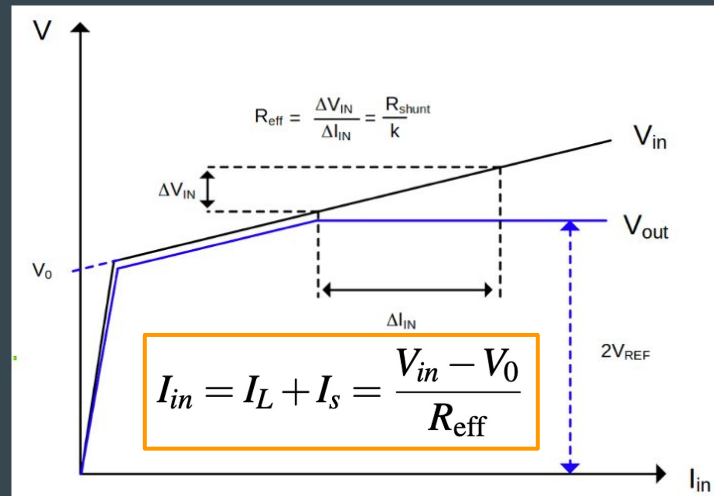
Shunt-LDO VI test

Shunt-LDO VI test

Chip load



Shunt circuit



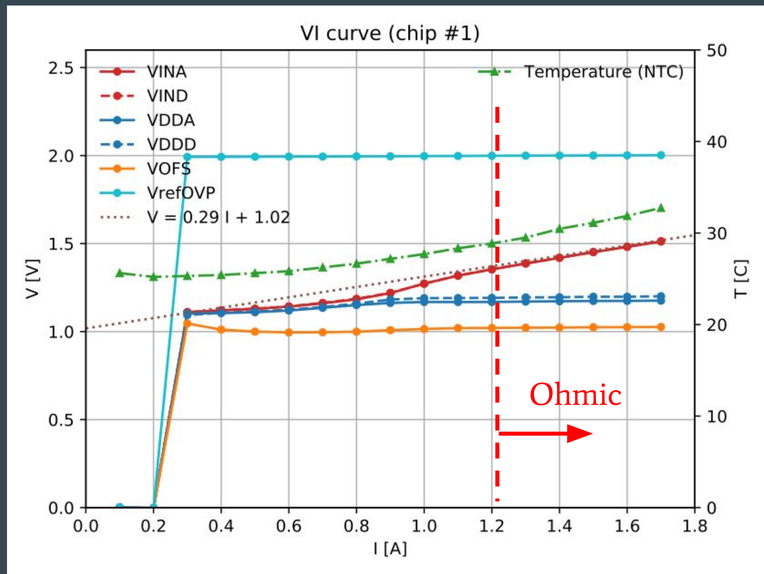
VI tests are crucial to validate the shunt-LDO design

Main goals:

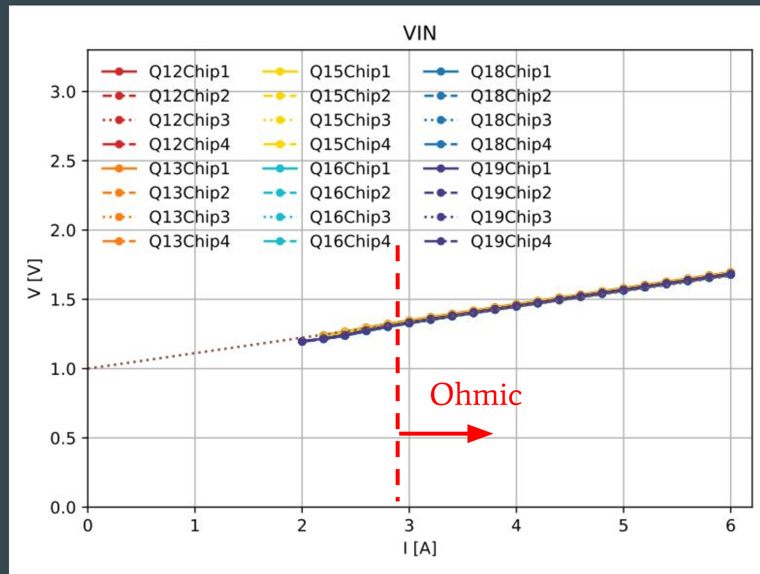
- Verify the ohmic behavior and compare with theory prediction
- Record the minimal operating current ($I_{in} > I_L$) and voltage ($V_{in} > V_{out} + V_{drop\text{-}out}$) for proper shunt-LDO operation

Results of Shunt-LDO VI test

Single-chip card



Serial-power chain



VINA(D) = input voltage for analog (digital) domain
VDDA(D) = V_{out} of analog (digital) domain regulator
VOFS = offset voltage of shunt circuit
VrefOVP = over-voltage protection threshold

Minimal operating current determined by chip configuration (changes chip load current consumption)

Ohmic behavior consistent with theory prediction

Low-power mode enabling

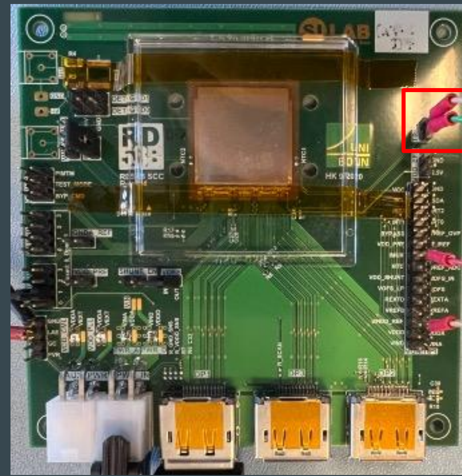
Low power mode

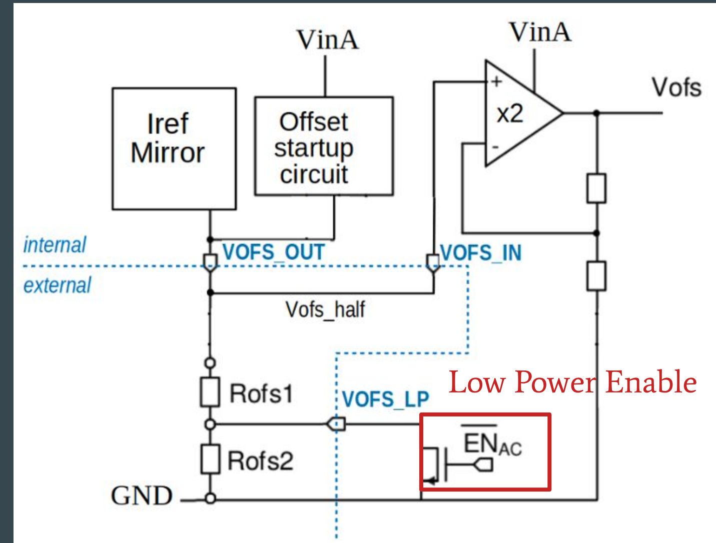
Increase the shunt offset voltage (VOFS) and allow for a smaller current (e.g. 2A) needed to develop a high enough voltage for voltage regulators

Low power operation useful for module testing without a proper cooling system (e.g. during integration to test cable connection)

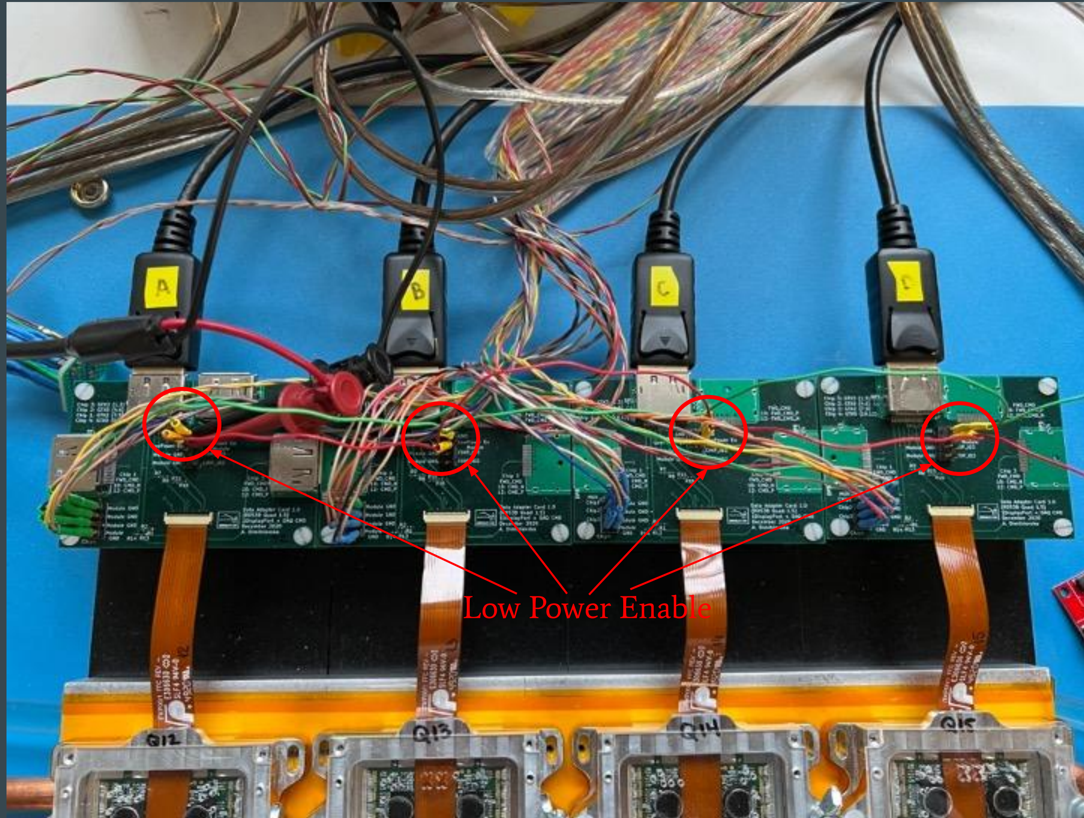
Low power mode can be enabled by injecting an A/C signal

- Square wave: Vpp > 1.2V, f = 80 kHz
- Sine wave: Vpp > 1.2V, f = 130 kHz





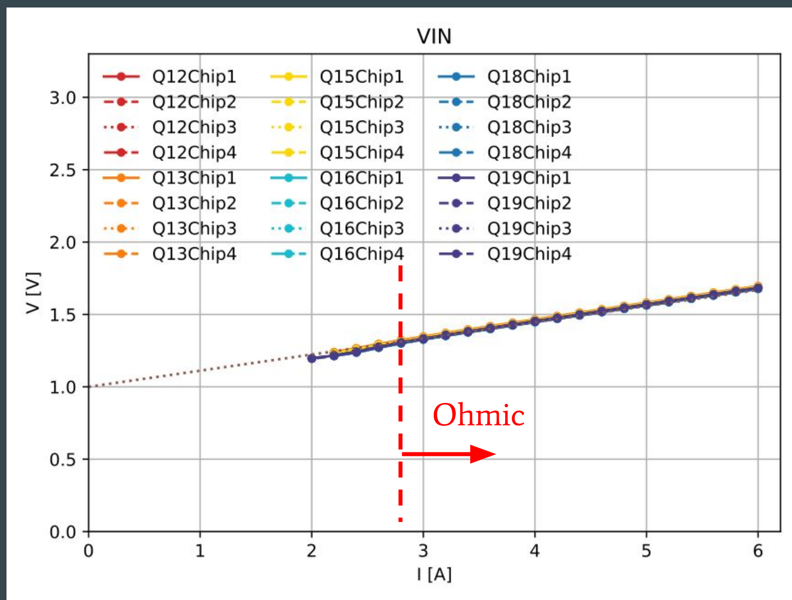
Enable low power mode for the serial power chain



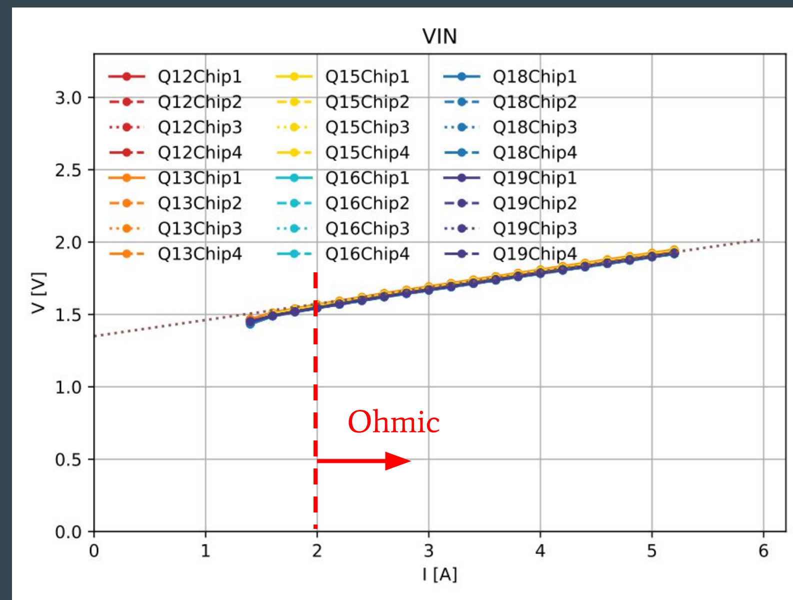
A/C signal can be injected through the data adaptor card to enable the low power mode for a quad module

Enable low power mode for the serial power chain

Normal power mode



Low power mode (inject square wave Vpp=1.2V, f=80kHz)



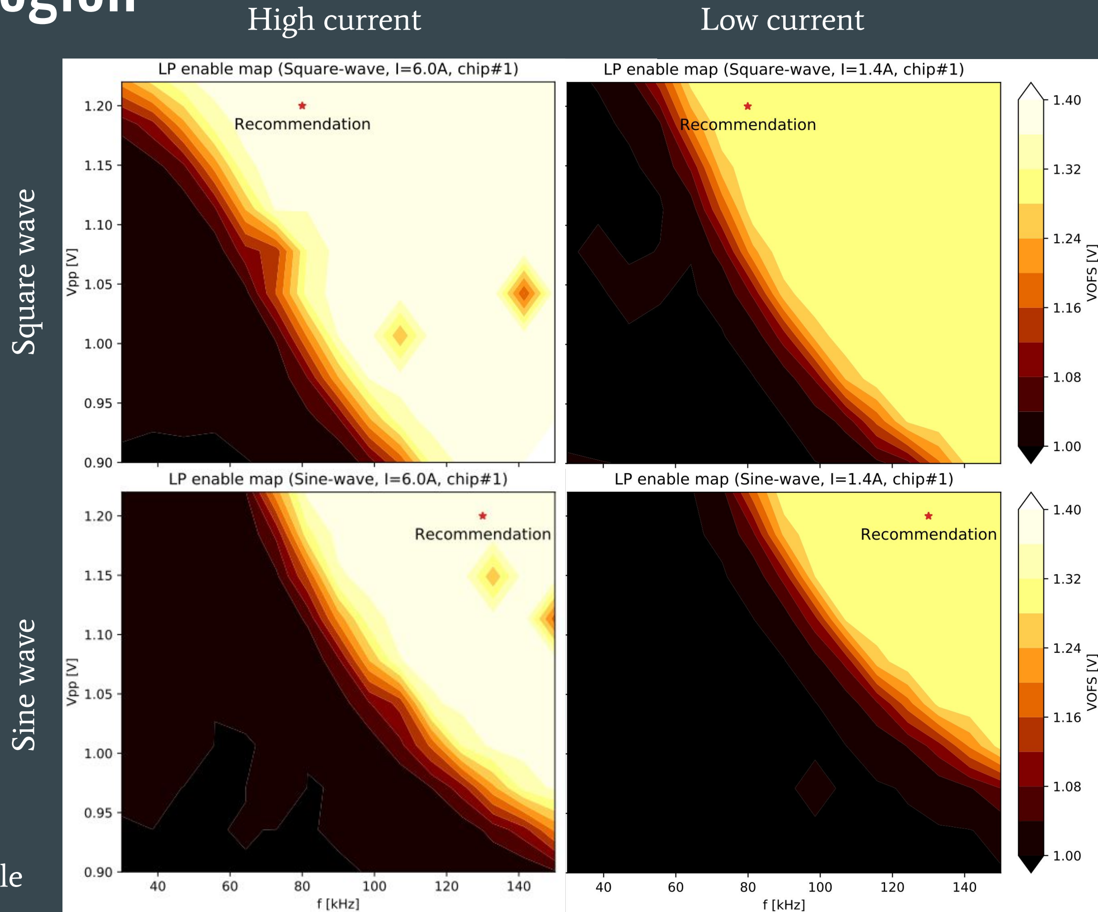
VOFS increased from ~1V to ~1.3V

Reach the ohmic region at a lower current

Low power enable valid region

Scan through the valid region of the injected A/C signal frequency and amplitude and compare against nominal values

Valid = VOFS increased to ~1.3V



From a single quad module

Under-shunt condition

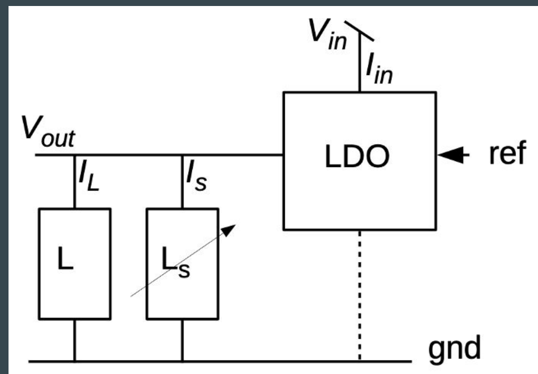
Under-shunt condition and protection

Under-shunt condition: shunt current drops to zero ($I_S \rightarrow 0$) when current consumption drawn by chip loads exceeds input current ($I_L > I_{in}$) (chip faults or wrong configuration)

- Effective resistance decreases from programmed constant value
- Could lead to internal shorts and cause chip damage
- Cause transient effect in a serial power chain

Under-shunt protection prevents shunt current going to 0 and protects against internal short induced by dynamic situation

- Function by reducing the reference voltage VrefA/D and subsequently VDDA/D
- Can cause internal oscillation



$$I_{in} = I_L + I_s = \frac{V_{in} - V_0}{R_{\text{eff}}}$$

$> I_{in}$ < 0

Test under-shunt condition in a serial power chain

Create under-shunt condition by raising the chip current consumption
with or without under-shunt protection

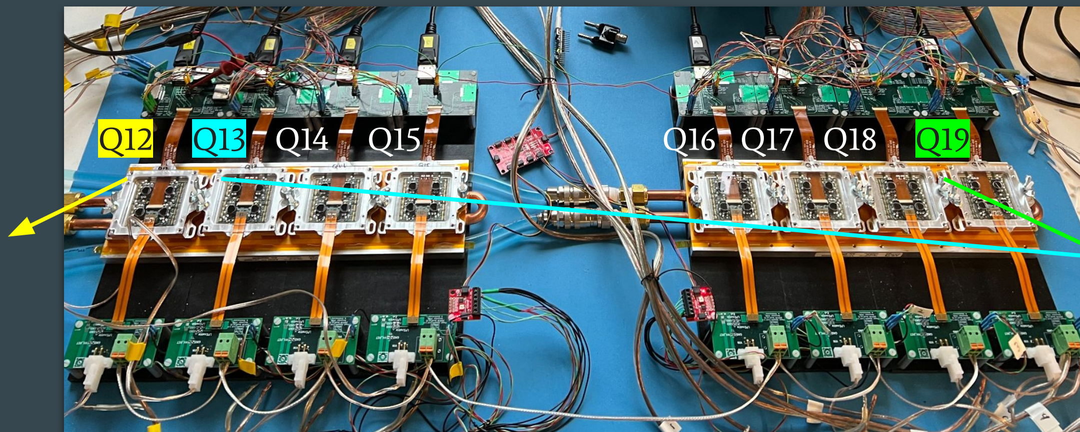
Steady under-shunt:

Change the chip preamplifier settings -> Steady under-shunt for analog domain

Dynamic under-shunt:

Inject signal pulses (digital scan) -> Dynamic under-shunt for digital domain

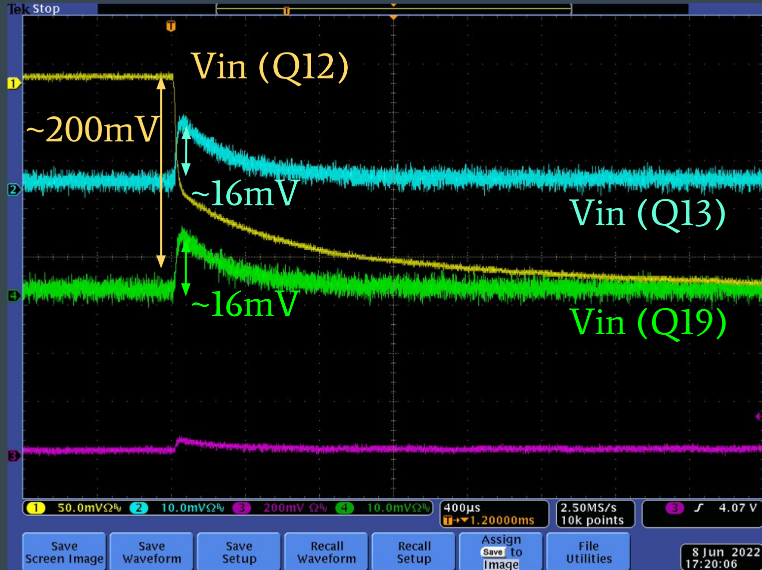
Induce under-shunt



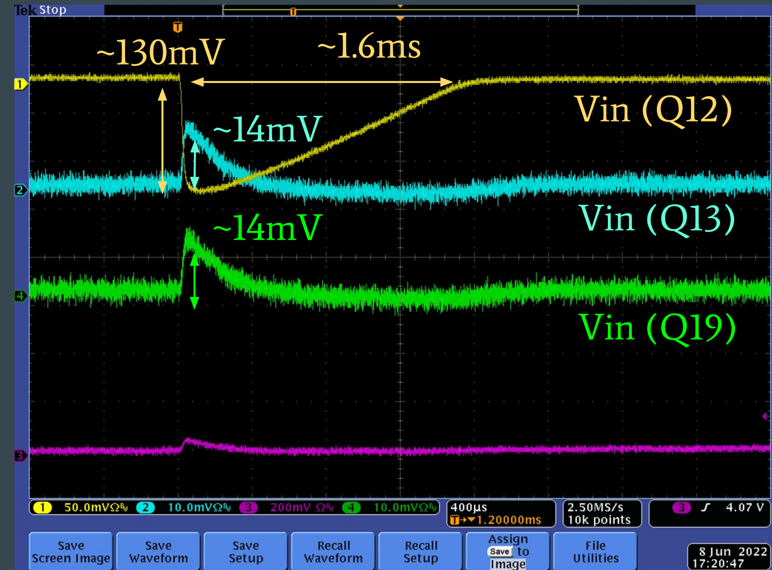
Monitor Vin transient on neighboring modules

Steady under-shunt condition (analog)

Oscilloscope image: Under-shunt protection off



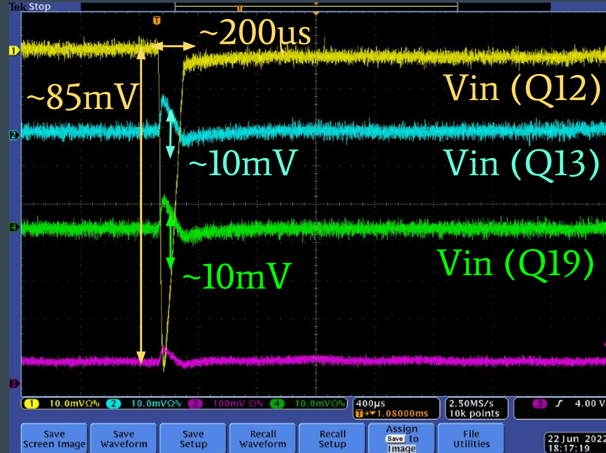
Oscilloscope image: Under-shunt protection on



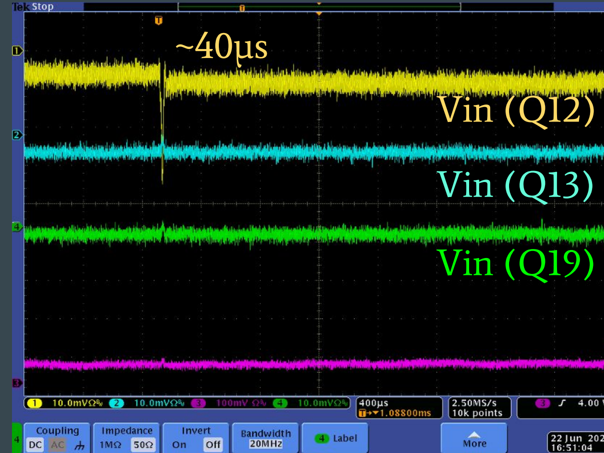
- When under-shunt protection is off: internal short from under-shunt condition causes Vin to drop
- When under-shunt protection is on: internal short is recovered by reducing reference voltage
- Observe transient effects on neighboring modules (both protection on and off)

Response time vs bypass capacitors

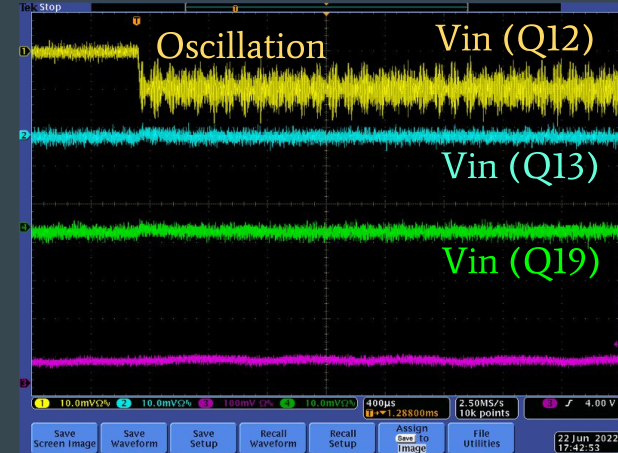
Oscilloscope image:
Under-protection on; Vref cap = 10 nF



Oscilloscope image:
Under-protection on; Vref cap = 1 nF



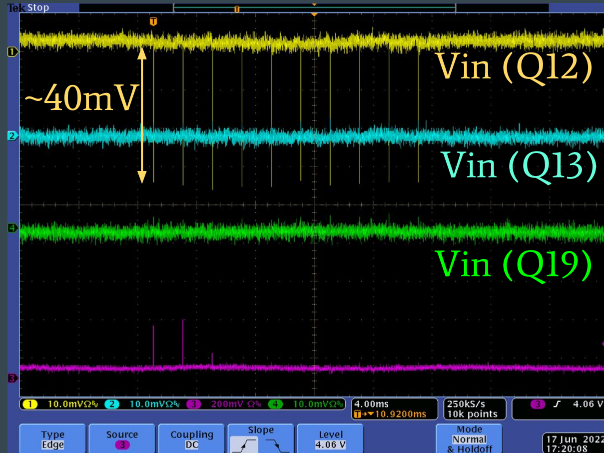
Oscilloscope image:
Under-protection on; Vref cap = 0 nF



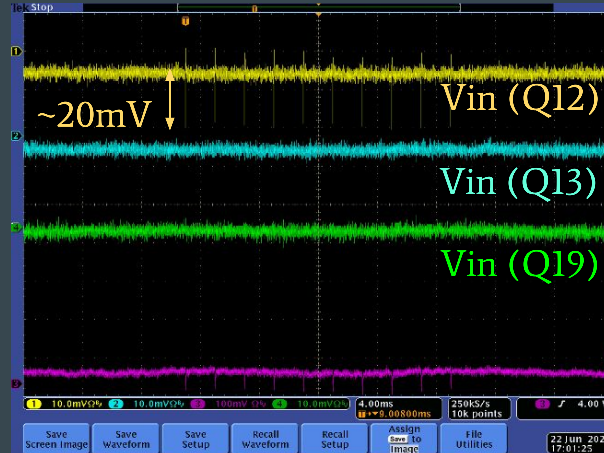
- Response time of under-shunt protection depends on the bypass capacitors for the reference voltages: shorter response time with smaller capacitor -> also smaller transient effects
- Too small capacitor results in large internal oscillations

Dynamic under-shunt condition (digital)

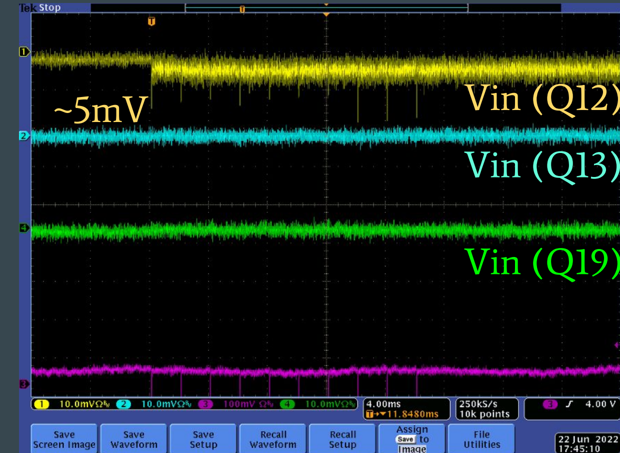
Oscilloscope image:
Under-protection off



Oscilloscope image:
Under-protection on; Vref cap = 1 nF



Oscilloscope image:
Under-protection on; Vref cap = 0 nF



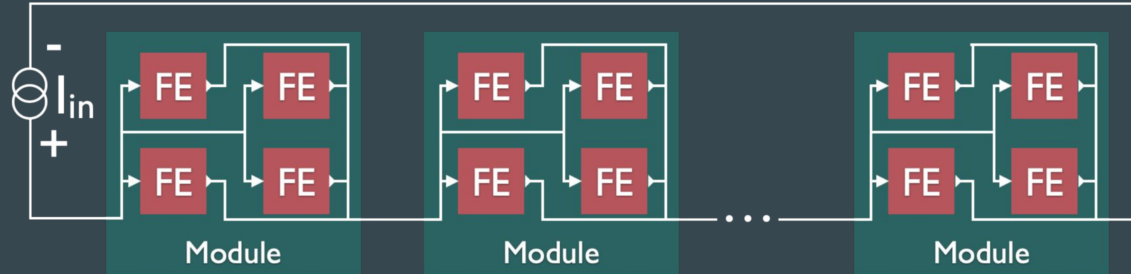
- Similar behavior observed for the dynamic under-shunt condition: small bypass capacitors result in shorter response time and larger internal oscillations
- No substantial issue observed (1 nF found to be a good balance between response time and internal oscillations)

Summary

- Serial powering of the ATLAS ITk pixel modules is a new concept of powering and allows to significantly reduce power cable materials
- Extensive electrical tests on the pre-production (ITkPixV1.1) module serial powering have been performed; powering tests highlighted in this talk:
    - Shunt-LDO voltage-current test
    - Low power mode enabling
    - Test of under-shunt condition
- Observed mild transient effect in a serial power chain, while no substantial issue was found; allows to move forward to the next stage of the chip/module developments!
    - Module pre-production submitted July 2022; chip production to be submitted February 2023

Backup slides

Module Serial Powering



Large volume of powering cable materials affects detector performance

Novel power scheme: groups of modules powered in series to reduce cable materials

Requirements/challenges:

- Constant-current power supply for stable operation
- Voltage drop across module determined by current
- Novel power scheme with no operational experience: need to build confidence with test setups!

Mass dominated by pixel services (e.g. cables)