
# TimeSPOT ASIC developments for 4D pixel readout

*Electronics for high-rate precision-timing Sensors. A system perspective*

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TimeSPOT TIME and SPace real-time Operating Tracker

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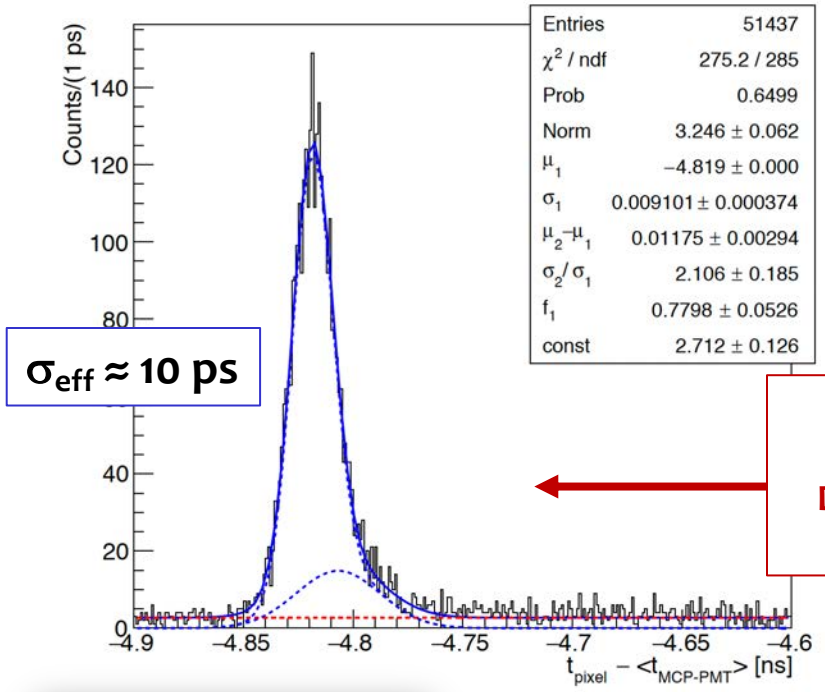
INFN Ground-up iNITiative for µElectronics developments

# CMOS 28-nm for pixels with timing capabilities

## *When system constraints come into play*




**$\sigma_{eff} \approx 10$ ps**

BUT:

**Rate constraints**
**Area constraints**
**Data BW constraints**
**Power constraints**

**A first complete set of «balanced HEP requirements»**

| Requirement | scenario $S_A$ | scenario $S_B$ |
|---|---|---|
| Pixel pitch [μm] | ≤55 | ≤42 |
| Lifetime fluence [$1 \times 10^{16}$ 1 MeV $n_{eq}/cm^2$] | > 6 | > 1 |
| TID lifetime [MGy] | > 28 | > 5 |
| Sensor Timestamp per hit [ps] | ≤ 35 | ≤ 35 |
| ASIC Timestamp per hit [ps] | ≤ 35 | ≤ 35 |
| Hit Efficiency [%] (1.5 W/cm²) | ≥ 99 | ≥ 99 |
| Power per pixel [μW] | ≤ 23 | ≤ 14 |
| Pixel rate hottest pixel [kHz] | > 350 | > 40 |
| Max discharge time [ns] | < 29 | < 250 |
| Bandwidth per ASIC of 2 cm² [Gb/s] | > 250 | > 94 |

LHCb-U2 specs from physics needs. VELO support document for FTDR


**Intrinsic sensor performance measured by means of HBT Si-Ge input stages – discrete components**
**Measured $t_r \approx 100$ ps, $\sigma_{ej} \approx 7$ ps @ 2 fC (1 MIP)**
**900 fs @ 20 fC, 70 mW/channel**

**The toughest constraint against speed is power budget, based on state-of-the-art capabilities in cooling system techniques (micro-channelling $CO_2$).**
**Other systems (e.g. CMS/ATLAS with hermetic structure) have harder constraints (< 1 W/cm²)**

# TimeSPOT ASIC developments

## *Purpose and scope*

TimeSPOT
TIME and SPace real-time Operating Tracker

1. **Explore the capabilities and technical pitfalls of CMOS 28-nm, which has been chosen as the successor of 65 nm for future HEP developments**
2. **Concentrate first on pixel performance addressing the questions:**
   - **What can be integrated in a pixel ≈ 50x50 μm² ?**
   - **Refererred to a target $\sigma_t \approx 30$ ps ($\sigma_{FE} \oplus \sigma_{TDC}$), what is the minimum power required ?**
   - **What is the maximum sustainable rate/pixel – or – is it possible to integrate 1 TDC per pixel?**
   - **What would be the best TDC resolution and its power consumption?**
3. **Design and produce the largest possible chip, compatibly with budget (32x32 pixels was the choice)**
4. **Drop the requirement about high data bandwidth, which needs specific additional developments (as Silicon Photonics)**

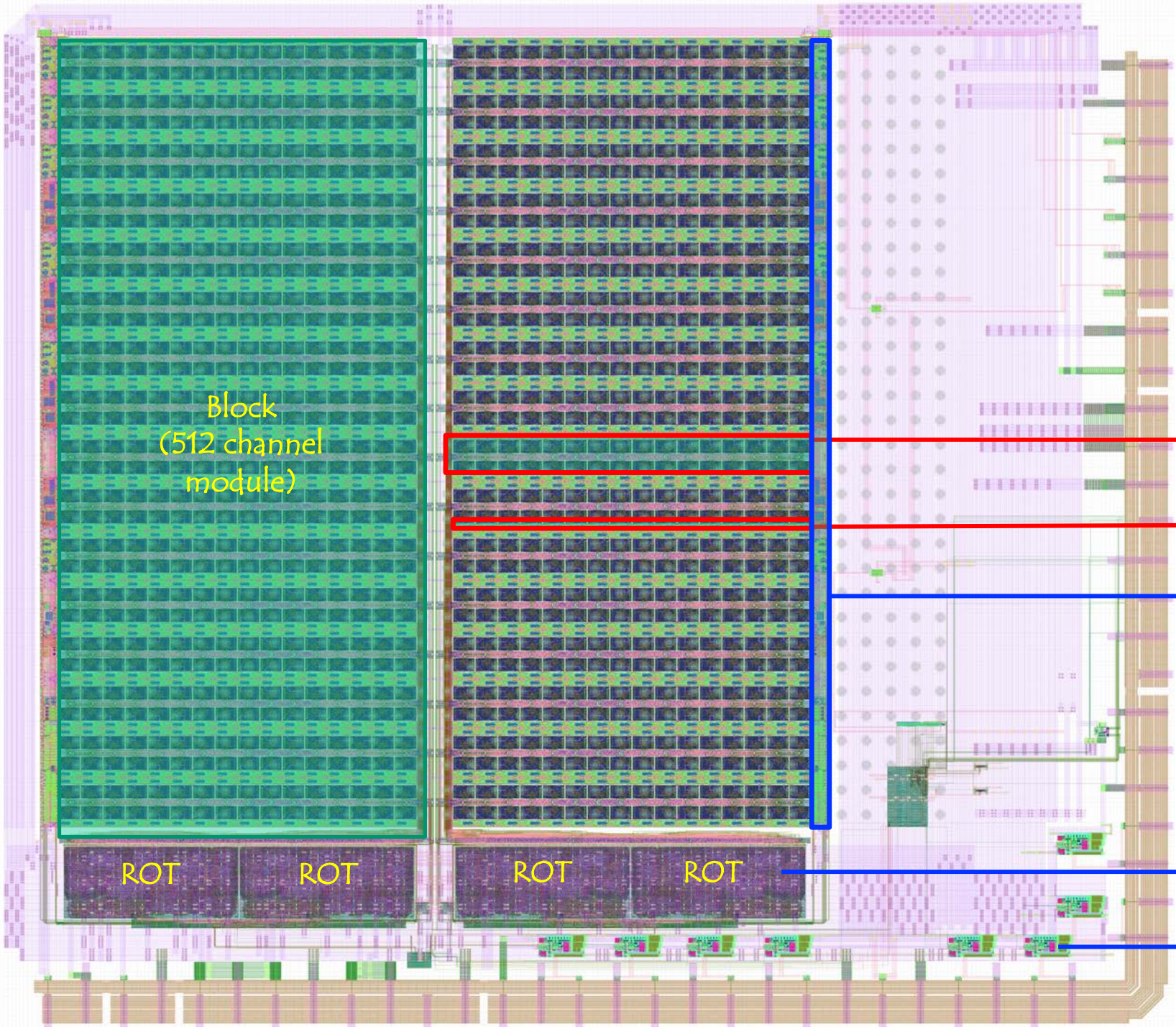
**2 submissions made: Timespot0 (single test-cells) and Timespot1 (complete matrix)**

# Timespot1 ASIC

## 28-nm CMOS

- Reduced size (1024 pixels, 6 mm²)
- HPC flavour
- Complete set of functionalities for pixel readout
- Slow read-out (demo-test purpose)

INFN Cagliari, Milano, (Pavia), Torino




640 MHz master clock

Digital row: 16x2 TDC
+ Controls, Conf. registers, I²C I/F

Analog row (16x2 AFE)

Analog (service) column.
Each contains:

- 1 Band-Gap circuit (Pavia)
- 5x Σ–Δ DACs (producing analog levels used by pixels)
- Programmable bias cell (for power consumption)
- bias replicas with source followers.

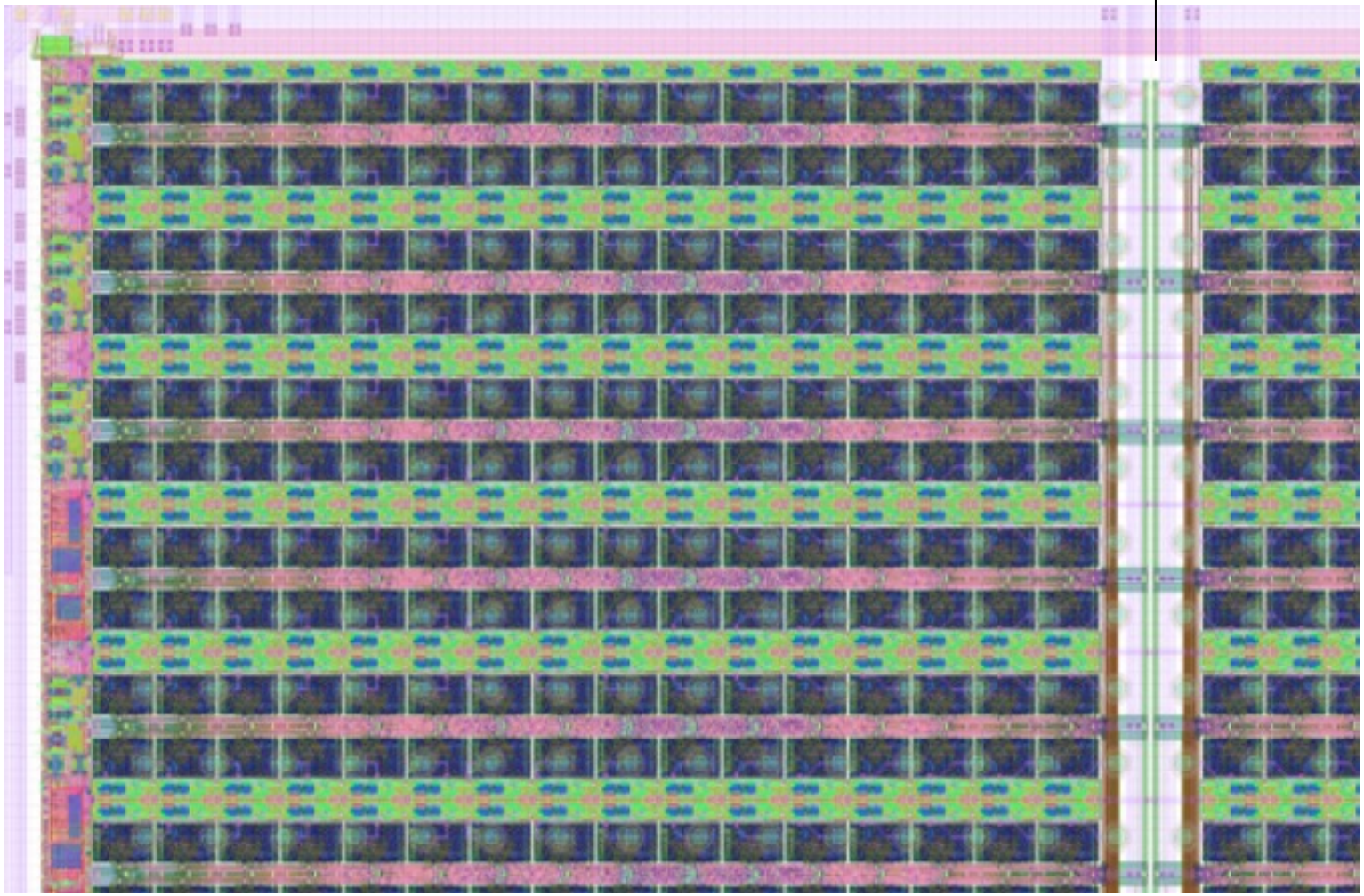
4x Read Out Trees

8x LVDS driver (Pavia)
(each @1.28 Gbps)

# The TimeSPOT1 ASIC

## *Floorplan concept*

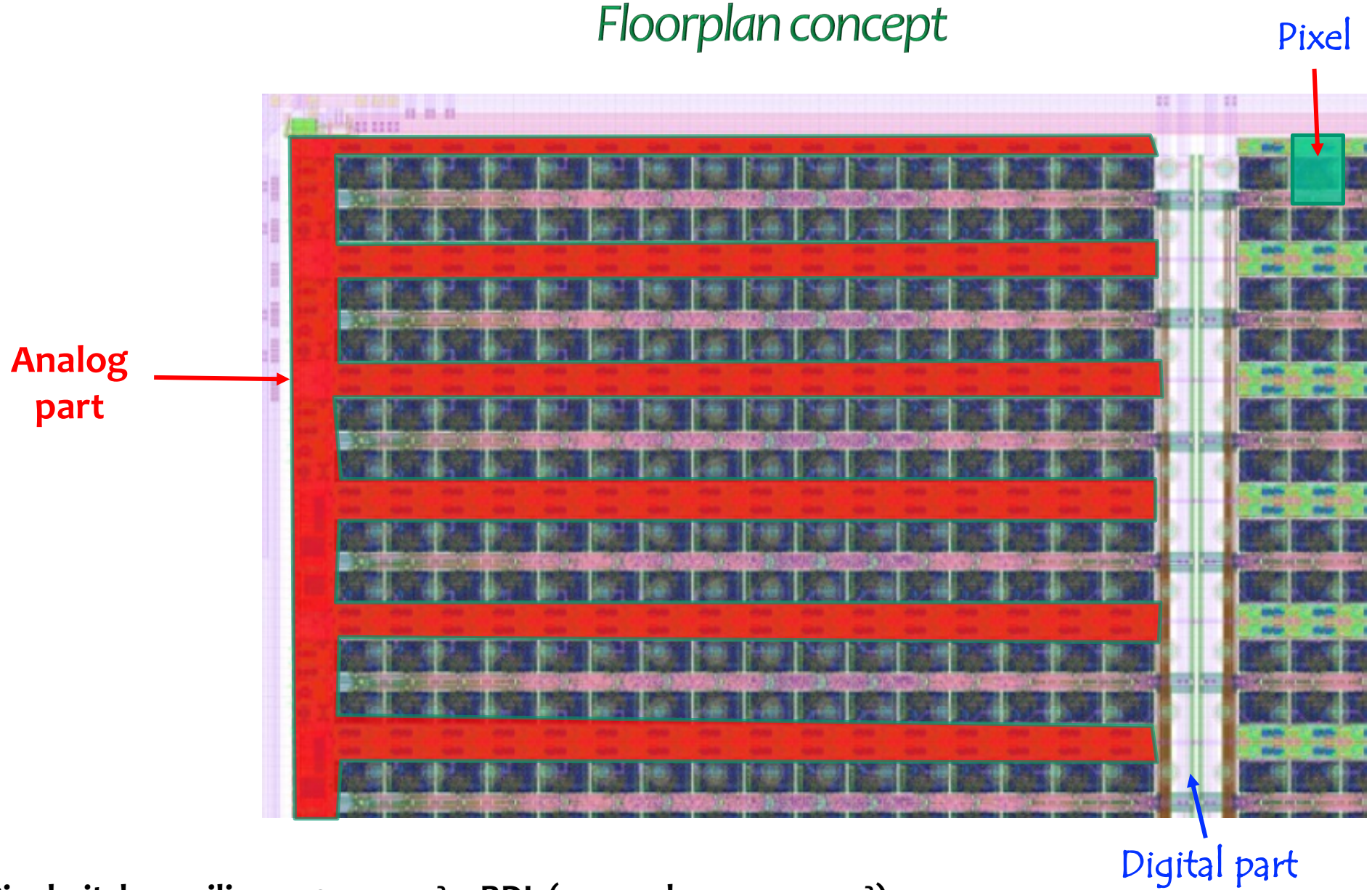
Every 16 pixels 80 µm are gained (40 µm per side) and used for inter-connectivity



**Pixel pitch on silicon 50x55 µm² + RDL (sensor has 55x55 µm²)**

# The TimeSPOT1 ASIC

## *Floorplan concept*



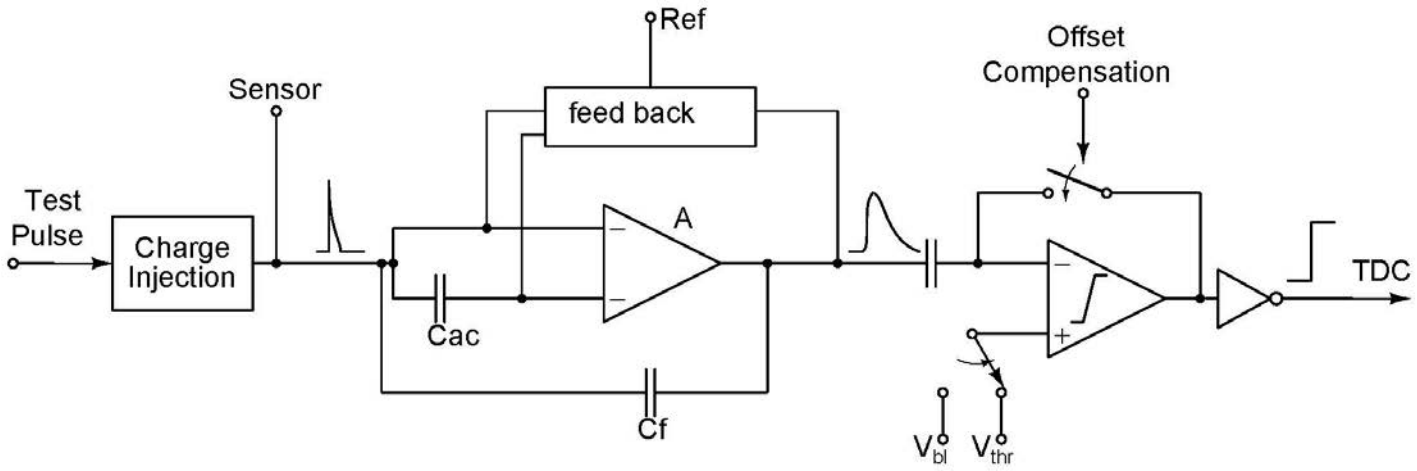

**Pixel pitch on silicon 50x55 µm² + RDL (sensor has 55x55 µm²)**

# Timespot1: Analog Front End

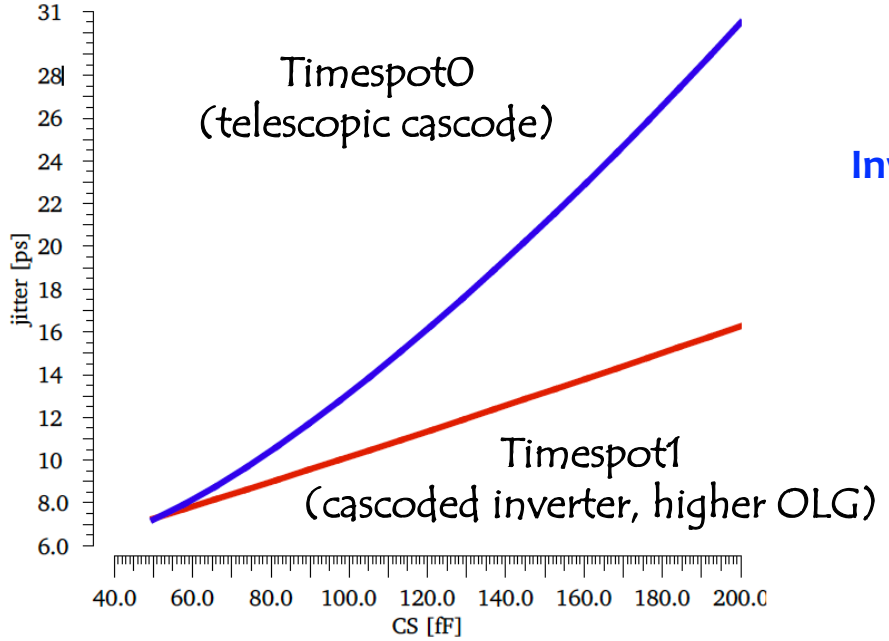
## *Inverter core amplifier with double Krummenacher FB*

**Leading Edge Discriminator with Discrete-time Offset-Compensation for threshold uniformity**
**OC procedure: 250 ns every ≤800 µs**
**(it causes dead time)**

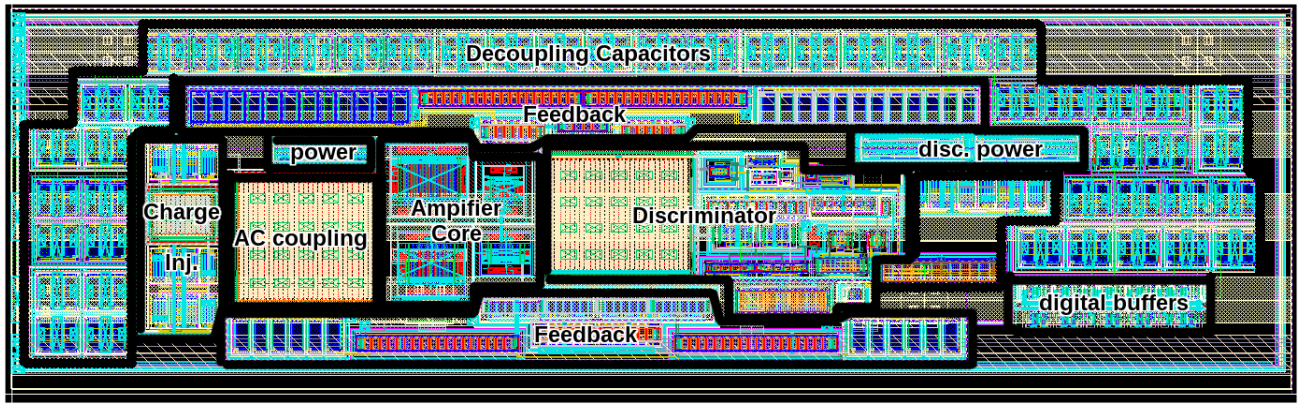
**Programmable power from 2.5 to 32 µW/channel**




**Inverter-based Charge Sensitive Amplifier (CSA) with DC current compensation.**




**Expected performance @ 2 fC**
**(post-layout simulation)**




**50x15 µm²**
**(space available)**

# Timespot1: TDC

## *Fully digital design, standard-cell based*

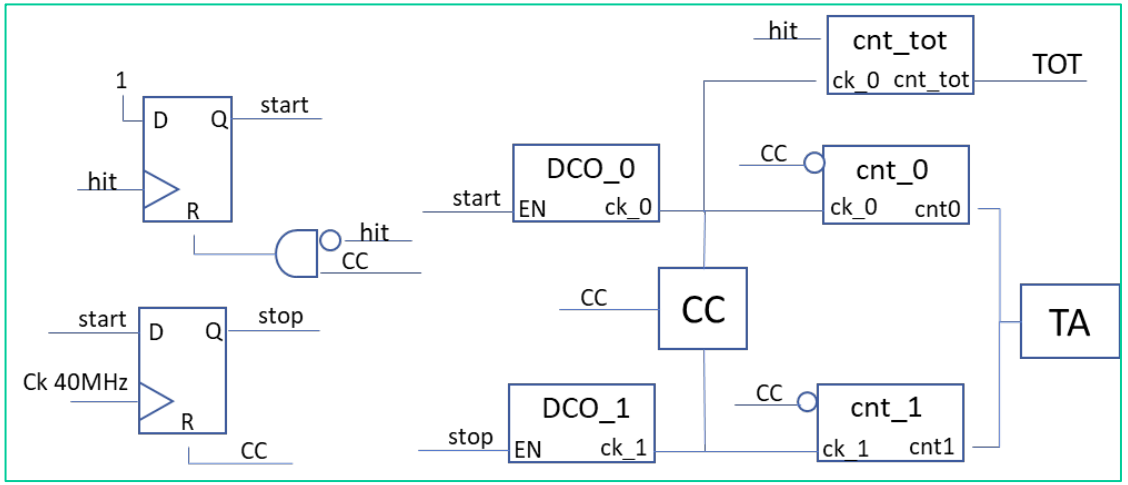
**To maximize sustainable rate, 1 TDC per pixel channel has been integrated**

**Max input rate = 3 MHz/pixel**
**23 bits output word (ToA + ToT)**
**ToT resolution ≈ 1 ns**

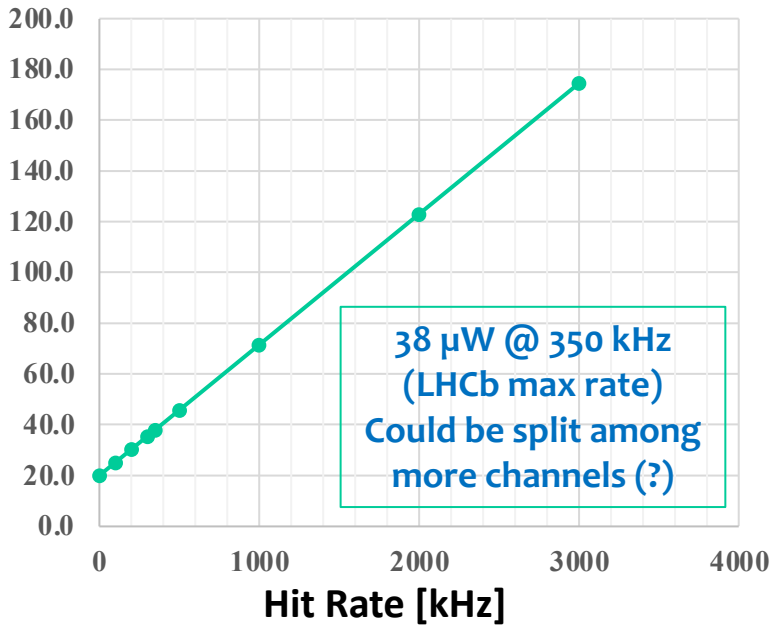
**High resolution, "low" consumption TDC based on 2 DCOs and a Vernier architecture**

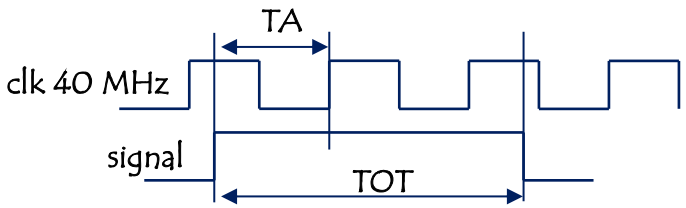
**Max conversion time 300 ns**

$$TA = (cnt_0 - 1)\,T_0 - \\ - (cnt_1 - 1)\,T_1$$

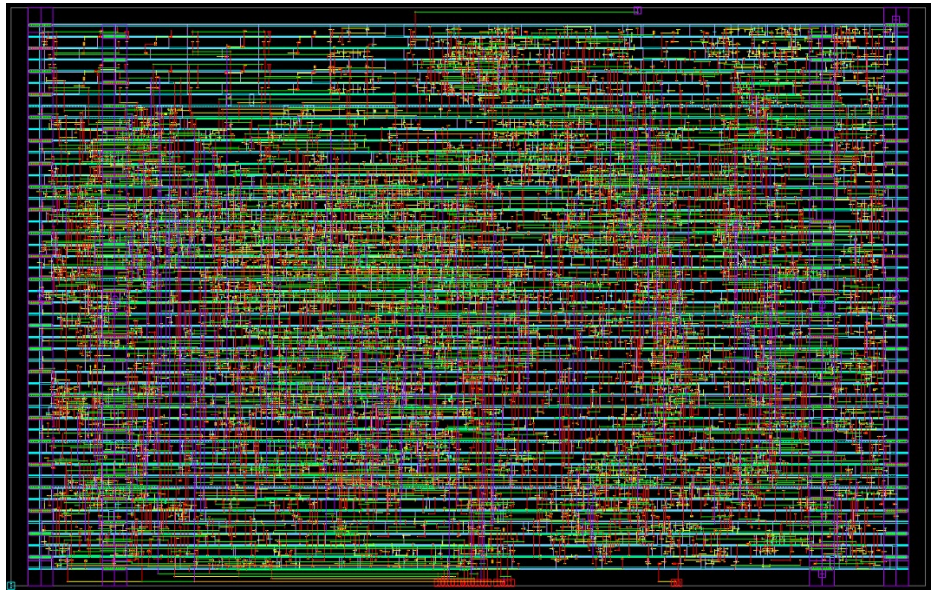



**Expected power per rate**




**The TDC gives the phase of the signal wrt the 40MHz BX clock**
**The TDC and the counter use the same DCO-generated Clk (~1 GHz)**
**4 levels of Vernier precision ($\Delta f$ in DCOs) can be programmed.**
**Typical LSB 12 ps**

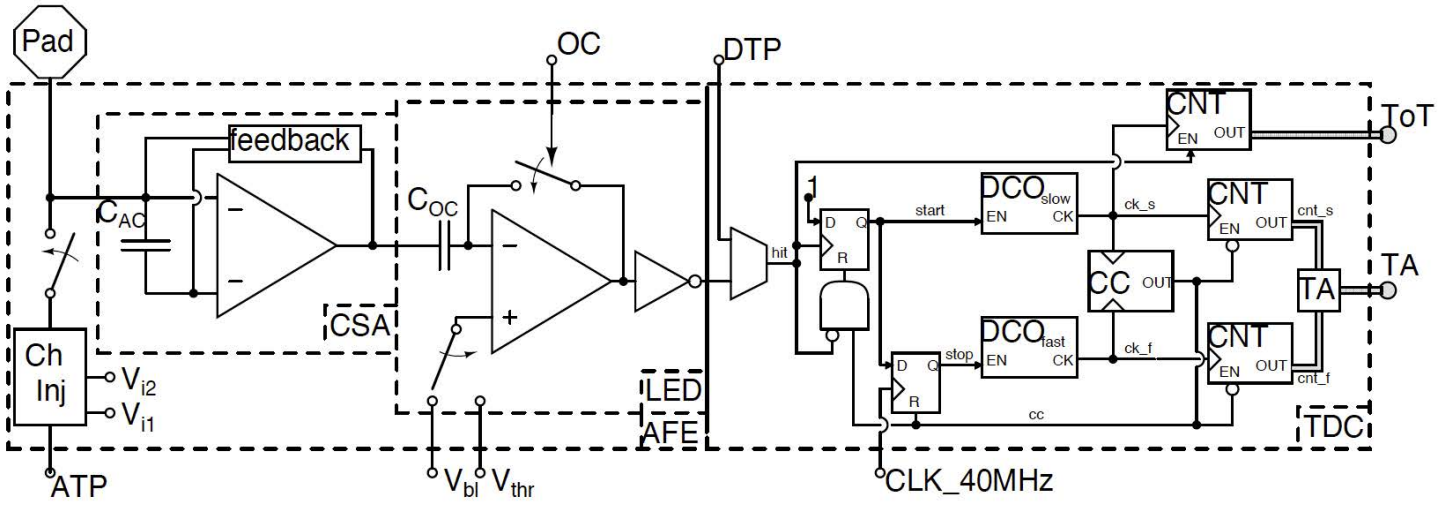


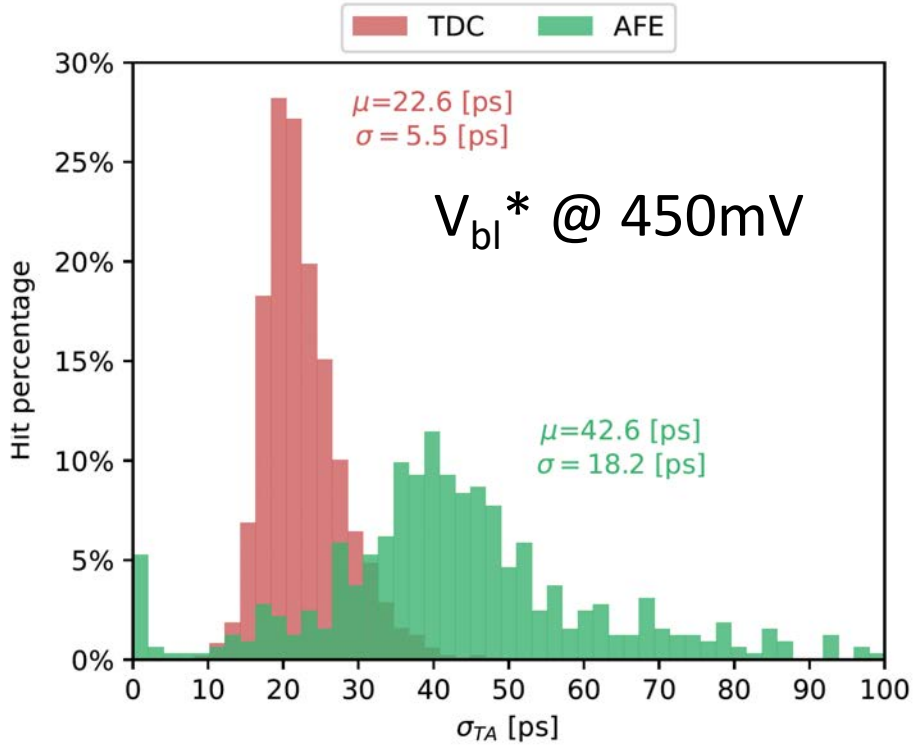
**50x32 µm²**

# Pixel architecture & characterization

## *Time resolution (no sensor)*

- The TDC has a typical $\sigma_t \approx 20$ ps, with a dispersion around 5 ps and is limited by the system clock jitter. As a consequence, no improvements are visible when increasing the Vernier precision
- The AFE $\sigma_t$ is intrinsically below 20 ps but an identified bug in the Offset Compensation of the LE discriminator spoils $\sigma_t$ in most of the channels (see next slide).
- In general, issues which are extrinsic to circuit design limit the very good resolution at the pixel level (clock distribution, OC bug). The pixel circuit design appears adequate to system requirements.

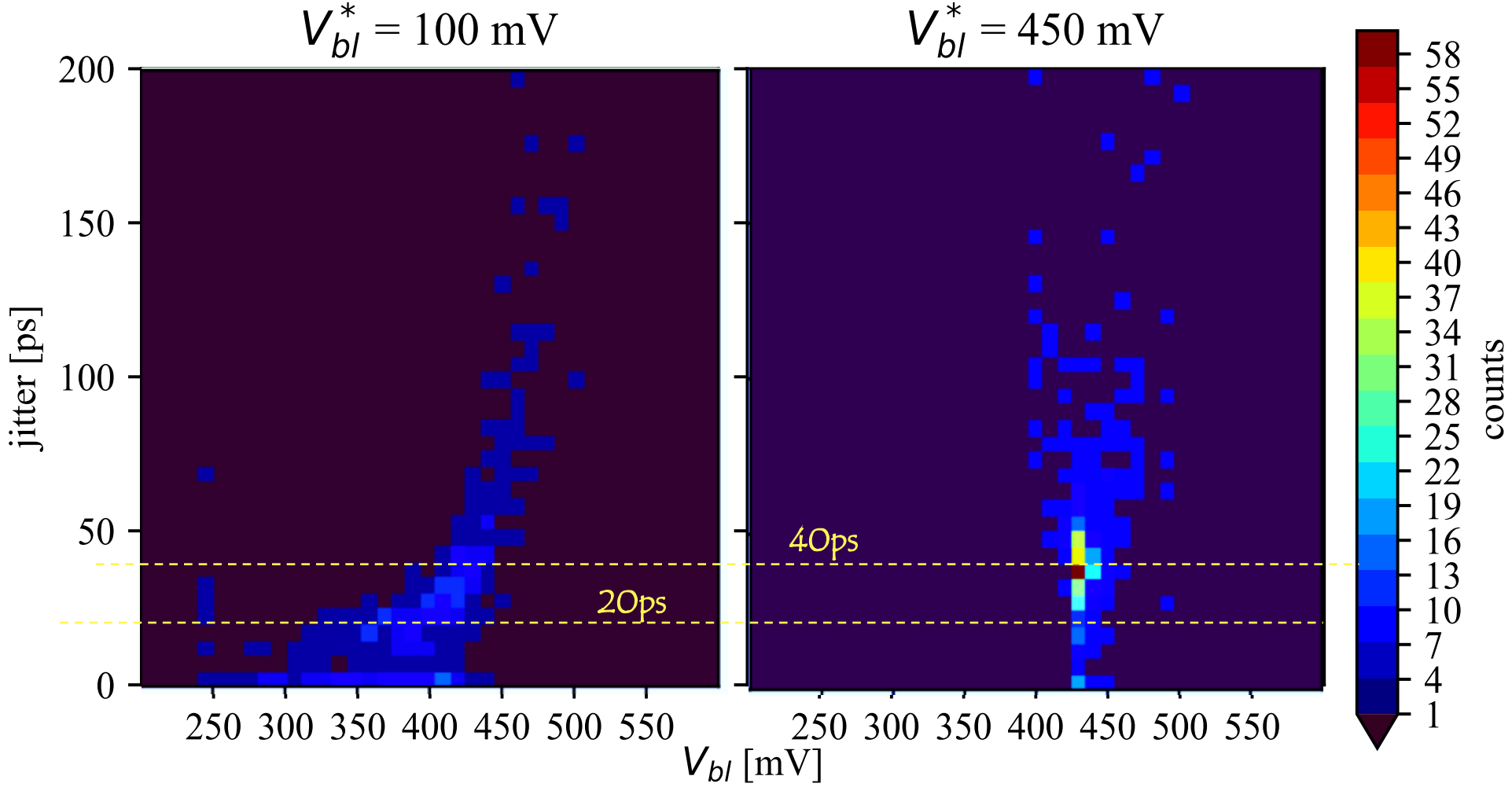


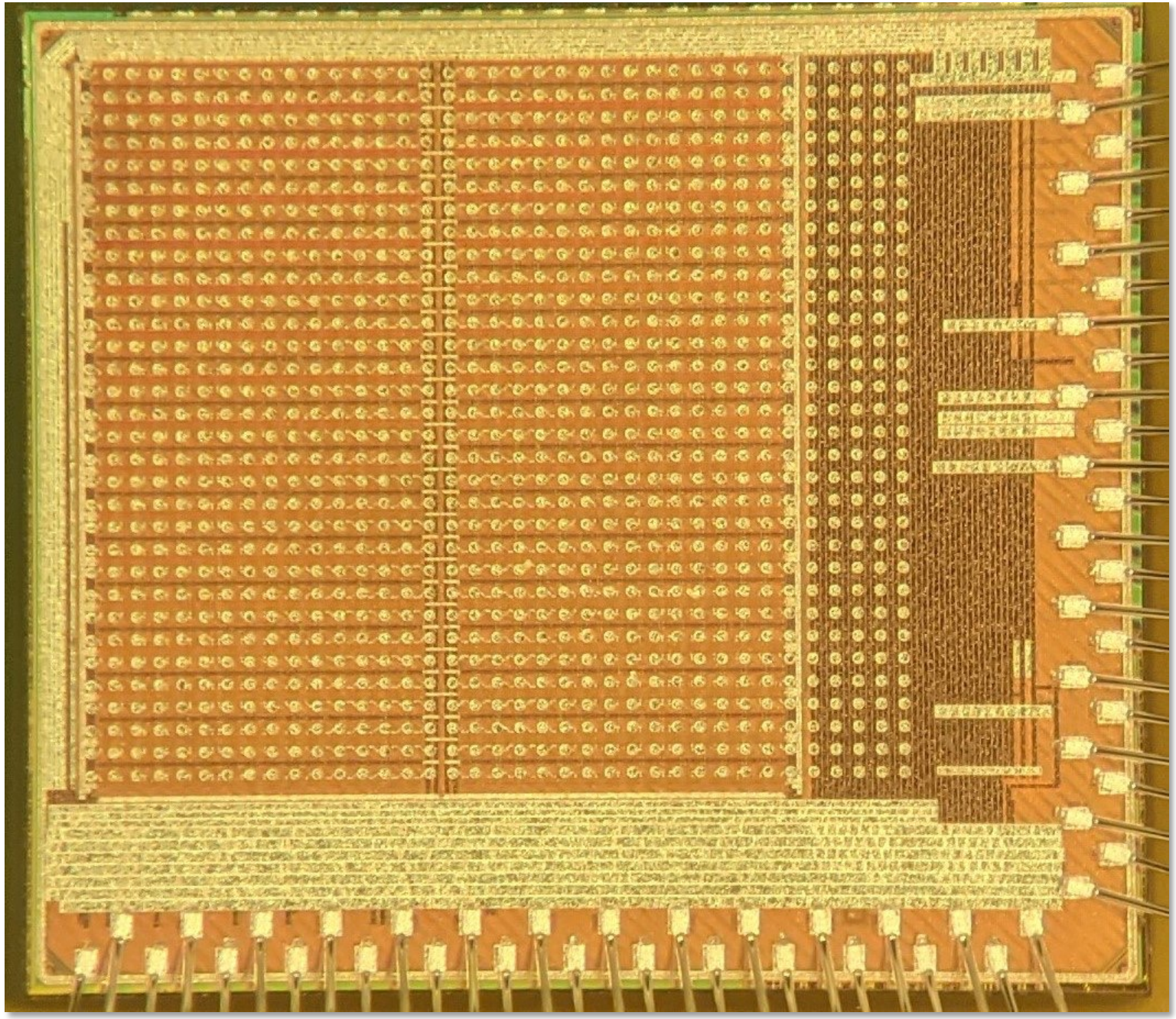

@ 12 µW on AFE

# Pixel: the Analog Front End

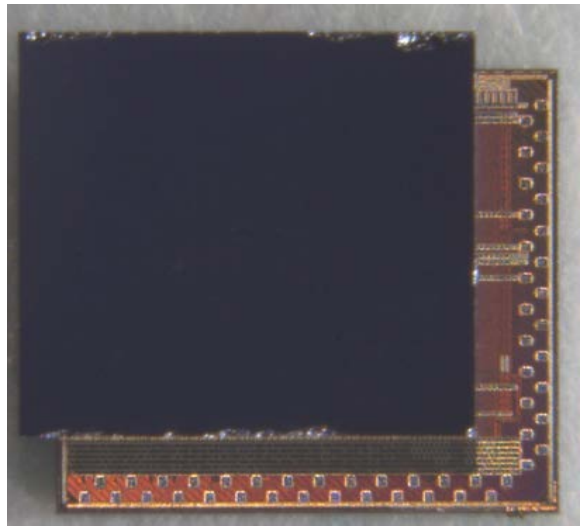
## *inadequate Offset Compensation*



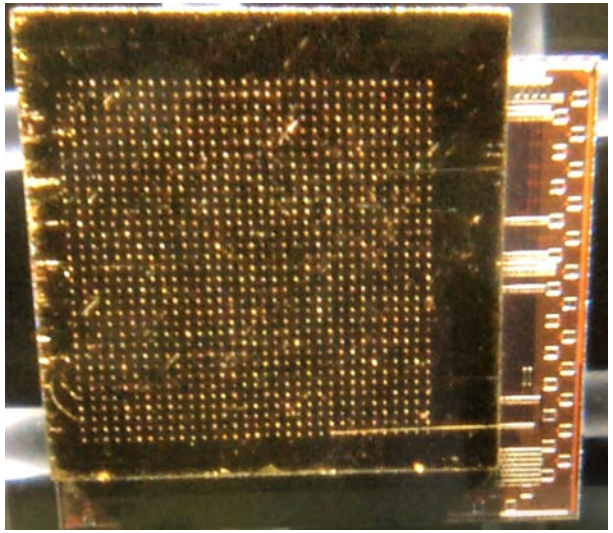

- When $V_{bl}$ is set at low values, in most of the channels, the OC circuit fails to charge the memory capacitance $C_{OC}$ .
- The discriminator is forced to work at high voltages, where it is band-limited
- The timing performance is heavily degraded



## Timespot1 on 3D-trench silicon matrix



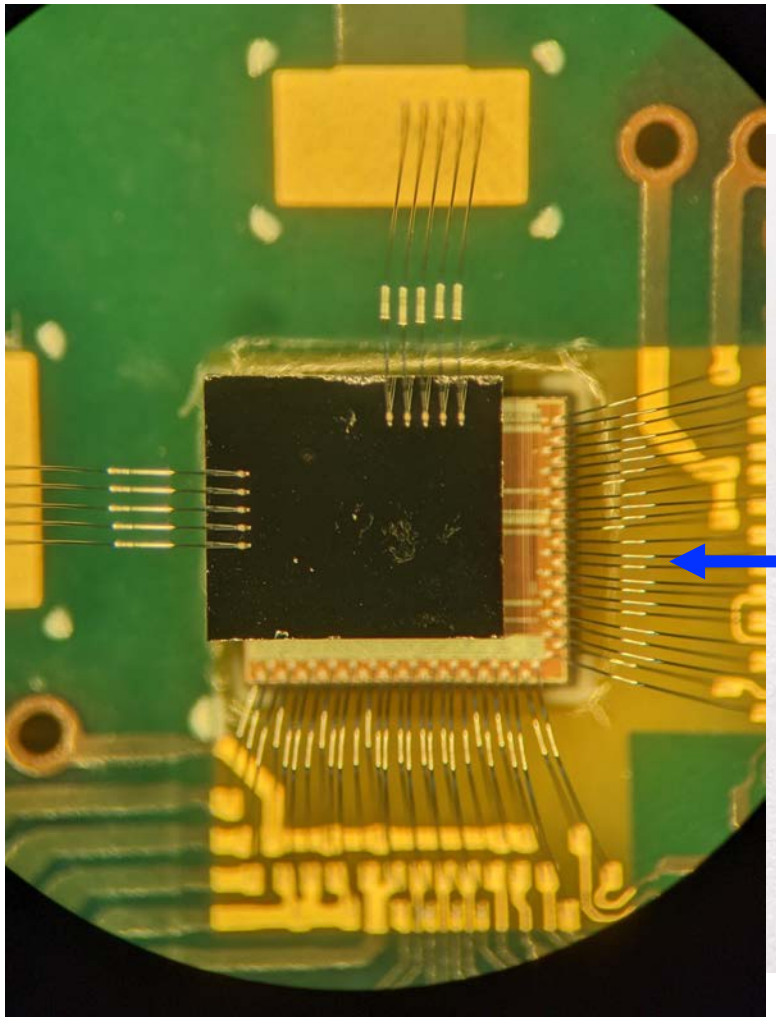
## Timespot1 on 3D-column diamond matrix

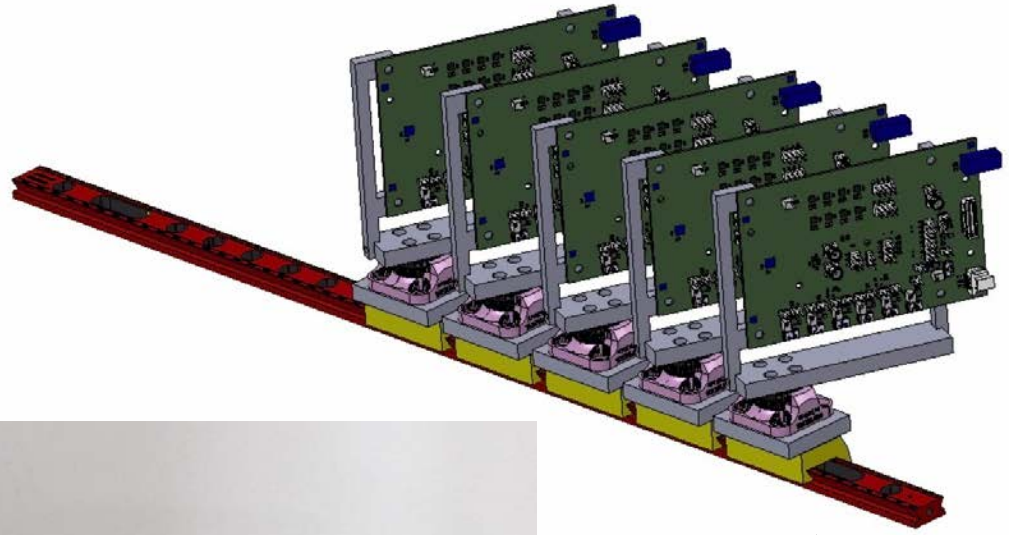


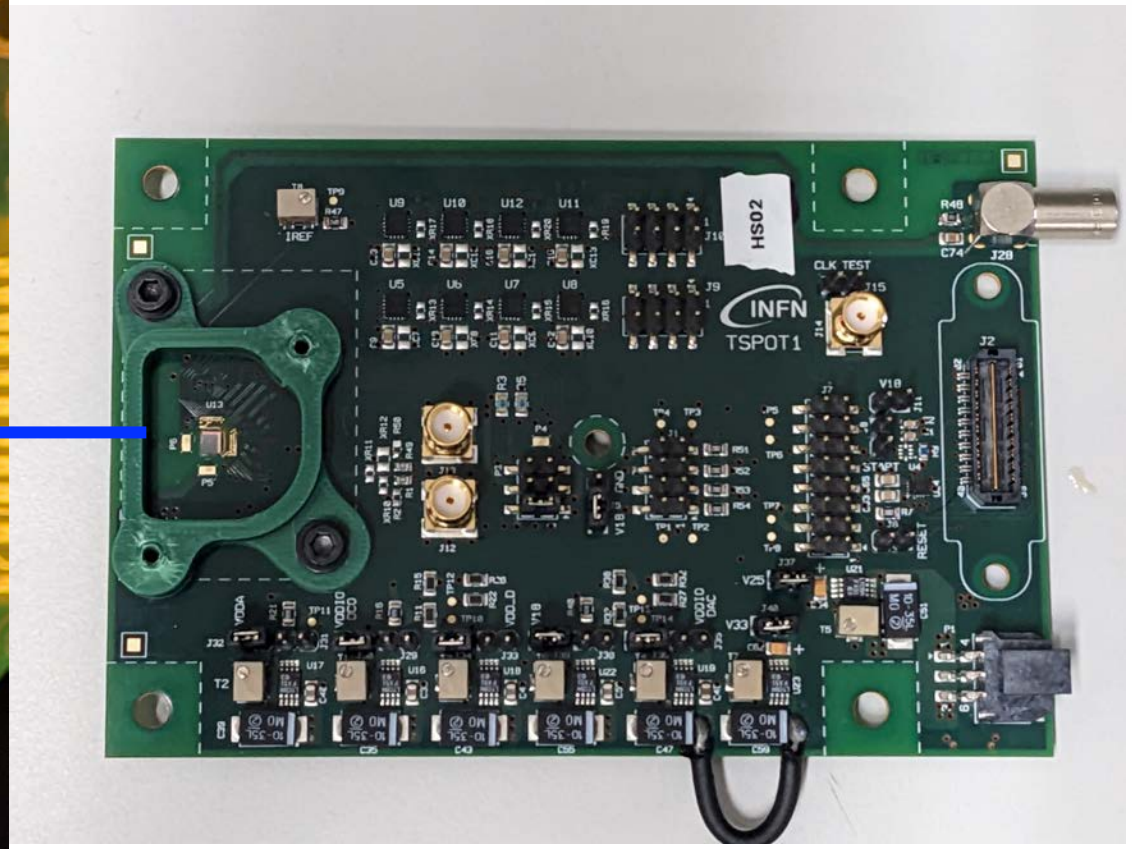
Fraunhofer IZM

# Hybridized devices

## *with 3D sensors*








**The test-bench PCB (named TSPOT1) operates also as a tracking station in the demonstrator**

# Hybridized devices

## *Cagliari test bench and ongoing tests*

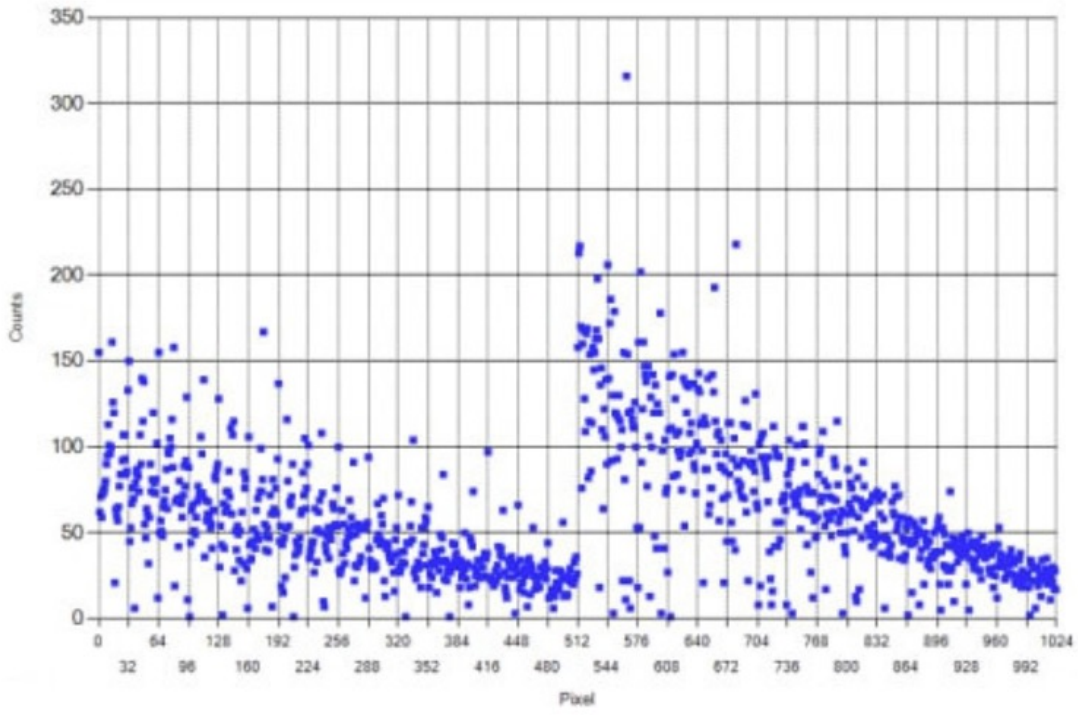
- **The system is completed by a low-jitter clock distributing board and an aggregation board (Mezzanine), which hosts up to 8 boards/layers.**
- **The Mezzanine is connected onto a KC705 performing DAQ functionalities (up to 10 Gbps)**
- **Hybrids are being tested by internal pulsing system and beta radiactive source**
- **Subsequently they will be characterized under IR synchrounous laser setup in the lab**
- **Test beam is foreseen next spring at SPS (up to 8 stations, silicon and diamond hybrids)**

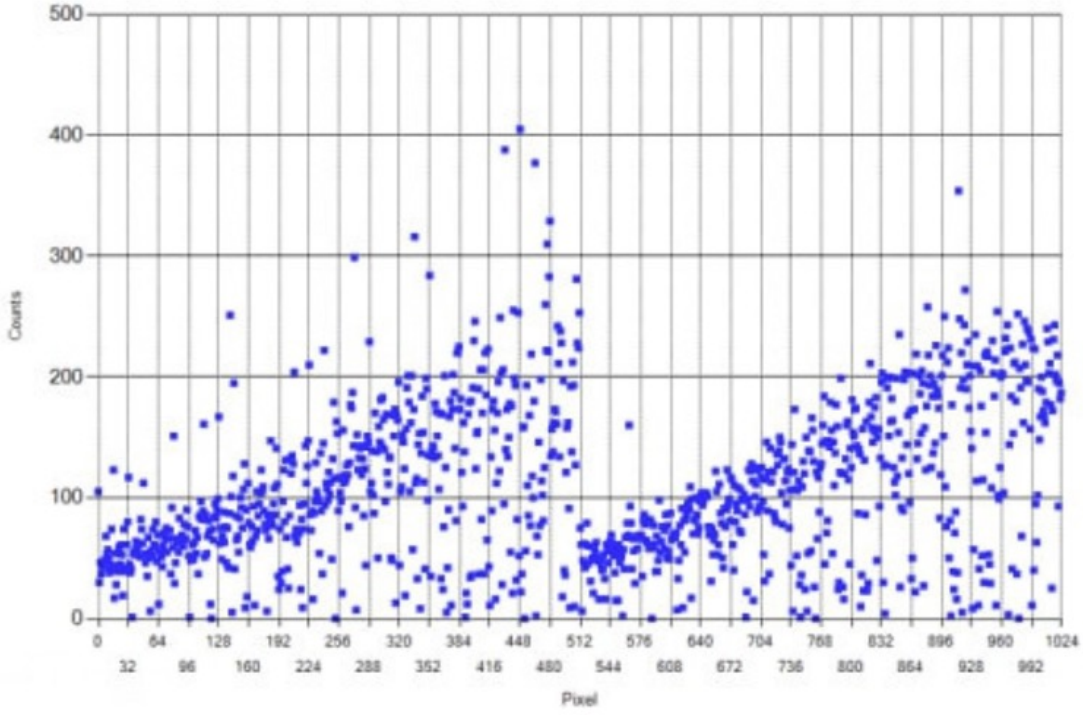
Clock distribution board Si5341

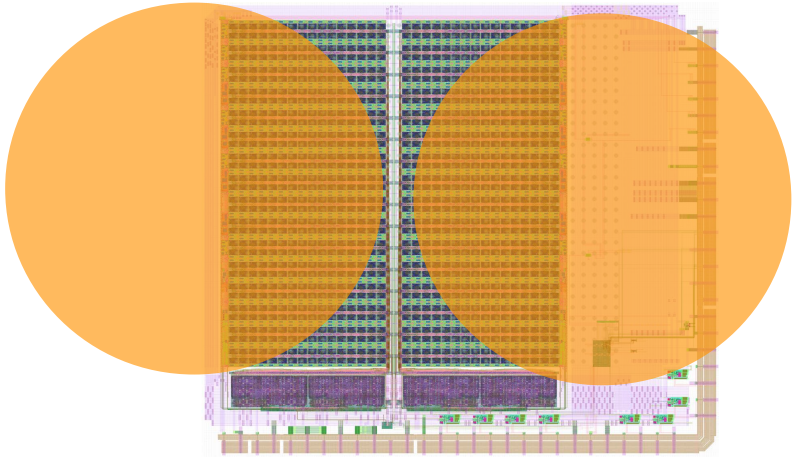
Mezzanine (max 8 tracking layers/DUT) and KC705 FPGA readout board

2 DUT on 2 TSPOT1 PCB

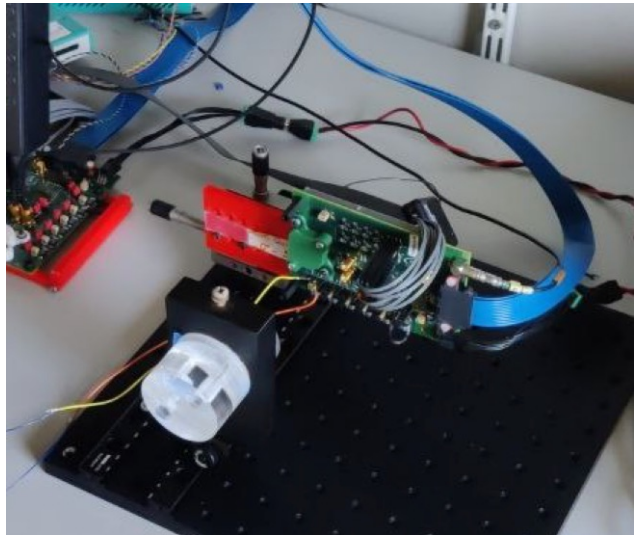
# Hybridized device under $^{90}$Sr source



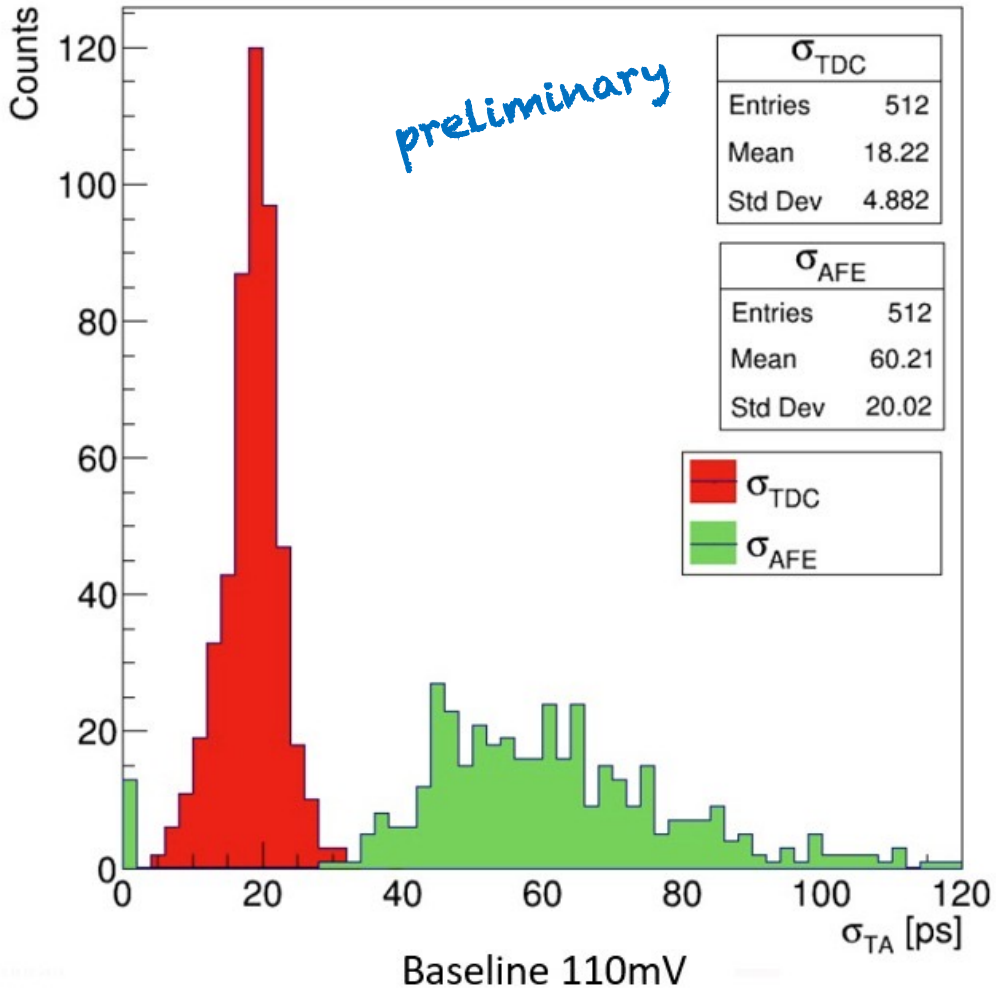



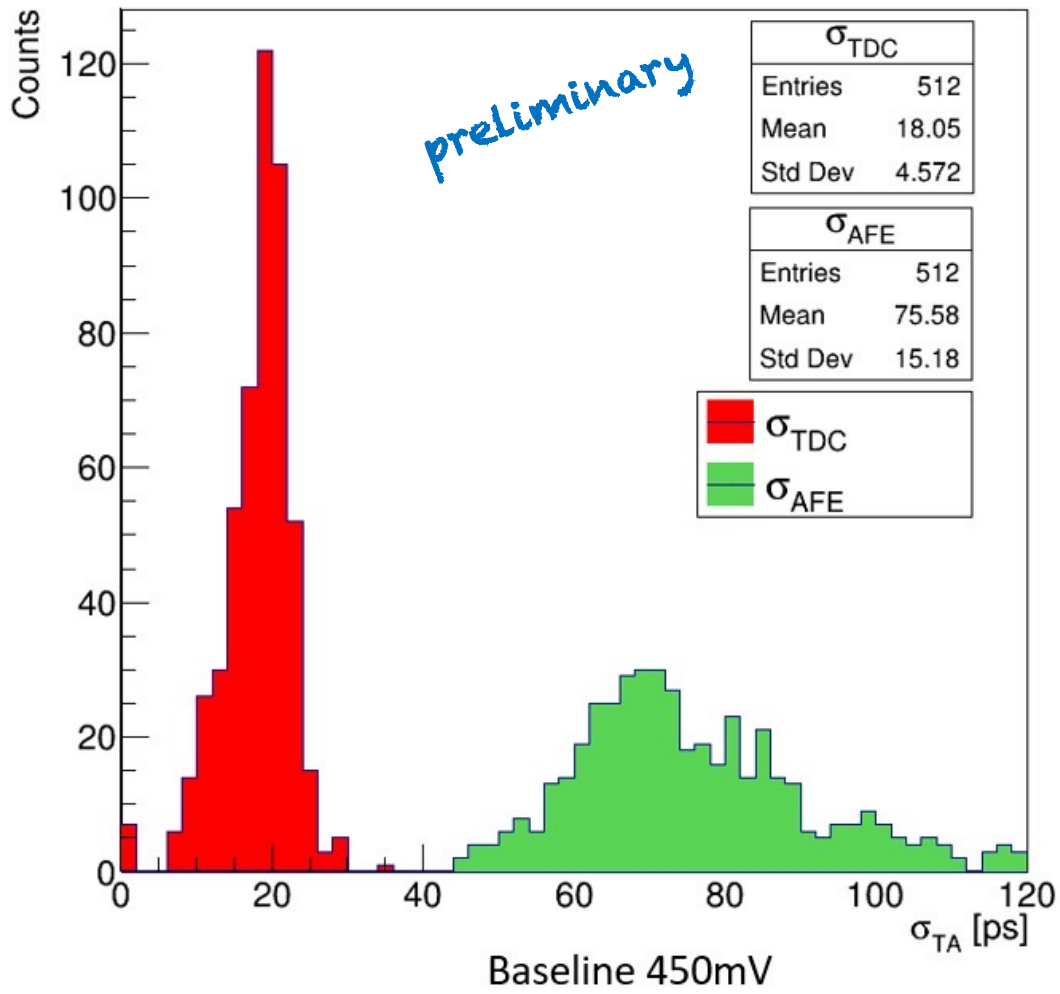
**Off-centered $^{90}$Sr source**



# Hybridized devices

## *time resolution (2 fC pulses, sensors connected)*



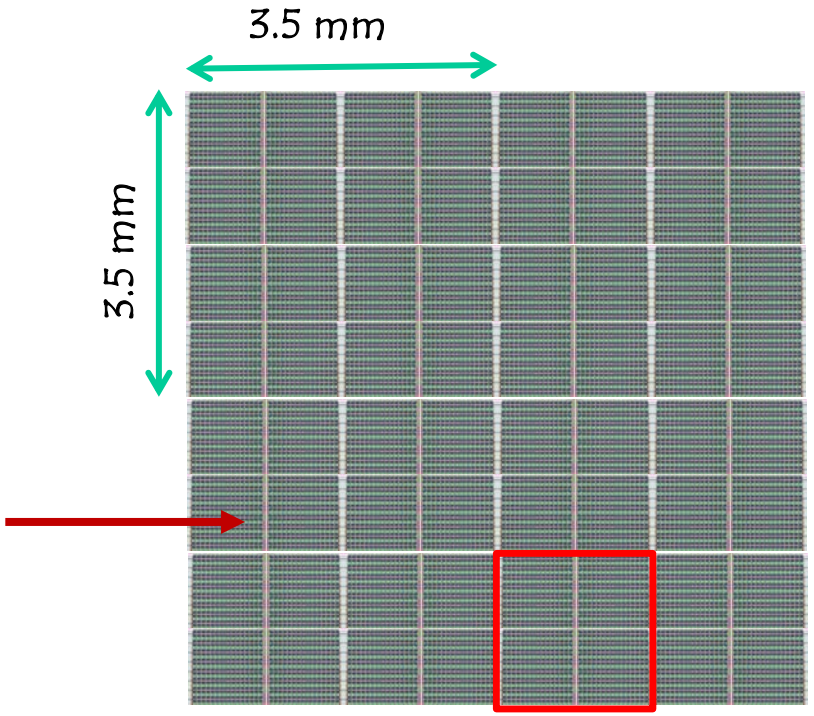

**Same behaviour with slight worsening of timing performance. Performance is dominated by the discriminator**

# Conclusions and Outlook

1. At the pixel level, the Timespot1 ASIC shows an intrinsic timing performance around 20 ps, both on the AFE and TDC stages at a reasonably low consumption (≈ 12 μW on the AFE stage)
2. Leaving apart the (amendable) OC-bug, true limitations are due to global issues as clock jitter and power distribution (such as geographical disuniformities, dispersion of values, instabilities when power is increased)
3. As expected, verification methods at the full ASIC level are crucial in this technology

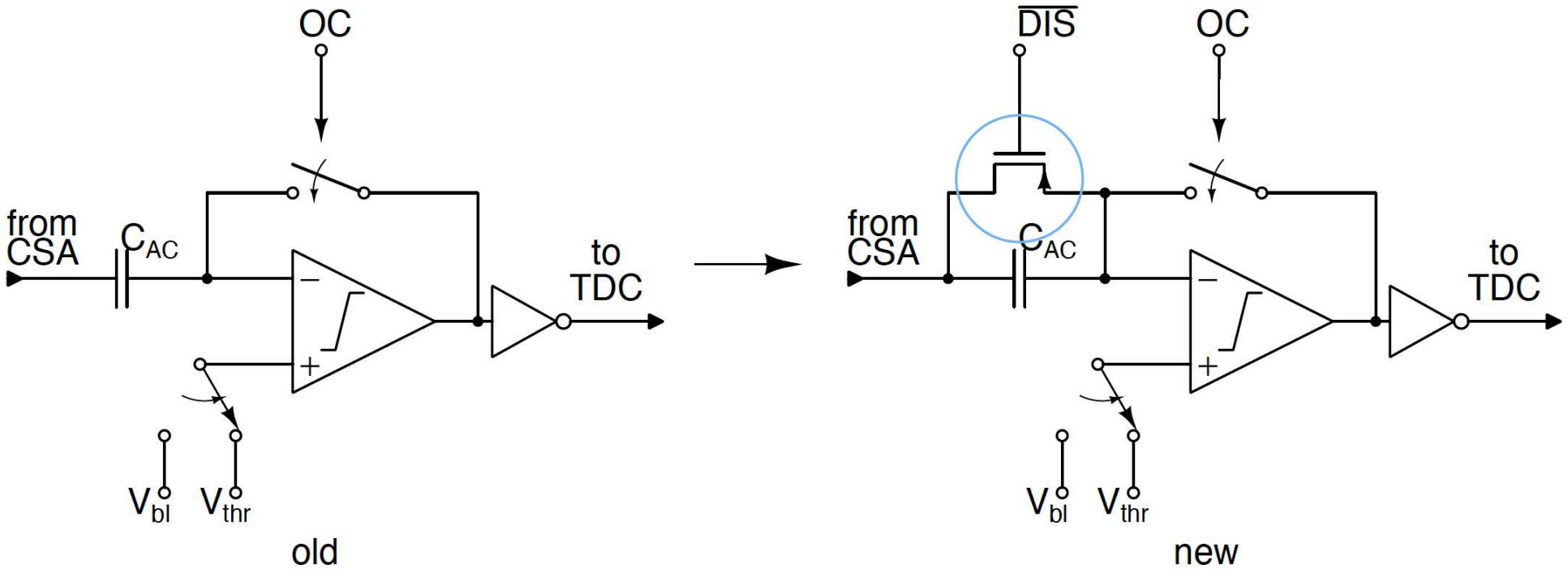
**FUTURE:**

- A test beam with up to 8 tracking station is in preparation for Spring 2023
- We are already working (**IGNITE** project) at the next version of the ASIC, with corrected features, fast readout (by integrated photonics), radiation hardening features and larger area (64x64 or 128x128 pixel matrix).
- The **IGNITE** ASIC aims at addressing the full requirements for 4D-tracking. Discussions on specs are ongoing in the present months. Many «users» interested (LHCb, HIKE, CMS-PPS, CMS-Endcap, ATLAS-AFP)

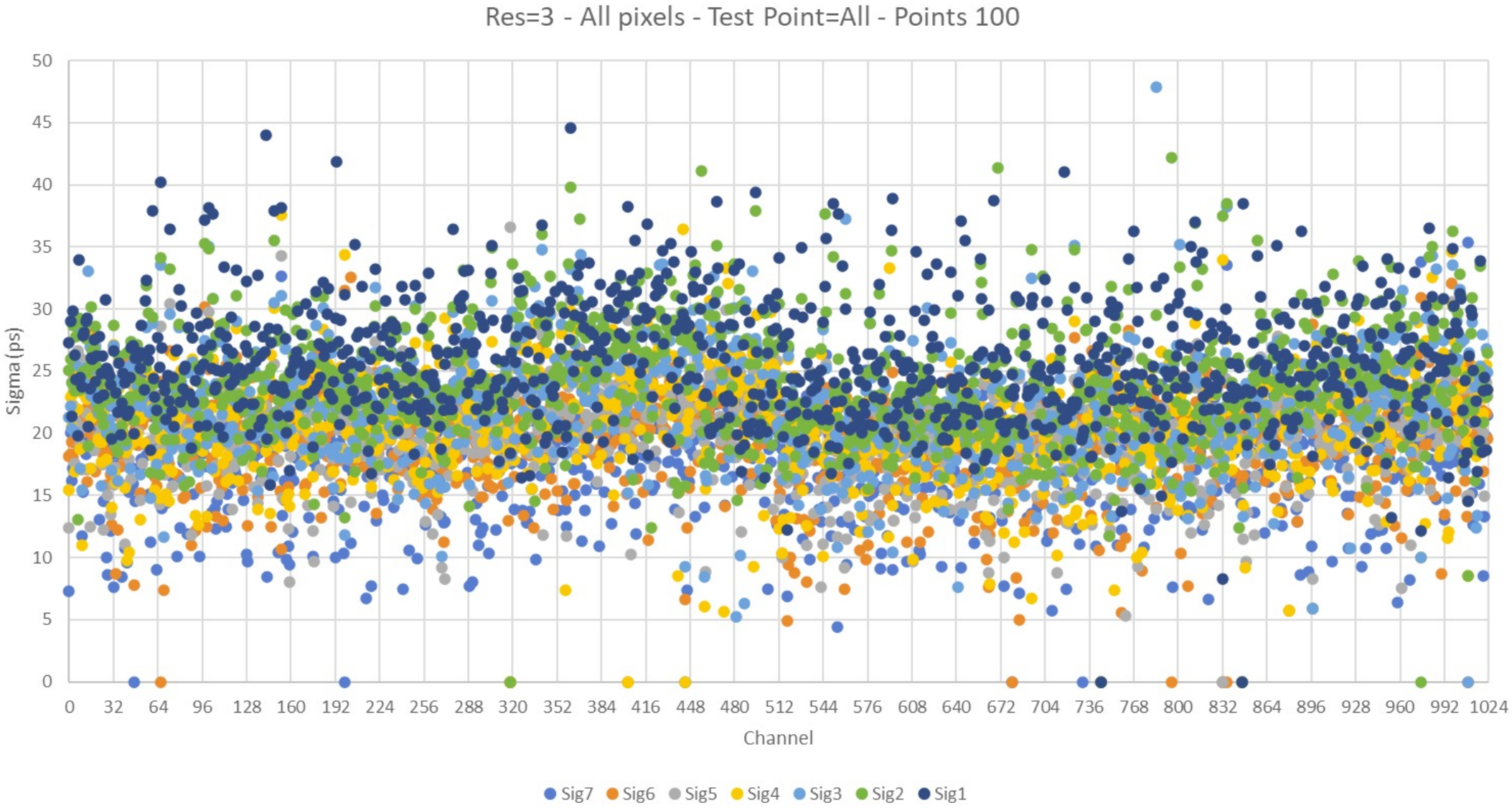



(modified)Timespot1
Matrix (32x32)

# Insights




- **Future advancement → minor tweaks on the current architecture could lead to a resolution better than 30 ps.**
- **Improve core discriminator.**
- **Implement a reset transistor.**
- **Improve the threshold setting switch.**




**Distribution of sigmas depending on channel position and pulse phase (1 to 7)**

S. Cadeddu, INFN Cagliari