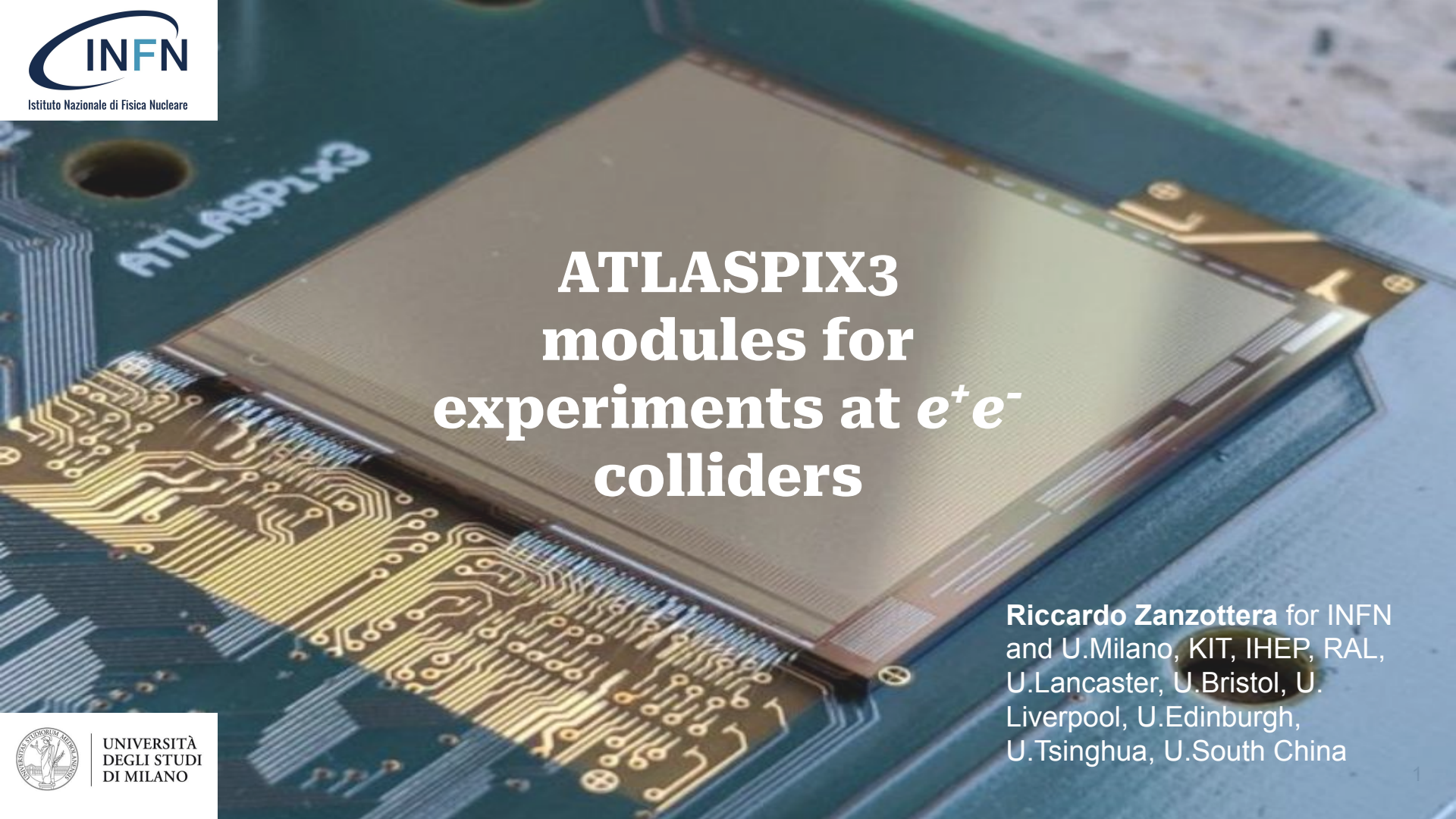


ATLASPIX3 modules for experiments at e^+e^- colliders

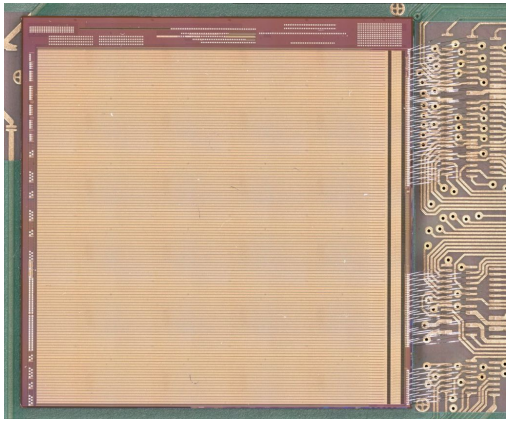
Riccardo Zanzottera for INFN and U.Milano, KIT, IHEP, RAL, U.Lancaster, U.Bristol, U. Liverpool, U.Edinburgh, U.Tsinghua, U.South China

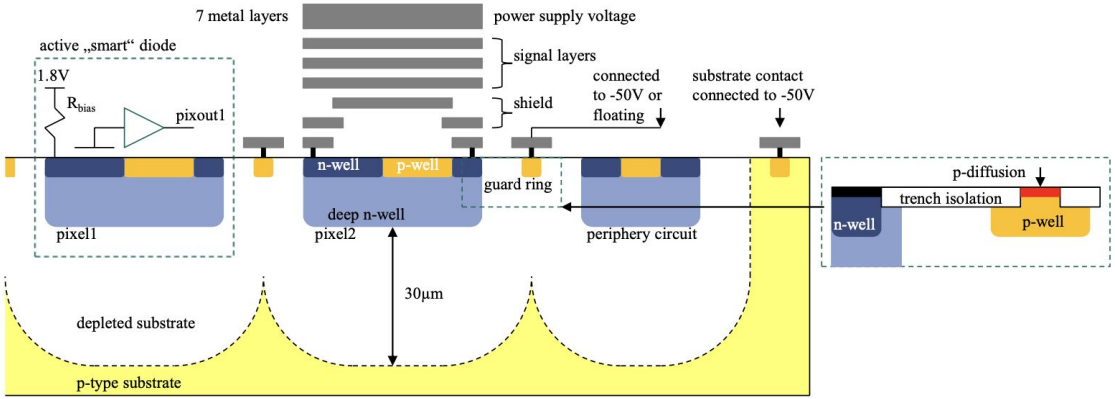
Outlines

- ATLASPIX3
  - general features
  - quad modules
  - serial powering
- Detector concept for e^+e^- colliders
  - system considerations
  - mechanical system

ATLASPIX3 - Features

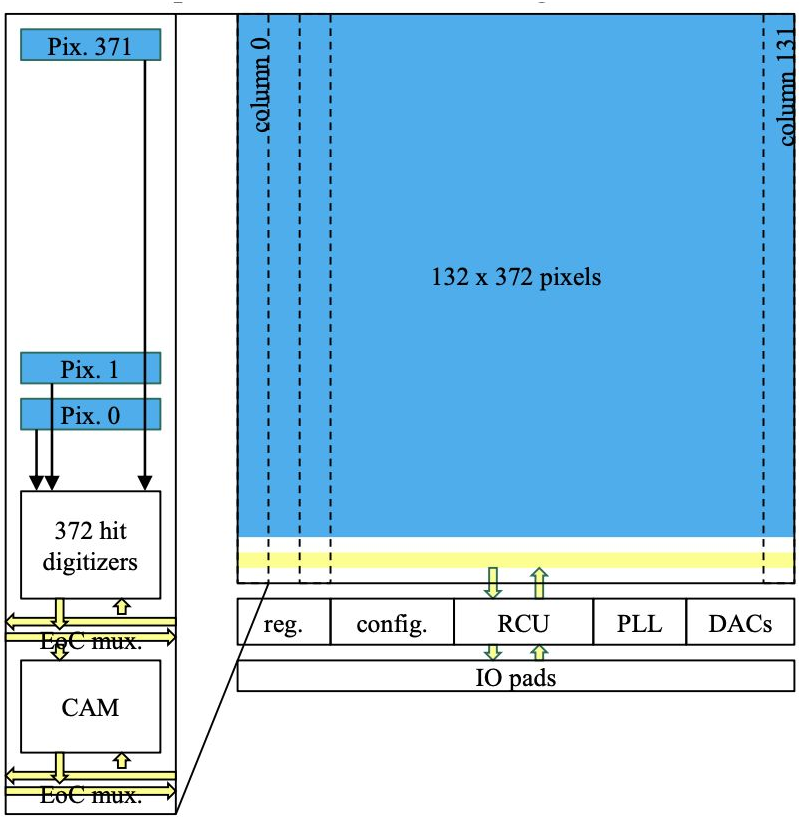
- **ATLASPIX3 general features**
  - Depleted Monolithic Active Pixel Sensor (**DMAPS**)
  - **HVCMOS** technology
  - full-reticle size **20×21 mm²** monolithic pixel sensor
  - **TSI 180 nm process** on 200 Ωcm substrate
  - **132 columns of 372 pixels**
  - **pixel size 50×150 µm²** (25×150 µm² on recent prototypes)
  - **breakdown voltage ∼-60 V**
  - up to **1.28 Gbps downlink**
  - **25 ns timestamping**
- **INFN**, **KIT**, **China, UK** collaboration





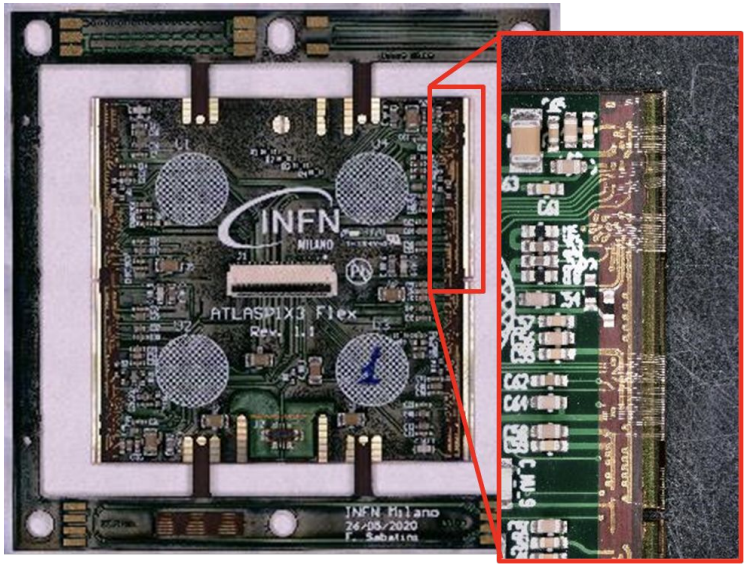
ATLASPIX3 - Chip architecture

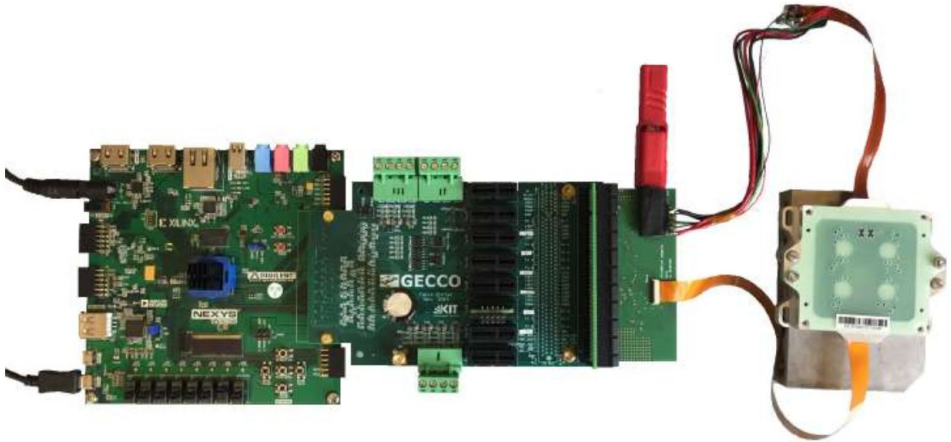
- **Chip architecture**
  - organized in 132 columns, each with 372 pixels, **372 hit digitizers** (HDs), **80 content addressable memory cells** (CAM) and **two end-of-column multiplexers** (EoC mux)
  - **digital part** (HDs, CAM, EoCs) in **chip periphery**, separated from analog pixels electronic (CSA and comparator)
  - chip periphery also contains the readout control unit (RCU), the clock generator, configuration registers, DACs, linear regulators and IO pads
  - **triggerless** and **triggered** readout
    - two EoCs
    - 372 hit buffers for triggerless RO
    - 80 trigger buffers for triggered RO



ATLASPIX3 - Quad modules

- **Multi-chip** module **assembly**
  - aggregates electrical services and connection for multiple sensors
  - **quad module, inspired by ITk pixels**
  - implemented **interface to readout system**
  - developed **software for module**

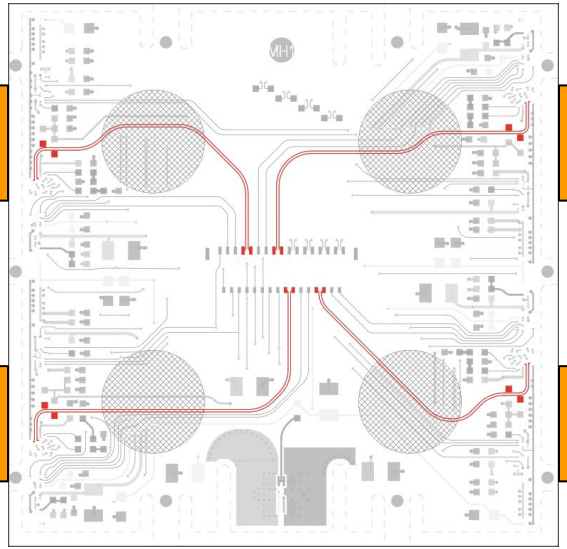




ATLASPIX3 Quads - Flex topology

4 LAYERS STACK-UP

OUTPUT lines TOP layer



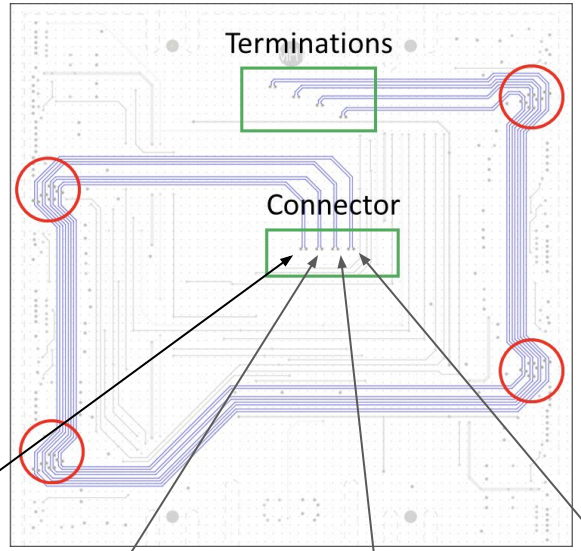
C1_DataOut
L = 26.5 mm

C2_DataOut
L = 30 mm

C3_DataOut
L = 29 mm

C4_DataOut
L = 24 mm

INPUT lines INNER layer



ExtTrigger
L = 125 mm

CkExt
L = 134 mm

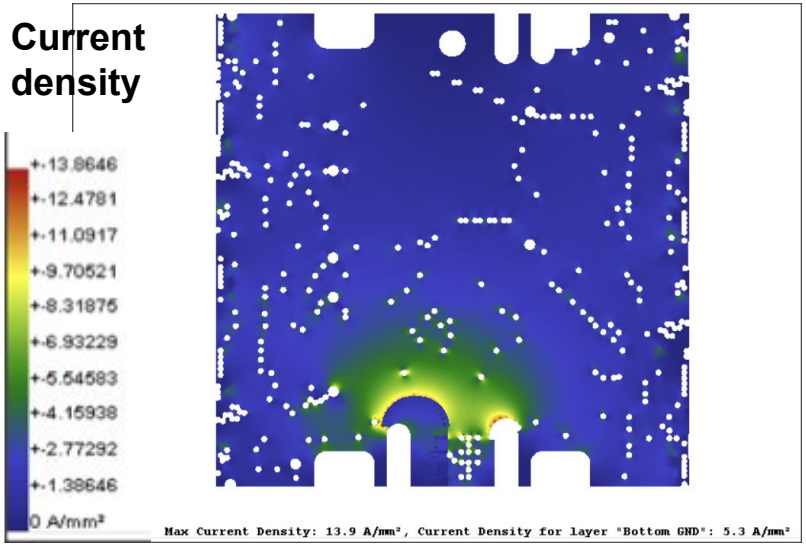
Cmd
L = 139 mm

SynRst
L = 146 mm

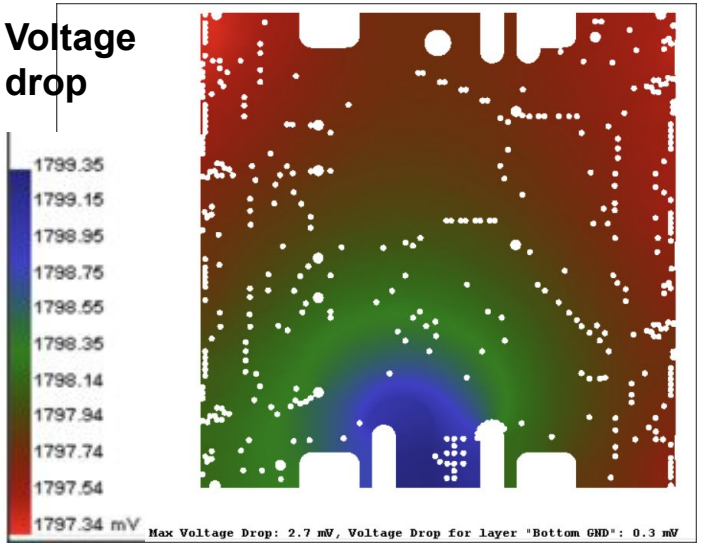
ATLASPIX3 Quads - Flex Power integrity

- **Power Integrity simulation** for VDD (GND as reference)
  - max Voltage Drop 2.7mV
  - max Current Density 13.9A/mm^2
  - max Via Current 137.0mA
  - **“circular” arrangement of the Vias to minimize current density**

Current density

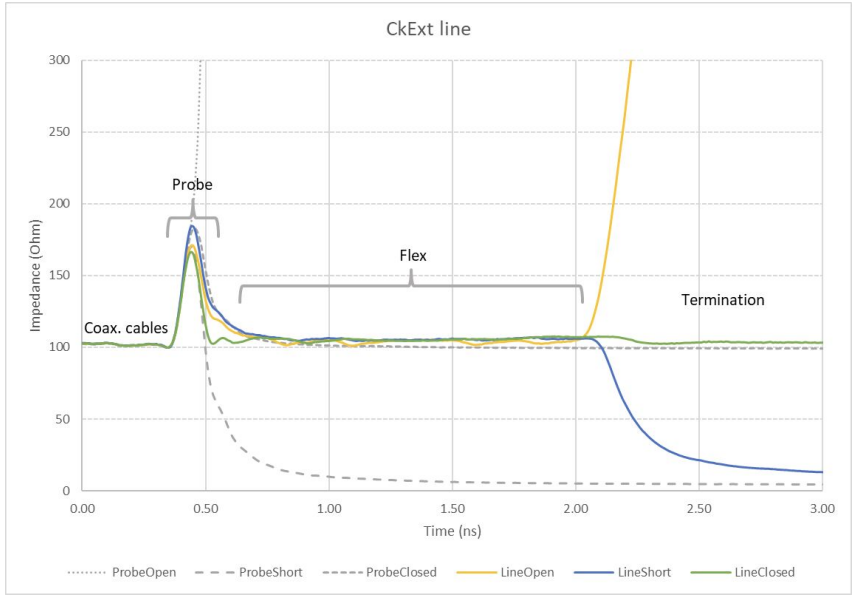


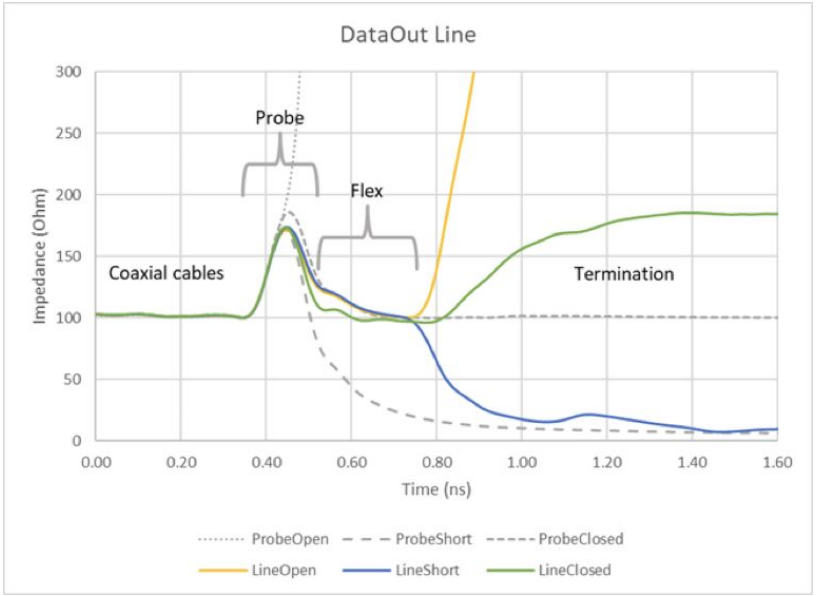
Voltage drop



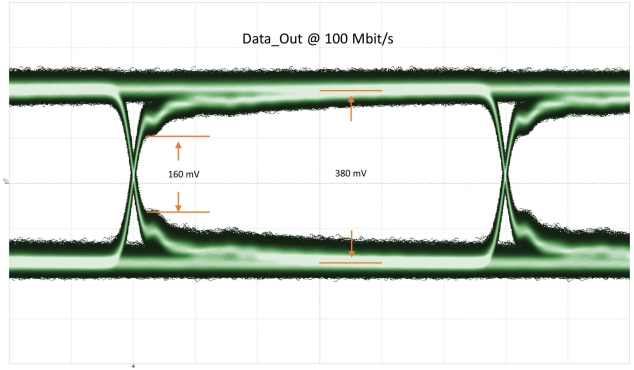
ATLASPIX3 Quads - Flex Impedance

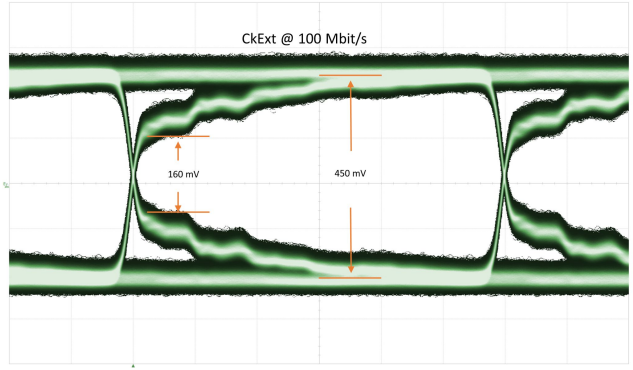
- **Flex impedance**
  - measurements with **TDR**
  - **CkExt** line (Input line)
  - **DataOut** line (Output line)
  - 100 Ω Stack-Up impedance as designed

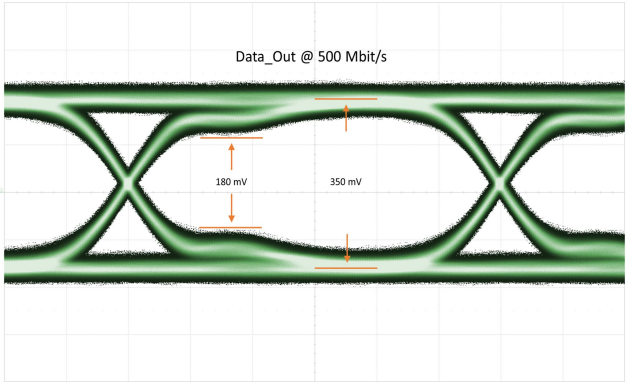


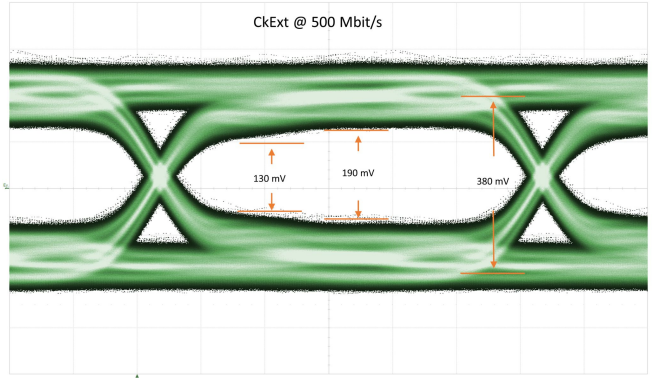


ATLASPIX3 Quads - Flex Eye diagram





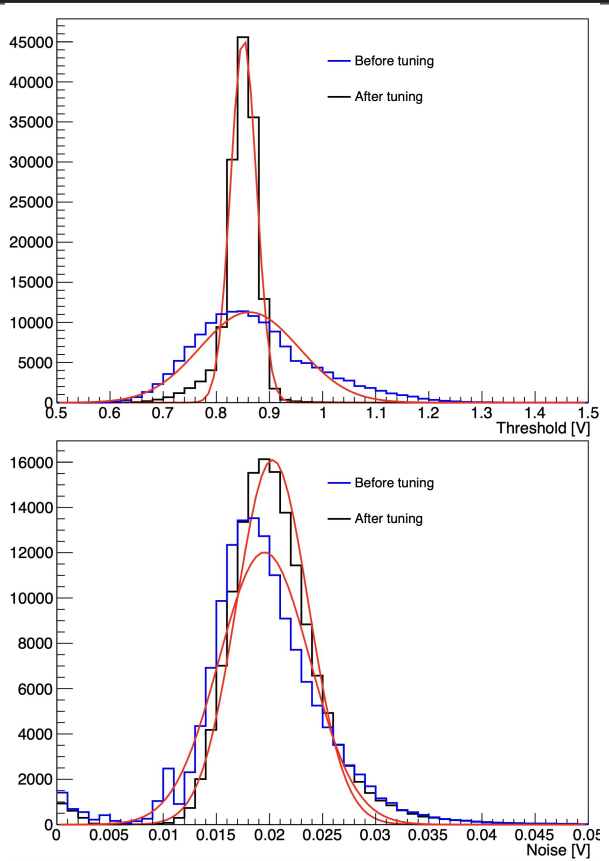




- **Eye diagram** for CkExt and DataOut
  - at 100/500 Mbit/s and 400 mV
  - **good opening** for **Output** lines
  - **opening less +/- 100 mV** for **Input** lines at **high frequency**

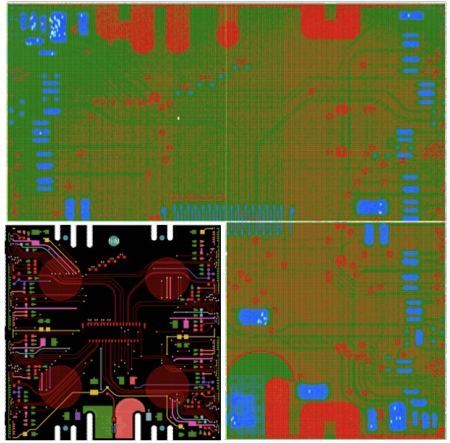
ATLASPIX3 Quads - Threshold and Noise

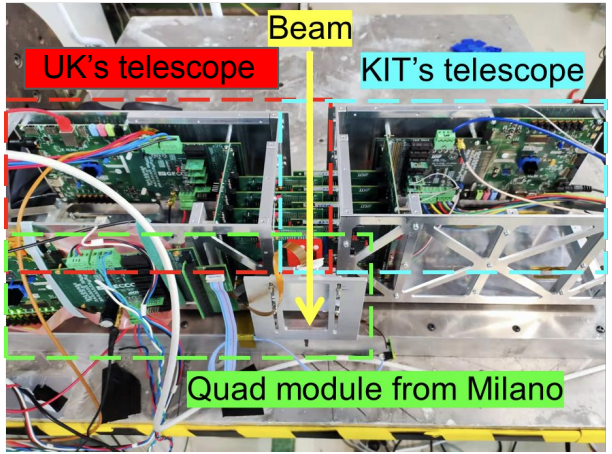
- **Test signal circuit** in chip periphery
  - injection of determined charge in n-well
  - discharge of a metal capacitor
  - regulated by an **on-chip DAC with 8 bits**
- **Tuning circuit**
  - **3-bit** differential current-steering **DAC**
  - SRAM cells to store the DAC value
- **Thresholds and noise measurements** with S-Curve method
  - mean threshold 870 mV (~2500 e-)
  - threshold dispersion from 100 mV to 20 mV after tuning
  - mean noise 20 mV (~60 e-)

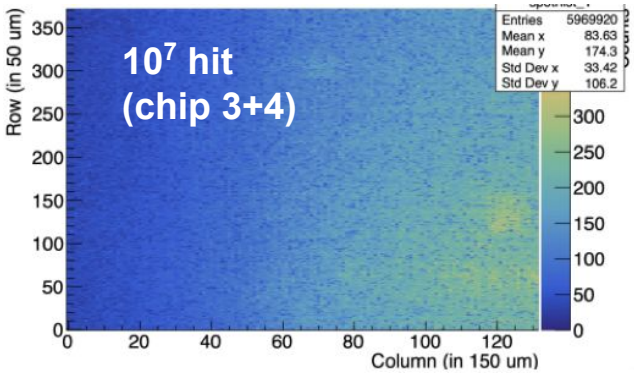


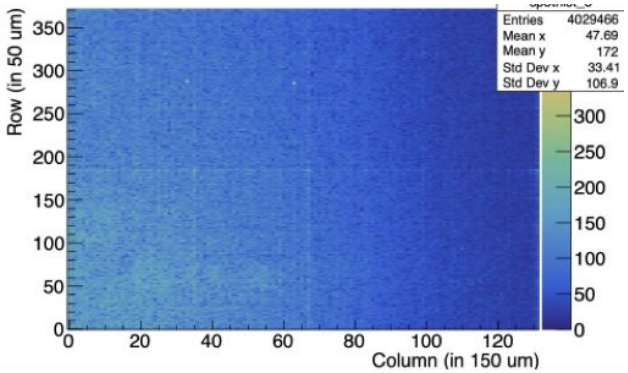
ATLASPIX3 Quads - Operation test

- Amptek Mini-X2 with silver anode, max energy 50 kV
  - Rate range: ~1.5 x 10^4 hits/s to ~ 3.4 x 10^4 hits/s
  - Components on the PCB can be easily identified
- Two modules used for the **testbeam** 4-10 april at **DESY**
  - Module's **operativity demonstrated**
  - telescope results in **poster "First Results of ATLASPix 3.1 DESY Testbeam"**



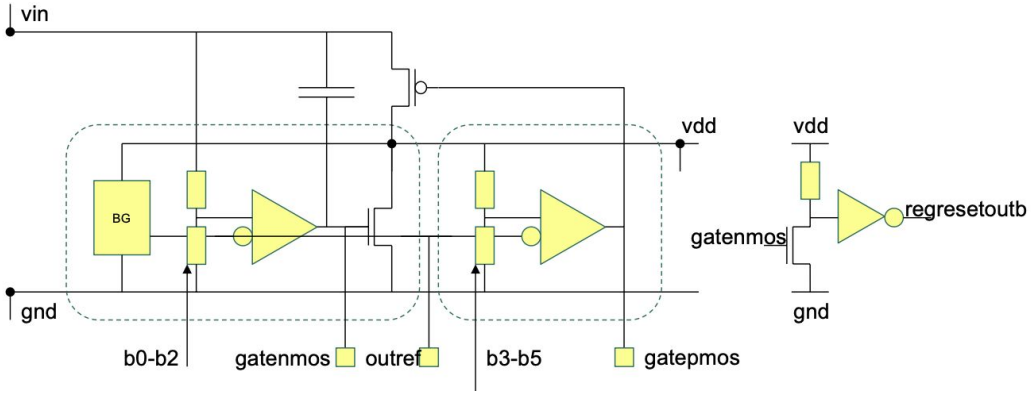






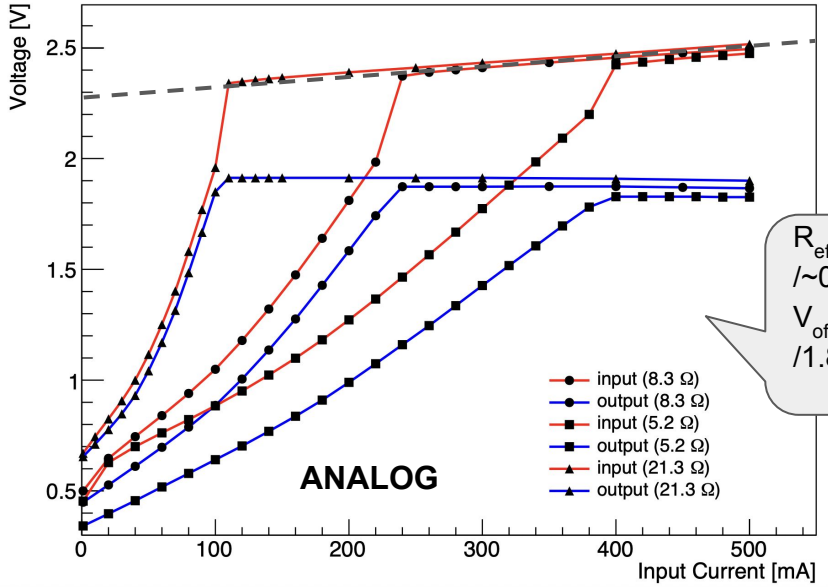
ATLASPIX3 - Serial powering

- Version **ATLASPIX3.1** has possibility for **serial powering** through **two shunt/low dropout regulators**
  - **digital** and **analog** (VDDD/A)
  - **3 bits** to tune threshold of shunt regulator
  - **3 bits** to tune VDD
  - gatenmos, outref, gatepmos are for monitoring
  - regresetoutb can be used as power on reset
- Possibility to use a **single power supply for all the 6 alimentation needed to operate the chips**



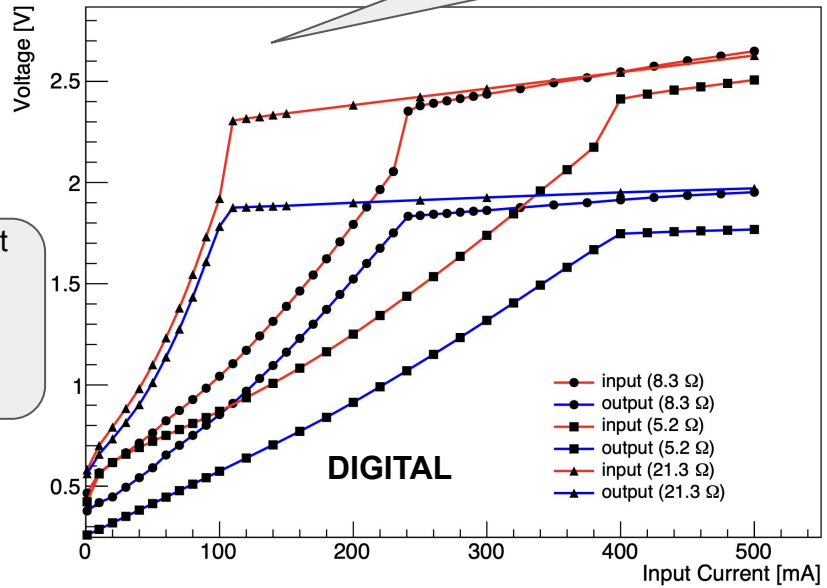
ATLASPIX3 - Serial powering

- **Turn-on curves** (input and output) for digital and analog regulators
- **Different external resistive loads**
- Linear part after the power on fitted with $V_{off}+I*R_{eff}$
- Ideal $R_{eff}\sim 0\ \Omega$, $V_{off}\sim 2$ V for input, ~ 1.8 V for output

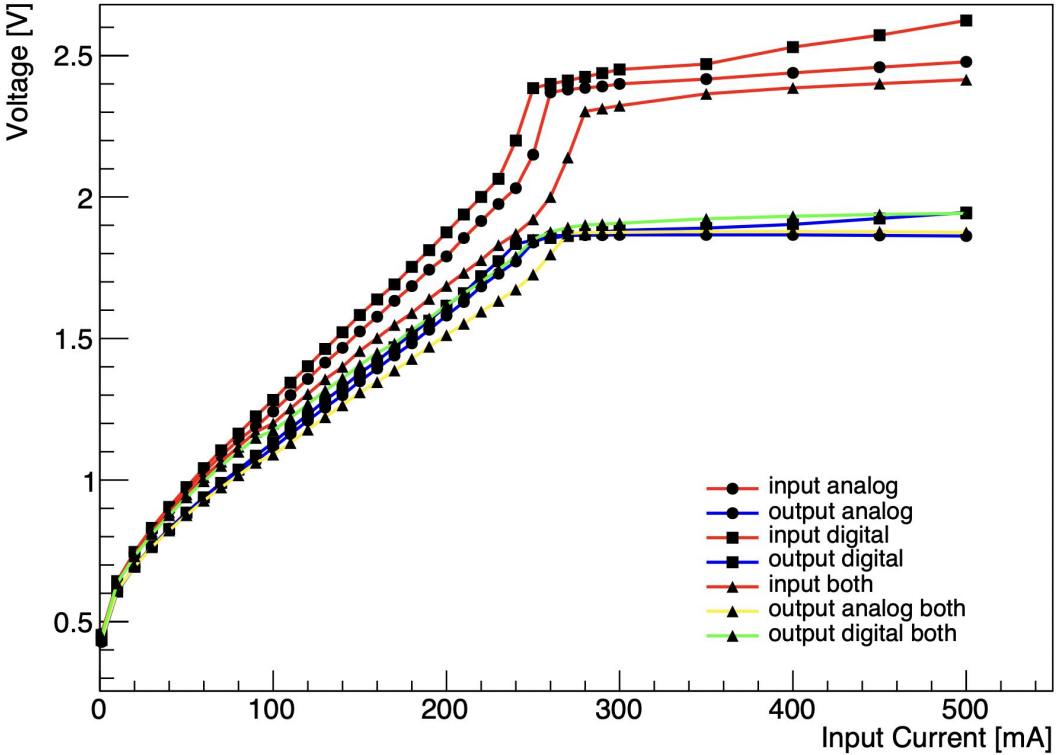


R_{eff}0.43-0.51 Ω input /~0 Ω output
V_{off} 2.22-2.3 V input /1.84-1.92 V output

R_{eff}0.8-1.1 Ω input/ 0.2-0.5 Ω output
V_{off}2.05-2.22 V input/ 1.67-1.85 V output



ATLASPIX3 - Power consumption



- Analog and digital regulators output connected to the chip
- Full chip **turn-on**
  - **∼300 mA**
- **Input voltage**
  - **∼2.3 V**
- **Power consumption**
  - **∼690 mW/chip**
  - **∼175 mW/cm^2**

e+e- Detector Requirements

Physics process		Detector system	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) =$ $2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV})\sin^{3/2}\theta}$
$H \to b\bar{b}/c\bar{c}/gg$	$\mathrm{BR}(H \to b\bar{b}/c\bar{c}/gg)$	Vertex	$\sigma_{r\phi} =$ $5 \oplus \frac{10}{p(\mathrm{GeV})\times\sin^{3/2}\theta}(\mu\mathrm{m})$
$H \to q\bar{q}, WW^*, ZZ^*$	BR(	L L	$\sigma_E^{\mathrm{jet}}/E =$ $3 \sim 4\%$ at 100 GeV
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\Delta E/E =$ $\frac{0.20}{\sqrt{E(\mathrm{GeV})}} \oplus 0.01$

high precision measurements at end of tracking volume

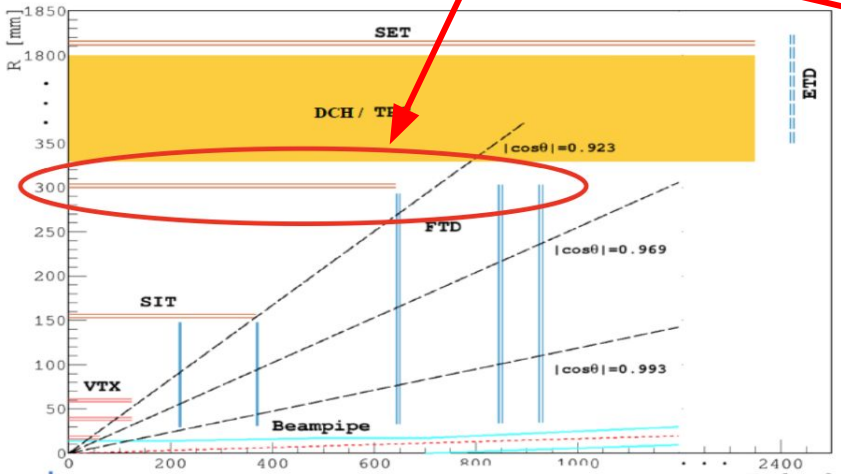
finely segmented vertex detector

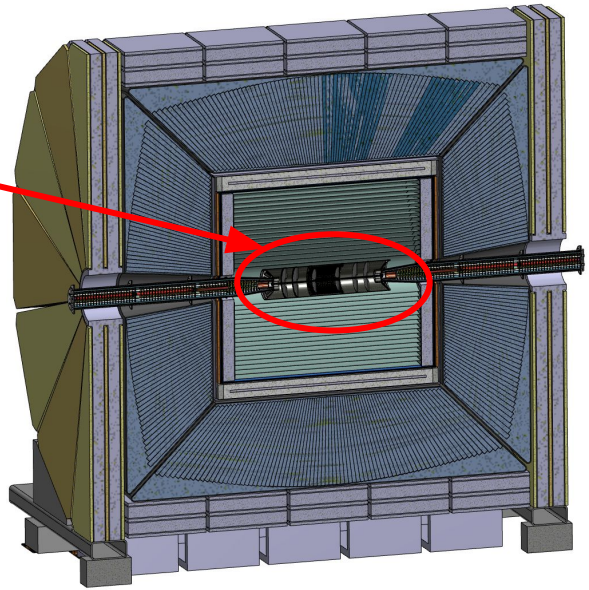
challenging requirements on detector material

- Similar approaches for ILC, CLIC, FCCee, CepC:
  - High resolution **pixel vertex detector**
  - Either **full silicon tracker** or **central gas chamber+Si wrapper**

Detector concepts

- **Different detector concepts**
  - **CEPC CDR baseline** concept
  - **IDEA** concept
- **ATLASPIX3** is suitable for **tracker layers in front of the Central Gas Chamber** and **silicon wrapper outside the Central Gas Chamber**
- **Different mechanical approaches for internal silicon layer**
  - long-stave structure for CEPC
  - double layer stave structure for IDEA



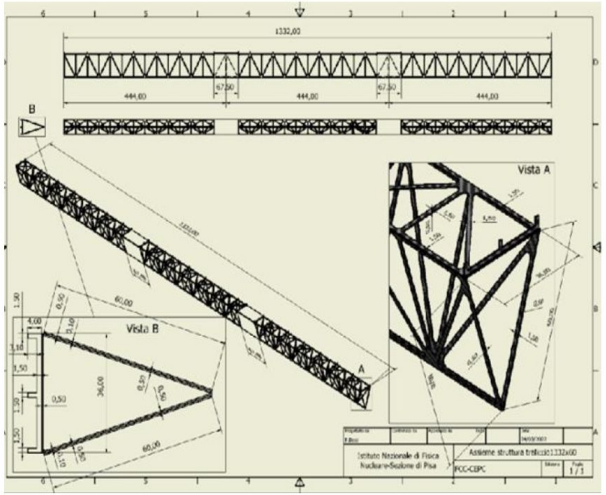


ATLASPIX3 - System considerations

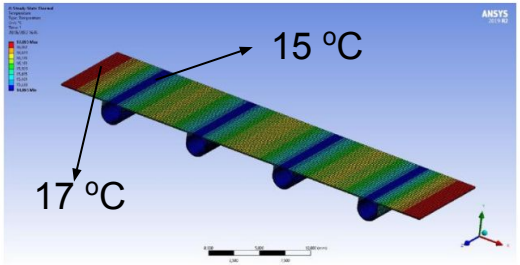
- **Complete system consists of 900.000 cm^2 area / 4 cm^2 chip = 225k chips (56k quad-modules)**
  - aggregation of several modules for data and services distribution is essential
  - inner tracker will be 5--10% of this
- **Data rate** constrained by the inner tracker
  - average rate 10^{-4} - 10^{-3} particles cm^{-2} event^{-1} at Z peak
  - assuming 2 hits/particle, 96 bits/hit for ATLASPIX3
  - **640 Mbps link/quad-module** (assuming local module aggregation) provides ample operational margin
  - 16 modules can be arranged into **10 Gbps fast links**: **3.5k links**
    - can also assume 100 Gbps links will be available: 350 links
- **DAQ architecture**
  - **triggerless readout** will fit the data transmission budget but requires off-chip re-ordering of data
  - **triggered readout** will be **simpler** and would also reduce the bandwidth occupancy
- **Power consumption**
  - ATLASPIX3 power consumption **170 mW/cm^2** with serial powering
  - 680 mW/chip → 2.7 W/module → **total FE power 150 kW**
  - additional power for on detector aggregation and de-randomizations **~2W/link**

CEPC CDR baseline - Long-stave design

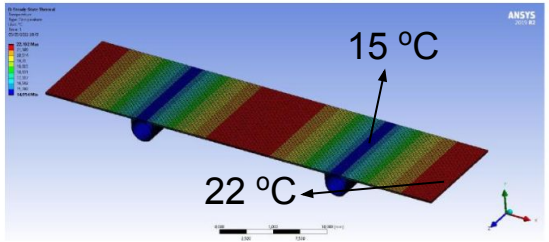
- **Very long stave structure**
  - **1330 mm** long
  - **triangular truss shape from water jet cutting** (similar developments as for Belle II upgrade studies)
  - **glued together three single structures**
  - **FEA of structure rigidity: gravitational sag about 100 µm**
- Simulated **two different cooling solutions**
  - **2 pipes** (0.3% X_0)
  - **4 pipes** (0.4% X_0)
- **Prototype** actually i**n construction**

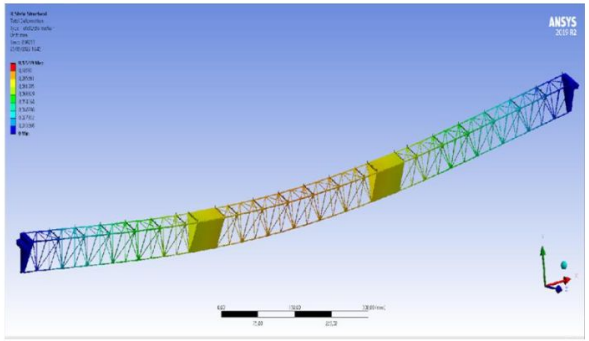


4 pipes 0.4% X_0

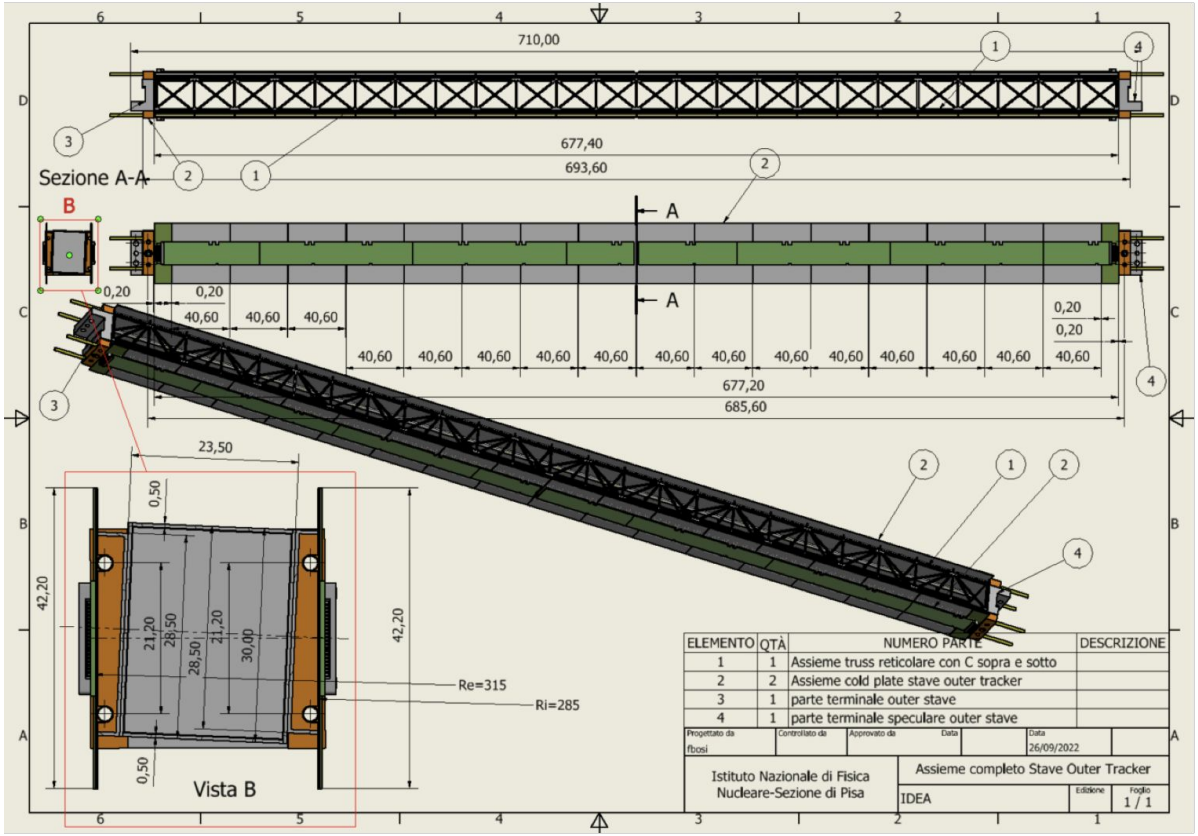


2 pipes 0.3% X_0





IDEA - Stave design

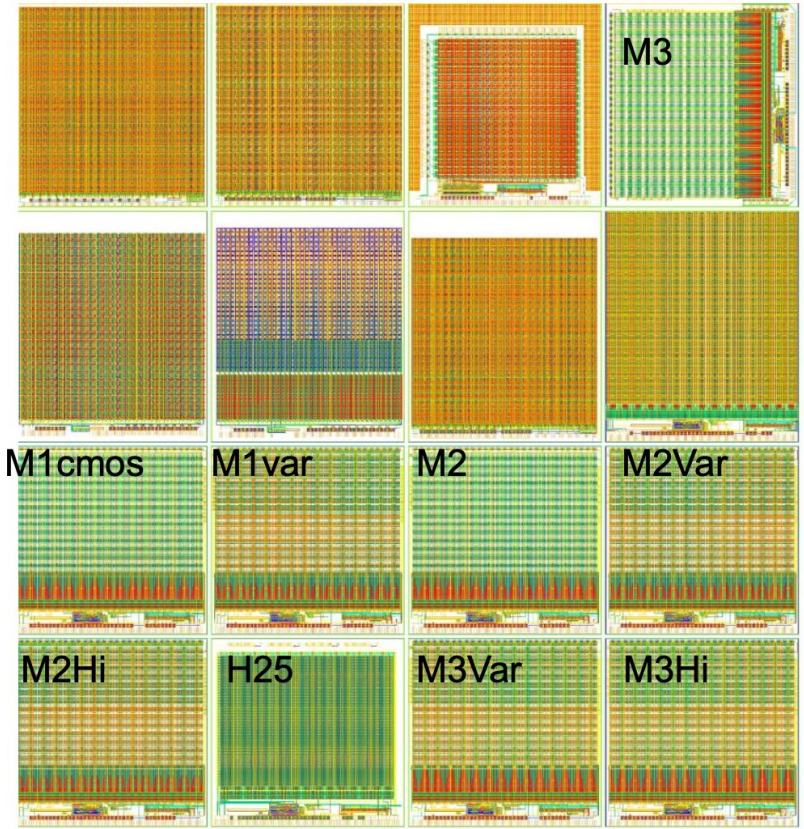


- **Shorter stave structure**
  - **rectangular truss shape**
  - **double layer**
  - **32 quads** modules per stave
  - cooling with **4 water pipes** per stave
- **Outer barrel structure**
  - **48 staves**
  - inner layer at 28.5 cm
  - outer layer at 31.5 cm
  - supported by the Drift Chamber
  - designed for **power budget** of **~2.63 kW**
- **Design is being finalized**

Conclusions and perspectives

- **ATLASPIX3** is a **full size detector** providing **most of the features needed by e+e- experiments**
- Deployment on a **real detector system requires the aggregration of data and services**, for this purpose **multi-chip modules have been realized and successfully tested**
- Further integration requires to be able to **chain multiple modules using the same serial-powering concept developed for the silicon trackers for HL-LHC**
- **Early tests on the shunt regulators implemented on the ATLASPIX3.1 chips are encouraging and make possible to proceed to a redesign of a module concept based on serial powering and the building of multi-module chains suitable for CepC and FCCee accelerators**
- **A prototype of the stave structure designed for CepC inner tracker is in construction**

Future chip developments



- **Improved sensor prototypes**
  - **Smaller pixel pitch**
  - **Less power consumption**
  - **different comparator and amplifier types**
- Design of **HLMC 55 nm HVCMOS technology**
- Design of **a chip to chip data transmission** to be used in quad modules to further reduce material

Thanks for the attention!