Monolithic Stitched Sensor (MOSS) Development for the ALICE ITS3 Upgrade

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On behalf of the ALICE Collaboration

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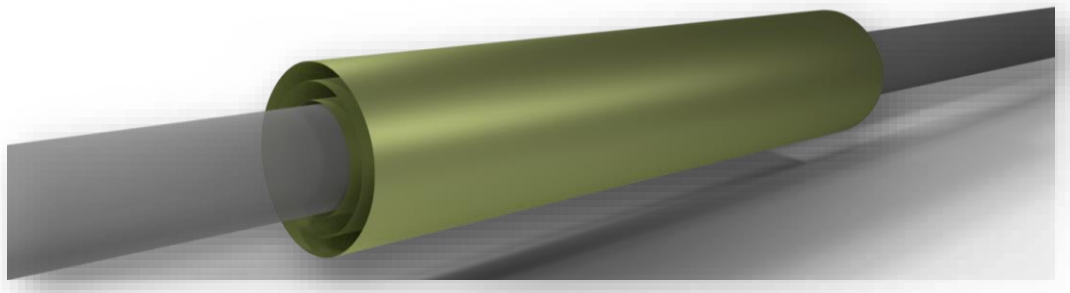
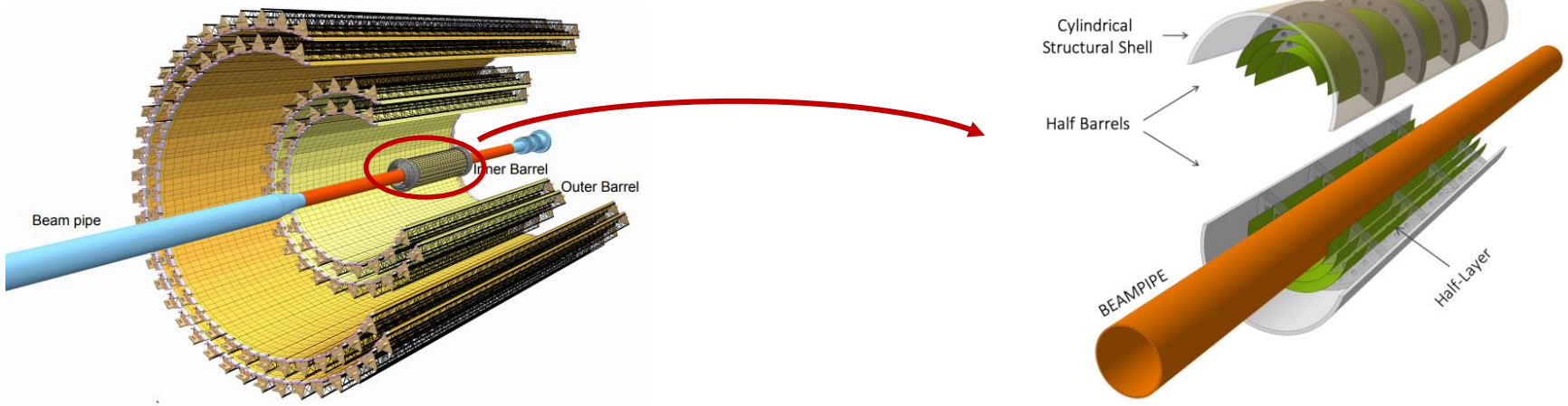


Overview

- Motivation
- MOnolithic Stitched Sensor (MOSS) prototype and challenges
- MOSS power plan and pad ring design
- Summary and outlook

ALICE ITS3 upgrade



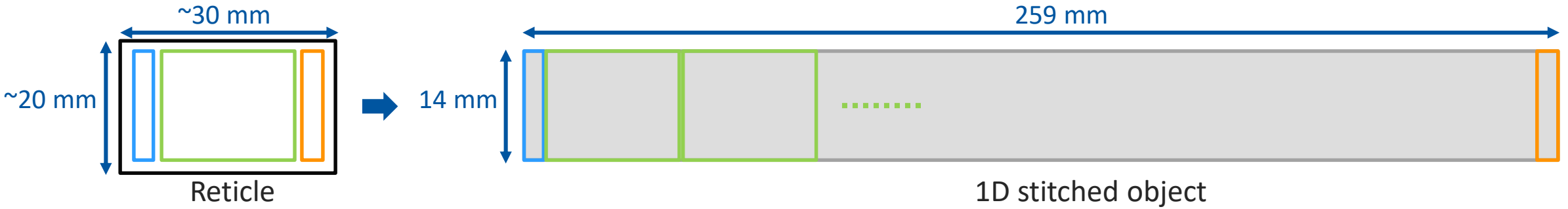
- ALICE (A Large Ion Collider Experiment) ITS2 (Inner Tracking System) to ITS3
  - **Wafer-scale bendable monolithic CMOS particle sensor measuring up to 270mm x 94mm**
  - Less and homogeneous material leads to better results for physics
    - Bent Si wafer alone allows a stable and self-supporting mechanical structure; Wafers thinned down to about 50um are bendable
    - No circuit board required for electrical connection
    - Cooling by air flow; power density limit is 20 mW/cm^2
  - 6 large sensors make up the entire ITS3 production
  - First application of stitching technology in high energy physics


Dummy silicon model

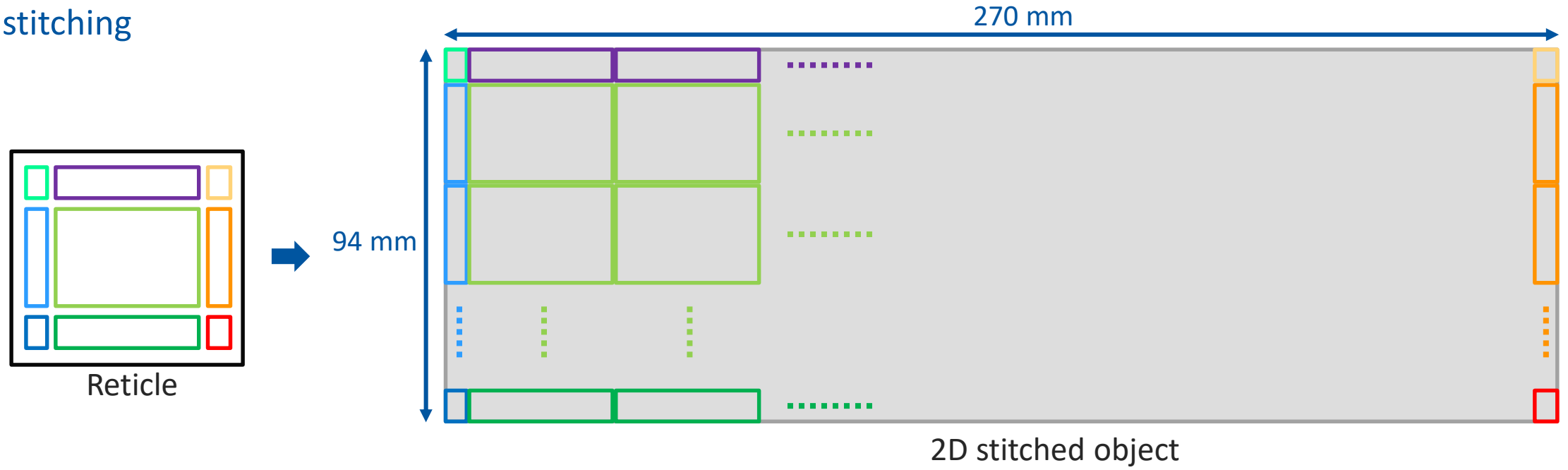
❖ More details on ITS2 and ITS3 upgrade:
Other talks by Valerio Sarritzu, Lukas Lautner, and Andrea Sofia Triolo
https://indico.cern.ch/event/1071914, ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS sensors, Magnus Mager (CERN)
https://cds.cern.ch/record/2703140/files/LHCC-I-034.pdf - Letter of Intent for an ALICE ITS Upgrade in LS3

Wafer scale stitched sensors

- 1D stitching



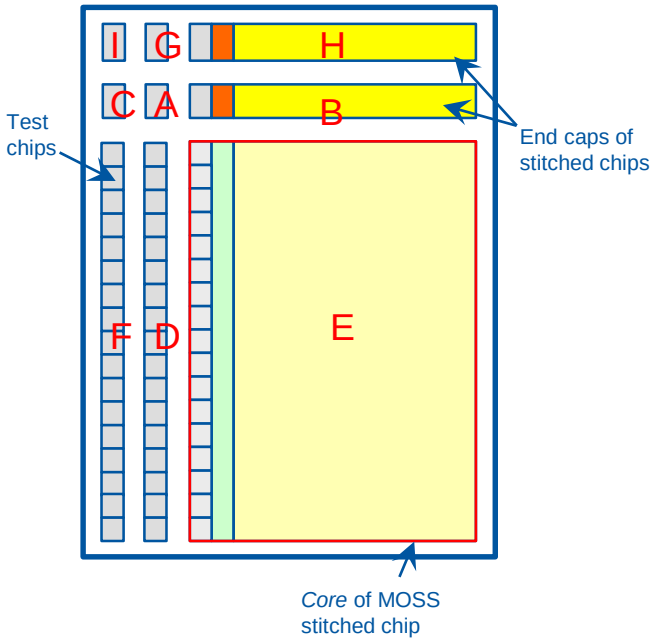
- 2D stitching



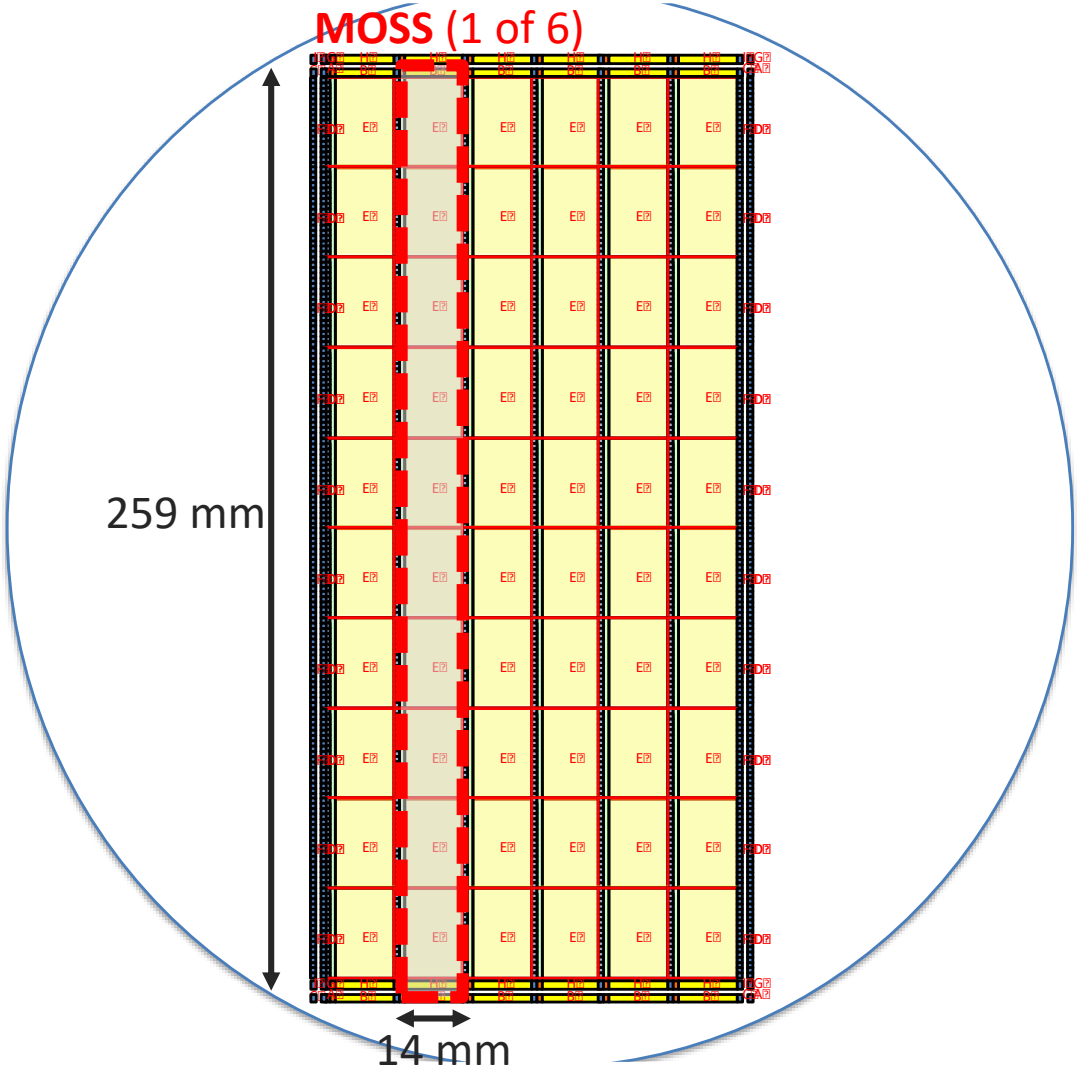
Wafer scale stitched sensors prototype: MOSS

Technology
- TPSCo 65nm Image Sensor CMOS process
- 300 mm silicon wafer
- Stitching technique
- Full wafer-scale sensor design

Design reticle

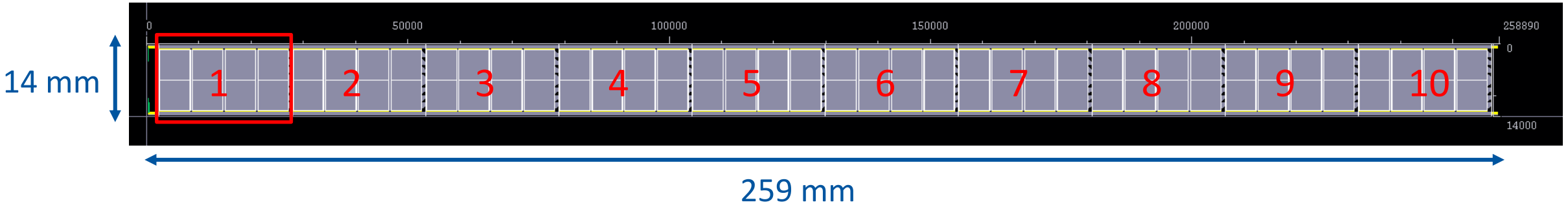


Sensor chips on wafer

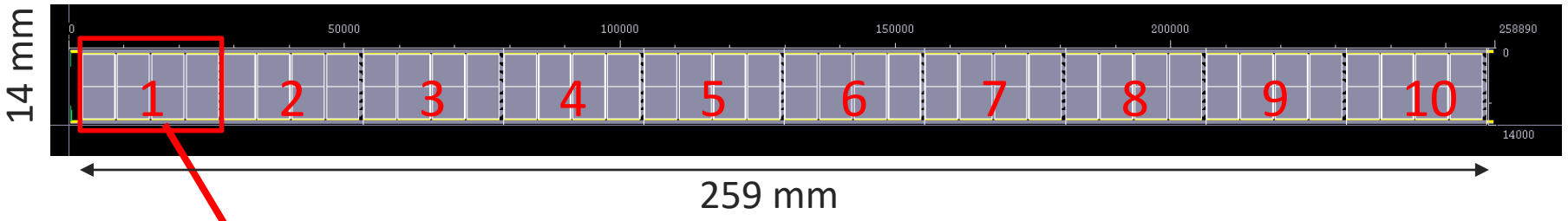


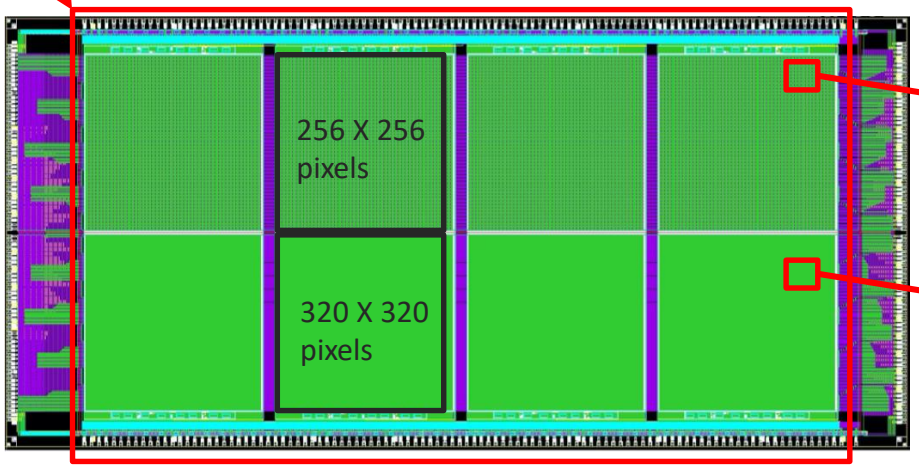
MOSS Monolithic Stitched Sensor Prototype

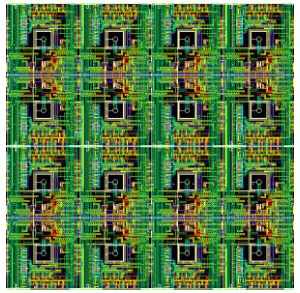
- Primary goal
  - Learn stitching techniques to make a particle detector
  - Learn about yield
  - Interconnect power and signals on wafer scale chip
  - Study leakage, spread, noise, and speed
- Stitched object
  - Left endcap
  - Repeated Sensor Unit x 10
  - Right endcap



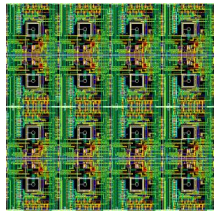
MOSS Monolithic Stitched Sensor Prototype







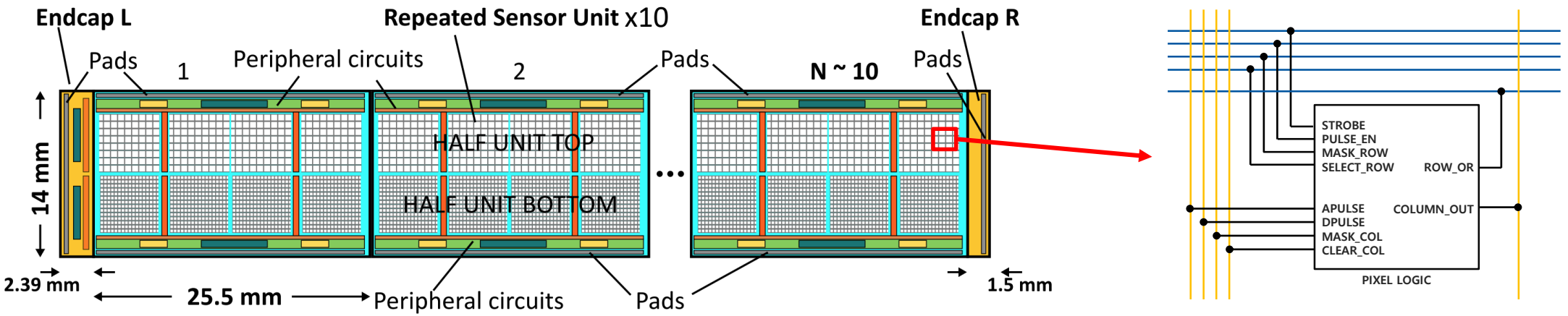
Half matrix top:
- Large pitch 22.5 µm
- Maximized width and spacing of structures for yield
- 7 mW/cm^2 from analog FE



Half matrix bottom:
- Fine pitch 18 µm
- Compact layout
- 11 mW/cm^2 from analog FE

- Main features
  - 14 x 259 mm^2 monolithic stitched sensor
  - 6.72 million pixels
  - 736.3 million transistors
  - 30 nA nominal static current of analog front-end
  - Negative bias to the substrate

MOSS Monolithic Stitched Sensor Prototype



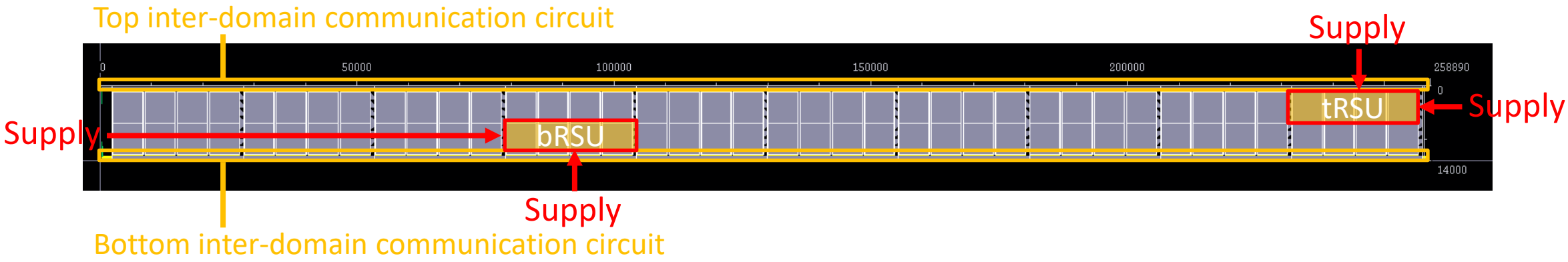
- Binary readout with parameterizable strobe duration
- In-pixel latch with fast OR for row and column output signals
- Zero-suppressed readout; sequentially encode address of pixels with hit
- Analog charge injection and digital pulse testing per pixel
- Masking features

Challenge arising from stitching: Yield

- How to learn about yield?
  - Architecture for resilience to manufacturing faults
    - Granular powering scheme to avoid that a single fault kills the full chip
    - Testing sub-units independently
  - Layout
    - Matrix designed with design-for-manufacturing (DFM) rules
      - Maximizing all width and spacing whenever possible
      - Multiple vias
    - Periphery designed with custom DFM standard cell library

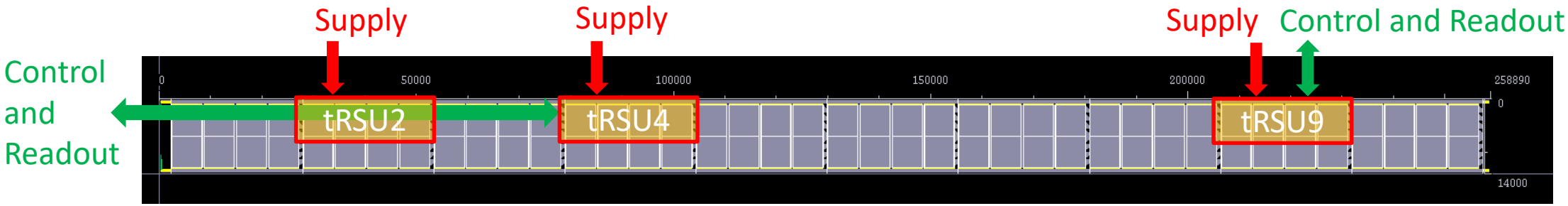
MOSS power plan

- Power granularity
  - Design is divided in 20 sectors (top and bottom RSU) that can be powered and operated independently
  - Any sectors that have fatal short can be turn OFF while others are operative
  - Each sector has analog and digital core and IO domain
  - Two additional domains for each inter-domain communication circuit at top and bottom
  - One global net for the substrate bias
  - In total, 65 power domains
- Power from Short edge (Left Endcap) and/or Long edge

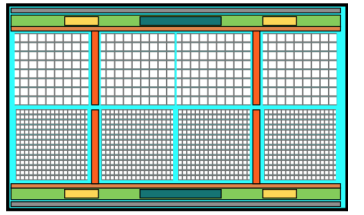


Measuring Yield

- An example of MOSS testing scenarios
  - Top RSU2 and RSU4 are controlled and read out through the top inter-domain communication circuit and the left endcap
  - RSU9 is electrically disconnected from the top inter-domain communication circuit
  - RSU9 is controlled by means of the long edge
  - All the other domains are off

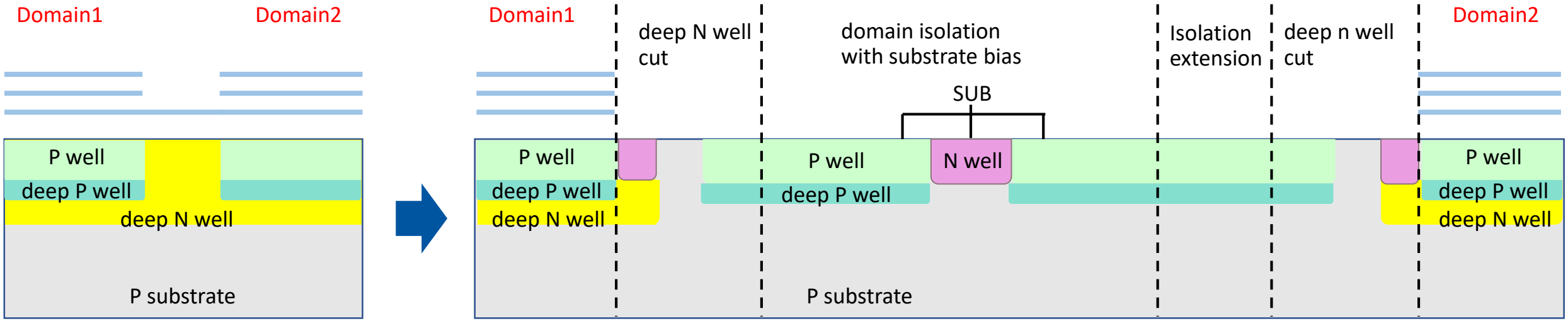


- Study manufacturing yield
  - Functional yield at half chip, half RSU, matrix, column/row/pixel level granularity
  - Possible dependence on pixel pitch and layout density



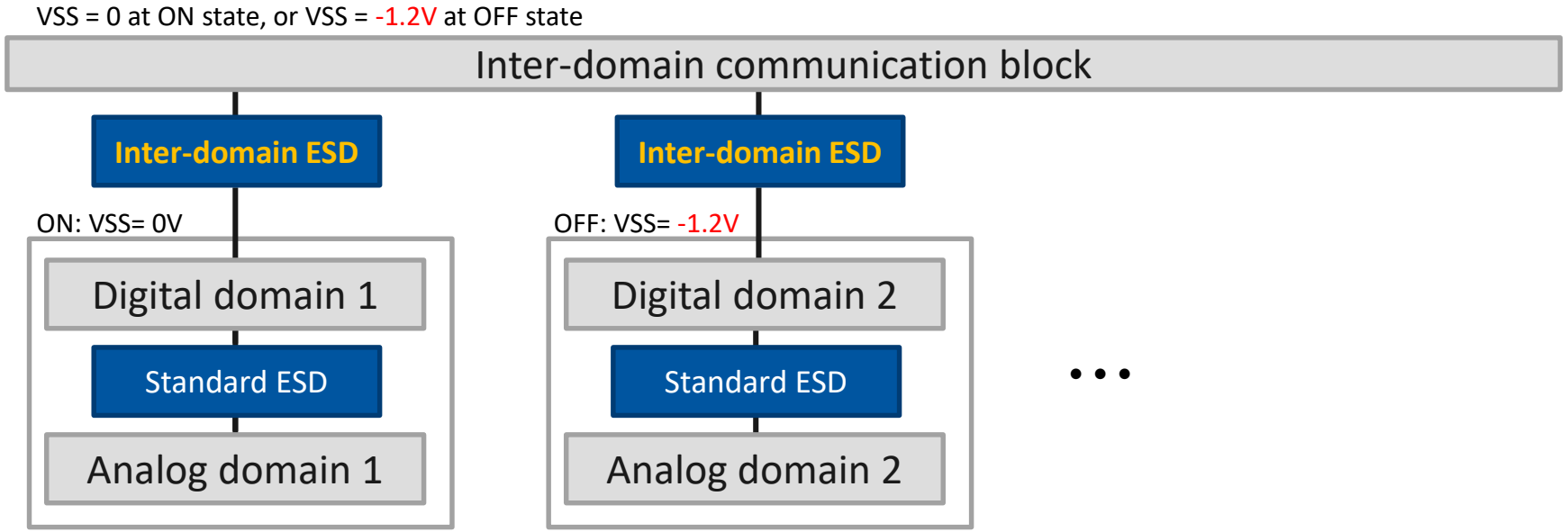
Domain isolation

- Challenges with the standard well structure
  - Domain isolation by separating wells in the substrate
  - Reducing the area of the reverse-biased junction as much as possible
- Pad ring separation cells
  - Deep N well is separated by deep N well cut cell
  - Substrate bias cell in between domains
  - Isolation extension cell to reduce the reverse-biased junction in the domains



ElectroStatic Discharge protection (ESD)

- Challenges with standard ESD structure
  - Standard ESD structure is not compatible with the power plan
  - Off domains are held at a negative voltage equal to the substrate bias
  - The inter-domain communication block must be able to operate while the other domains are off, and vice versa
- Inter-domain ESD between the communication block and the other domains
  - Introduced 4-diode strings as an inter-domain ESD
  - Added power clamp diodes to the inputs of the inter-domain signaling buffer



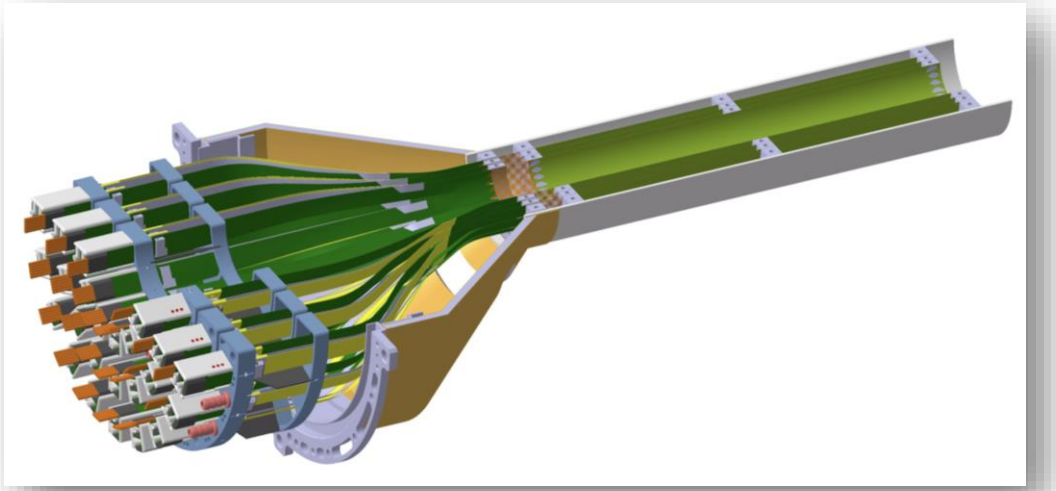
Summary and outlook

- MOSS developed as a proof-of-concept of a stitched monolithic particle detector for ITS3
- Submitted in Nov 2022
- Expected to be ready for testing in June 2023
- Much learning and complex design challenges in order to maximize the yield
  - Power granularity
  - Design-for-manufacturing
  - Domain isolation
  - Inter-domain ESD protection
- Outlook
  - Quantify yield on MOSS by testing
  - Adopt the learning from the testing into the future prototype development
- First ever wafer-scale monolithic CMOS sensor applied to high-energy physics

SPARE SLIDES

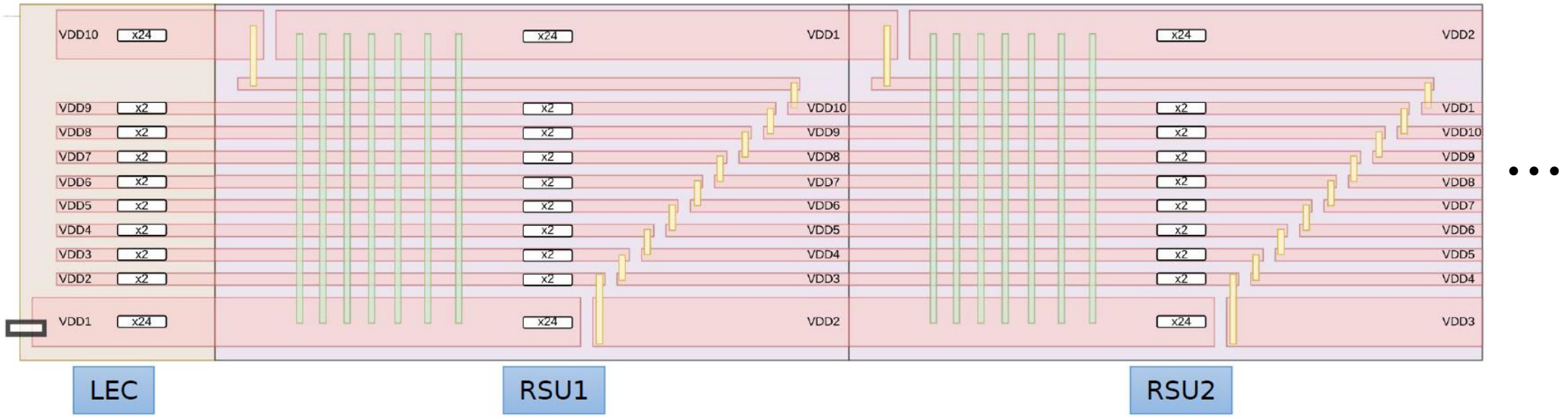
Requirements of flux and radiation levels

Pb-Pb Interaction Rate	50 kHz
Particle Flux	2.2 MHz/cm^2
TID	<10 kGy
NIEL	1×10^{13} 1 MeV n_{eq} cm^{-2}



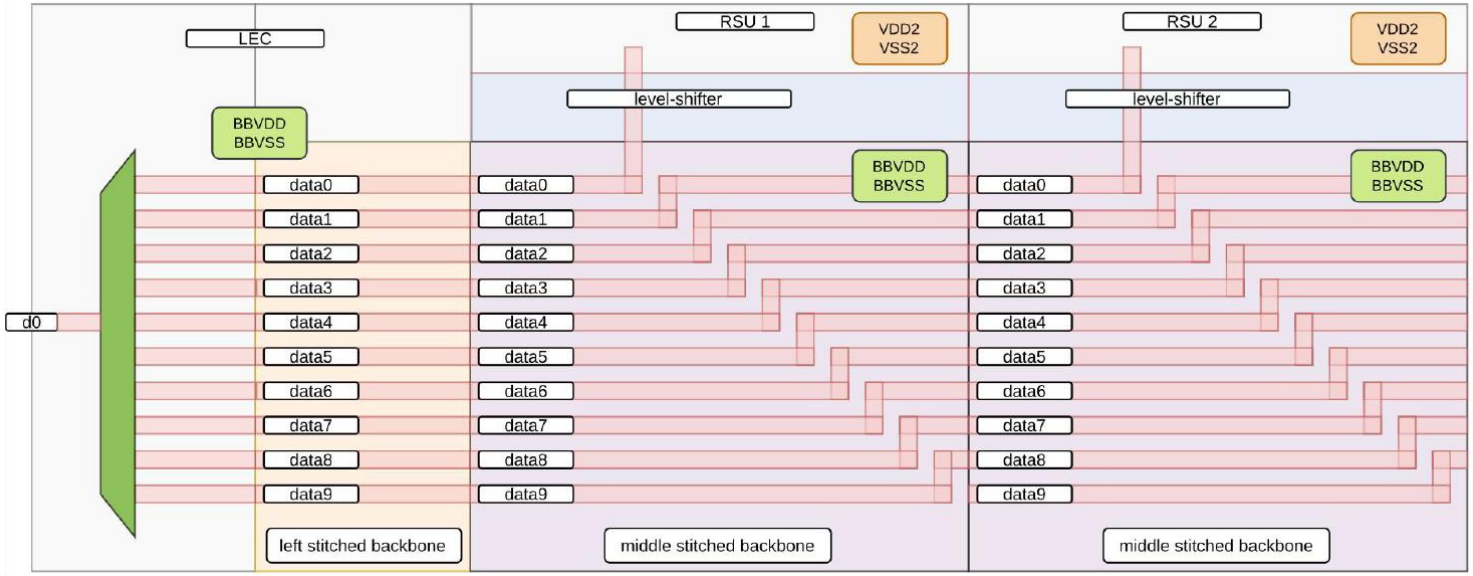
MOSS power distribution

- With the same physical RSU, it is necessary to forward power from the short edges to the most far RSUs
- We achieve this by performing *line-hopping*
- Powering & monitoring from the short-edge (example of VDD)



Data readout through Left Endcap

- Data readout through the inter-domain communication block (Stitched backbone)
  - Readout requests are sent over the serial slow control
  - We can read one RSU at a time (1x15Mbps)
  - Line-hopping allows to connect all 10 RSUs to a mux in the Left Endcap
  - The mux is controlled by means of the slow control



Special readout mode: all RSUs at once (10x 3.75 Mbps)

RSU addressing

- RSU addressing in the inter-domain communication block (Stitched backbone)
  - Each RSU address is set by means of line-hopping in the stitched backbone
  - A local tie-high cell ensures the address increment