Design and timing characterization of radiation-hard circuits for monolithic sensors

Francesco Piro
ESR 12
Sv. Heinz Pernegger
CERN EP-ADE-ID

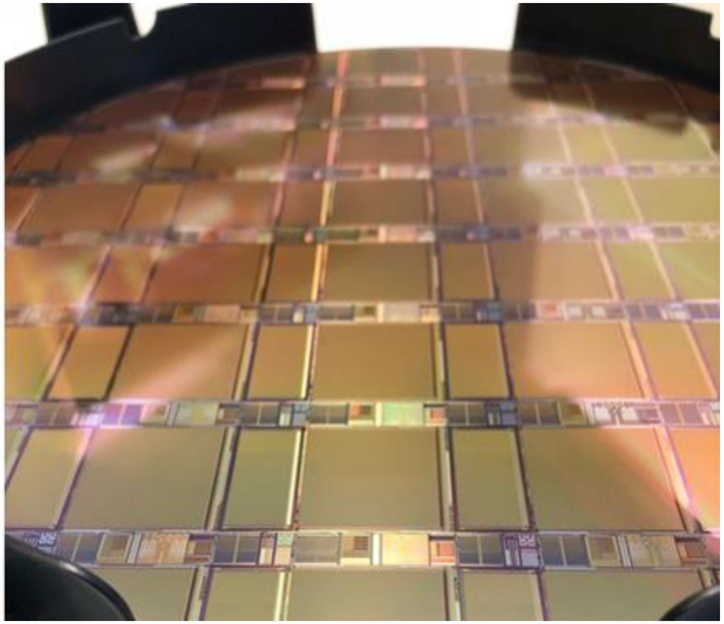
OUTLINE

- **DACs and biasing circuits**
  - Voltage & Current DAC design
  - Measurements

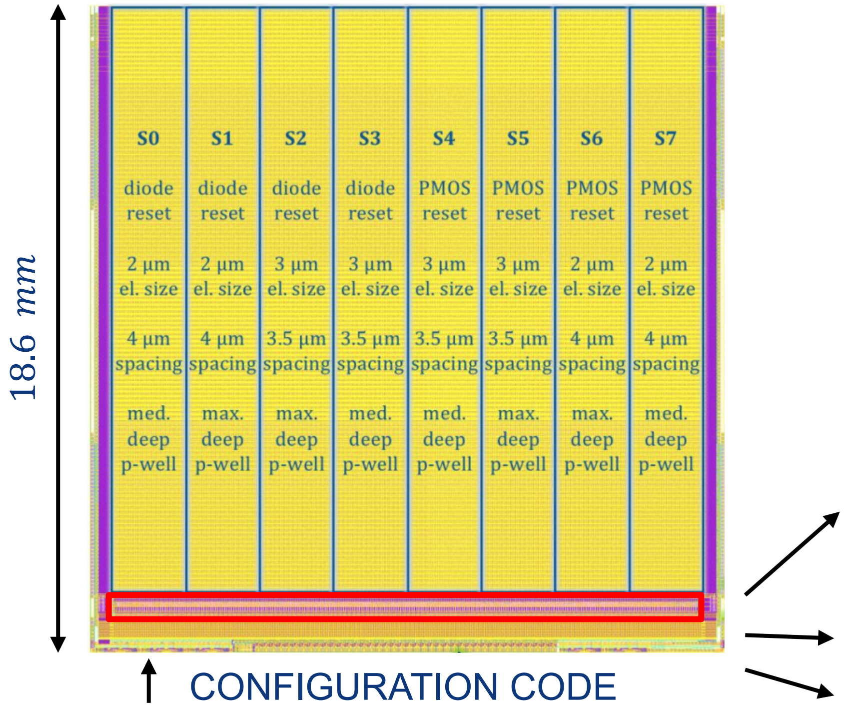
- **Low power Front-End design**
  - Front-End circuit design
  - Simulation results
  - In-pixel tuning DAC

- **Timing characterization of MALTA**
  - MALTA asynchronous output
  - PicoTDC specifications
  - Lab measurements
  - Testbeam

- **Conclusions**



DACs and biasing circuits



DACs FOR ANALOGUE BIASES

DIGITAL PERIPHERY

LVDS DRIVER

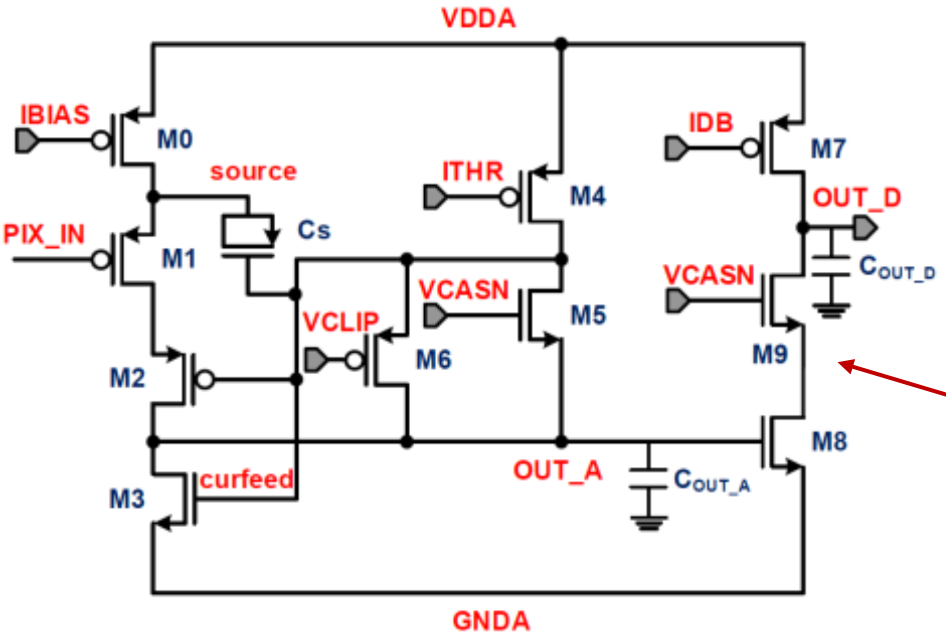
CONFIGURATION CODE

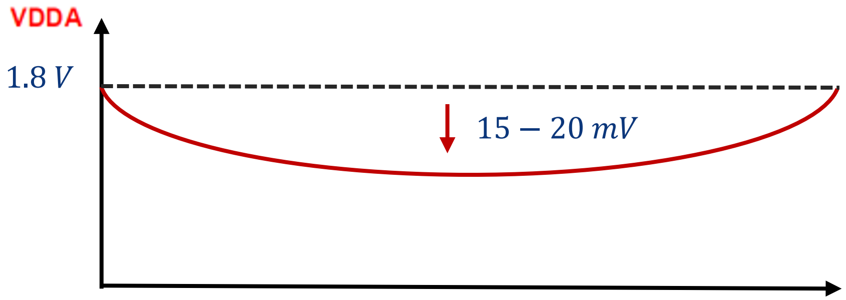
In a pixel sensor, part of the chip is dedicated to the DACs: blocks to bias the analogue circuits providing a current or a voltage, configurable through a digital code.

Challenges:

Independent from process, voltage and temperature.
Linear behavior as a function of code.
Small area.

MALTA Powering scheme





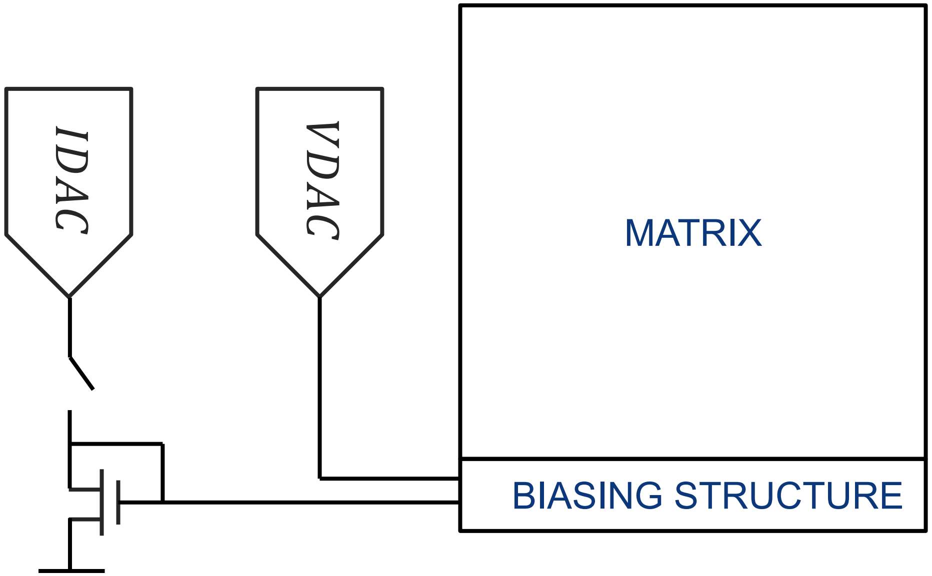
Supply voltage provided from the side

Front-End current ~ $0.5\ \mu A$

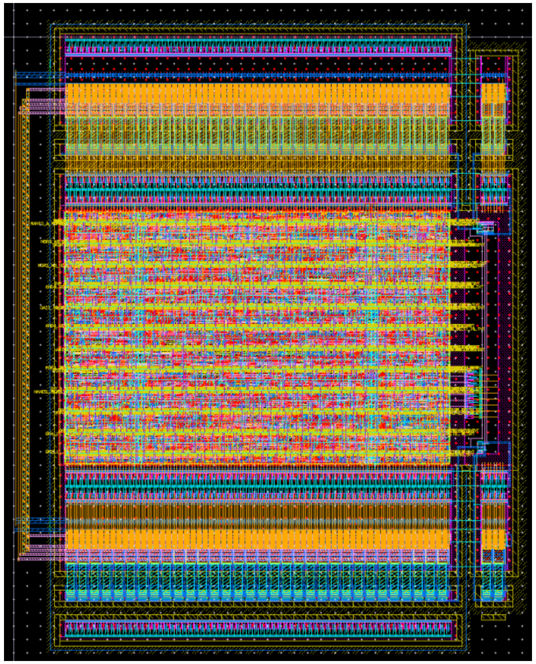
$512x512$ pixels $\sim 262\ k$ pixels → $\sim 132\ mA$

$15-20\ mV$ voltage drop on the supply in the middle of the matrix

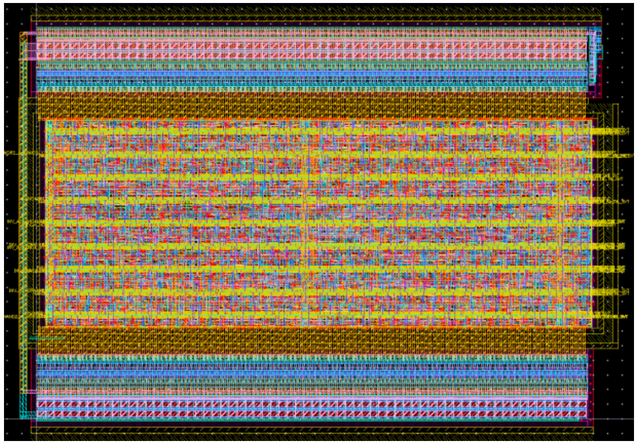
MiniMALTA DACs concept



CURRENT DAC



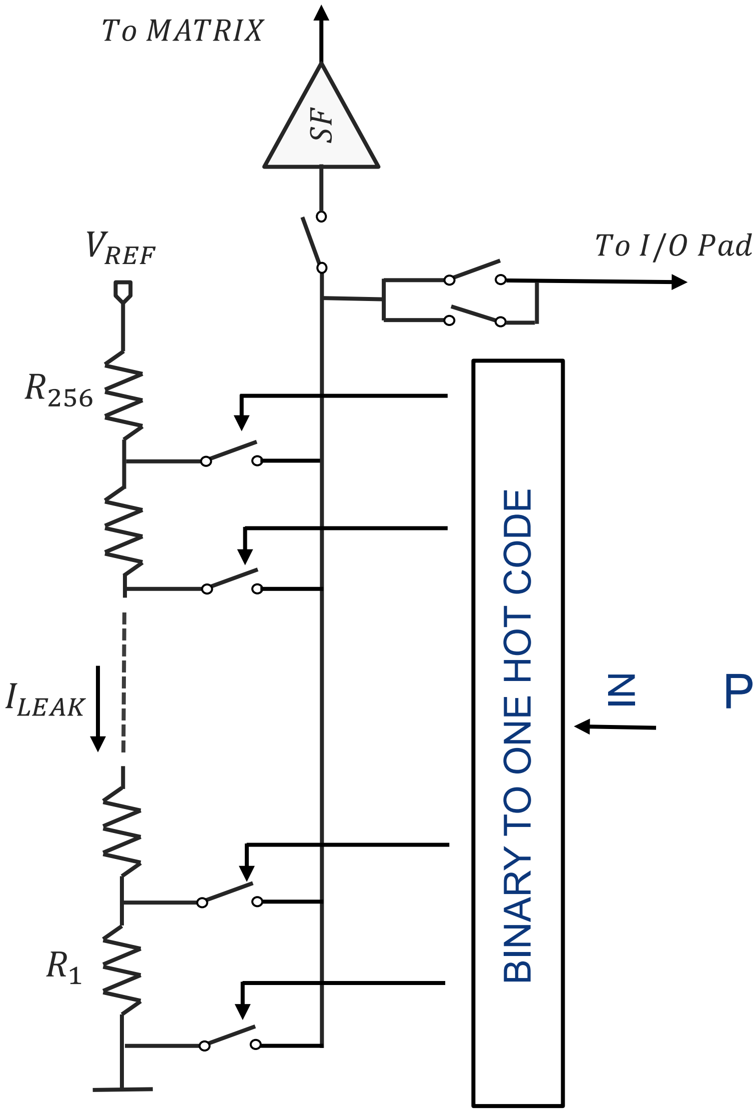
VOLTAGE DAC

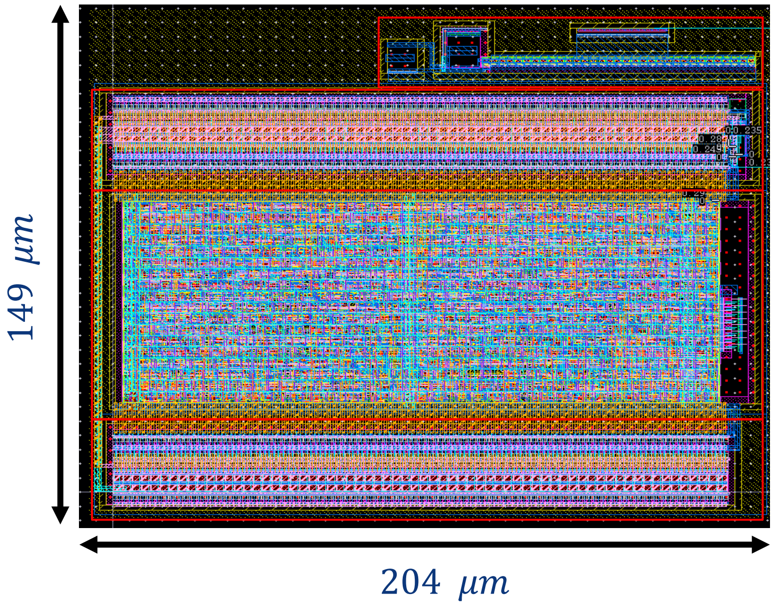


Non Modular design:

- Local DACs implemented to save space ($\sim 5\ x$ with respect to a modular approach)
- Number of bits independent from the Matrix width (8 bits DACs implemented)
- Easy to increase the number of DACs and biasing lines towards the FE
- Flexible layout

Voltage DAC

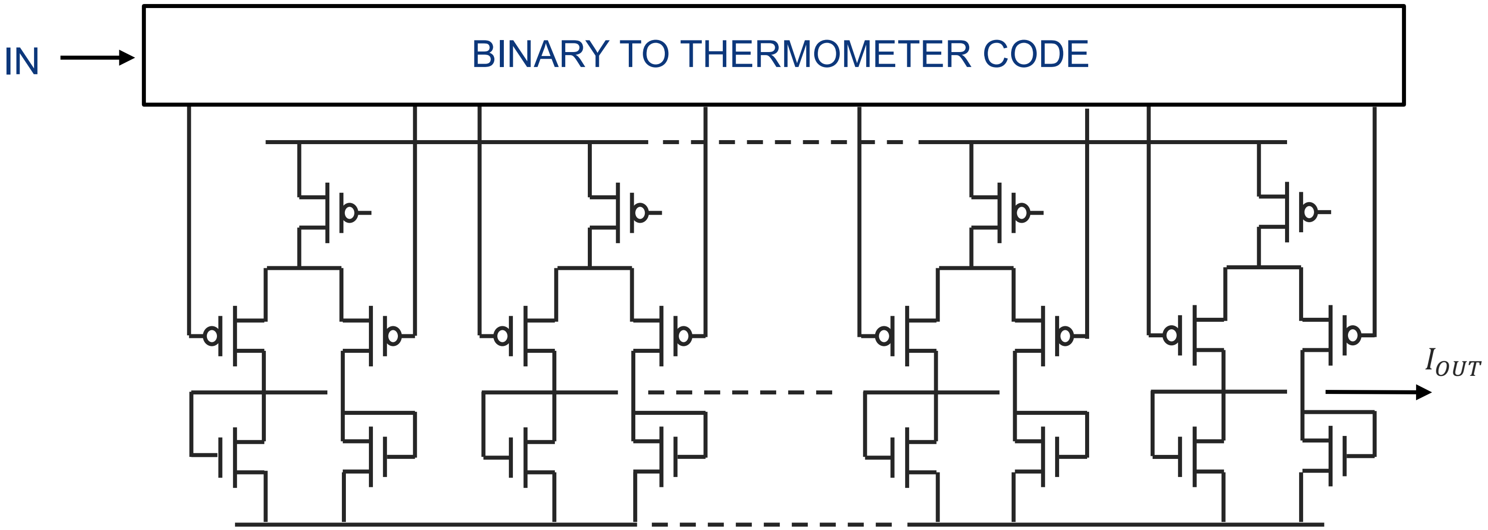


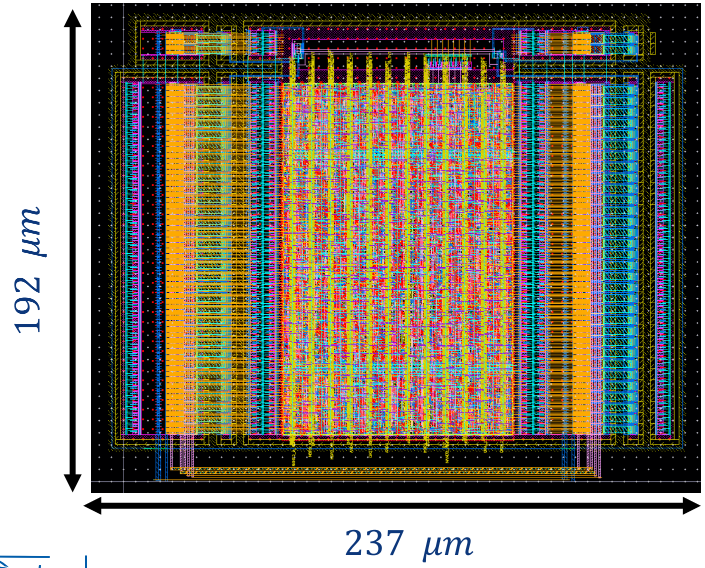


Possibility to override and monitor the voltage.

TYPE	RESISTOR STRING
RESOLUTION	8 BITS (LSB=7.03mV)
POWER	$32\ \mu W$
AREA	$204\ x\ 149\ \mu m^2$

Current DAC



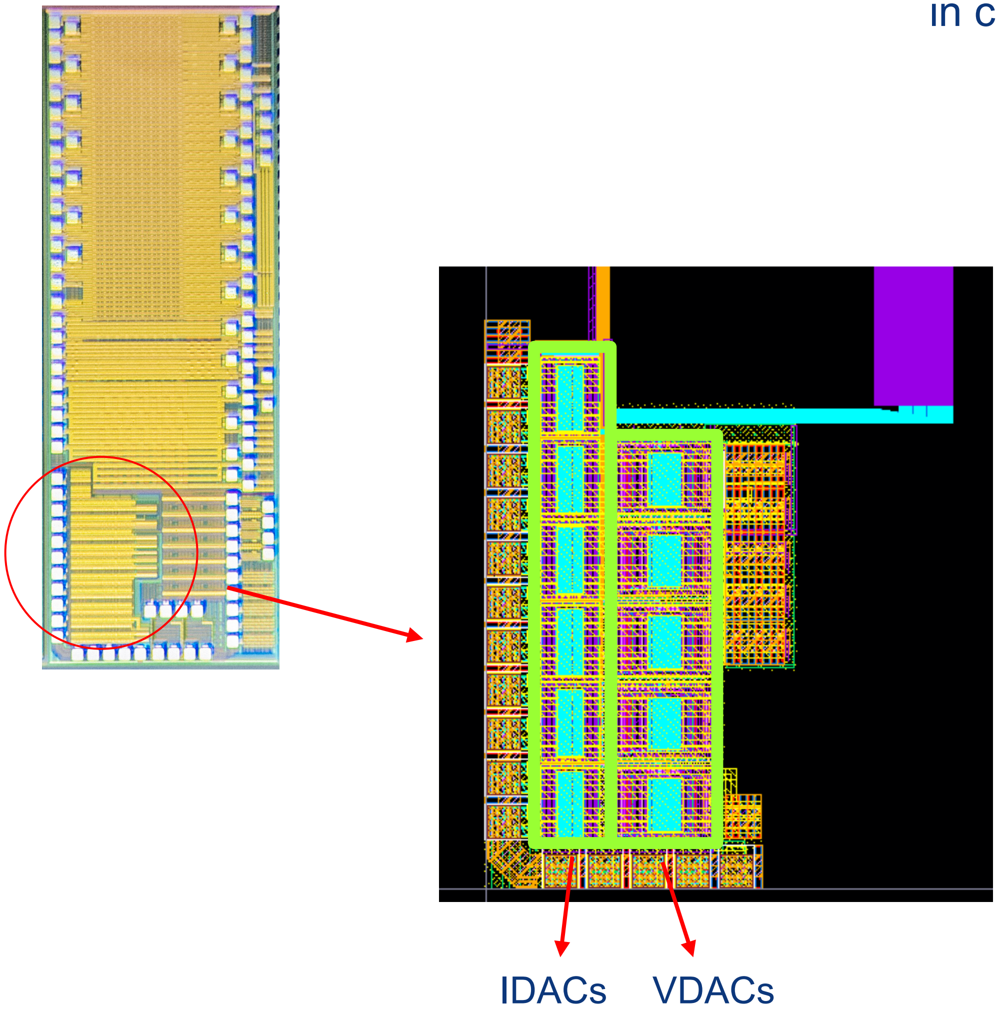


Possibility to override and monitor the current.

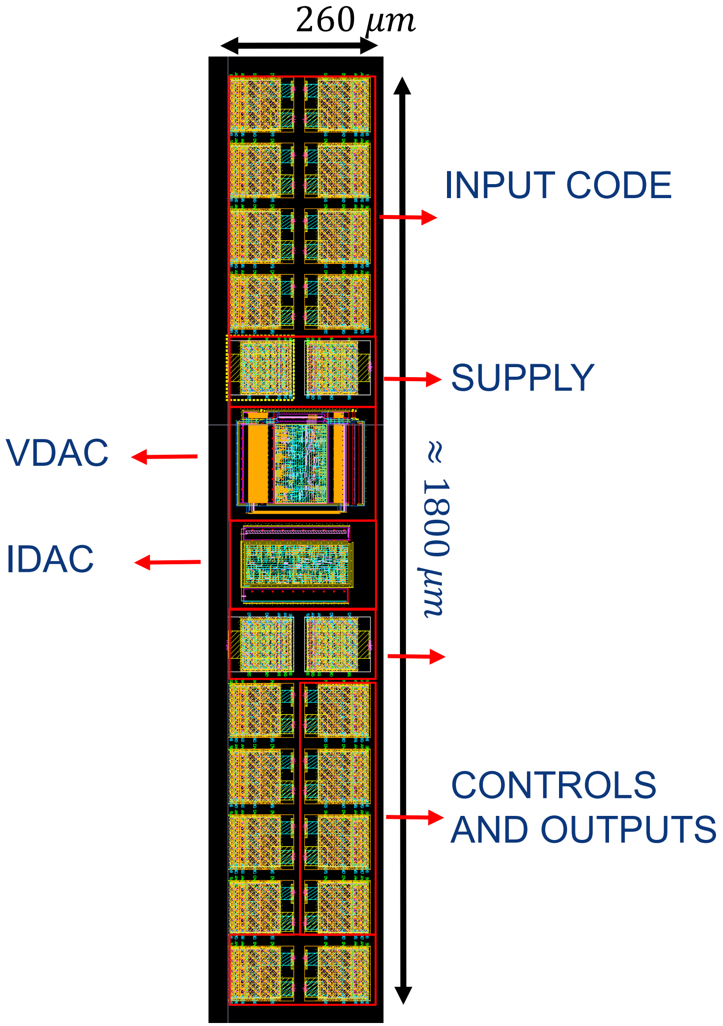
TYPE	PMOS CURRENT SOURCE
RESOLUTION	8 BITS ($LSB \approx 20nA$)
POWER	$14\ \mu W$
AREA	$192\ x\ 237\ \mu m^2$

Integration in MiniMALTA and testchip

MiniMalta



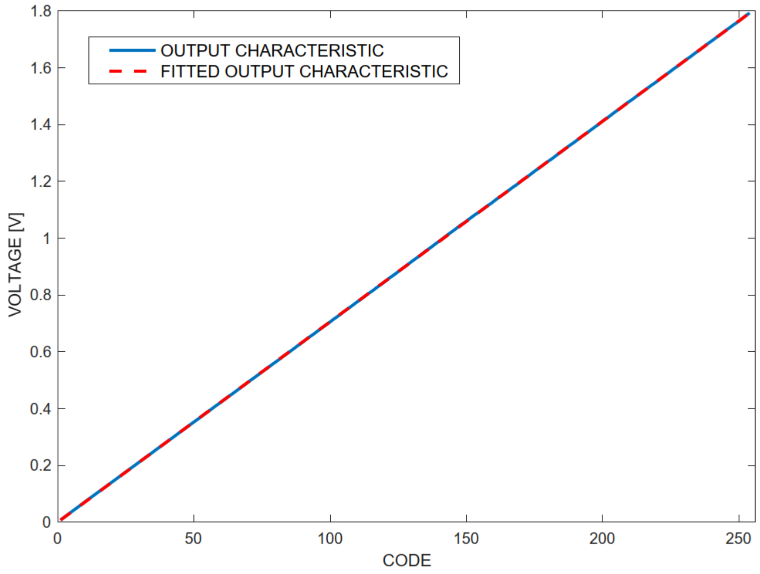
Test-chip implemented as a backup solution in case of malfunctioning on MiniMALTA



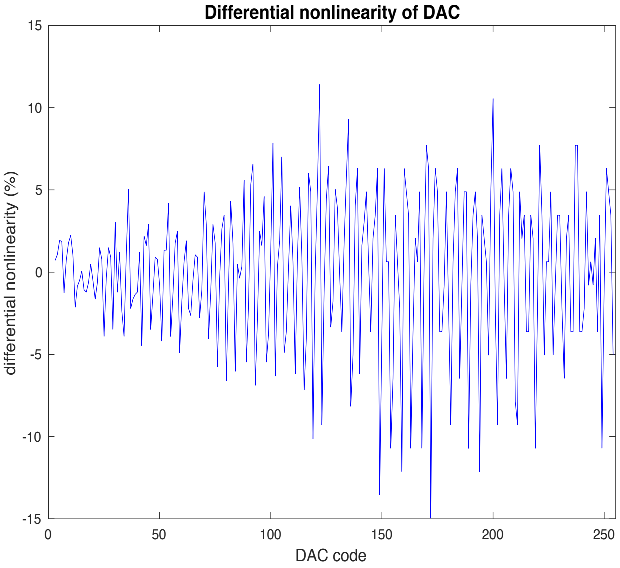
Linearity of the VDACs vs TID

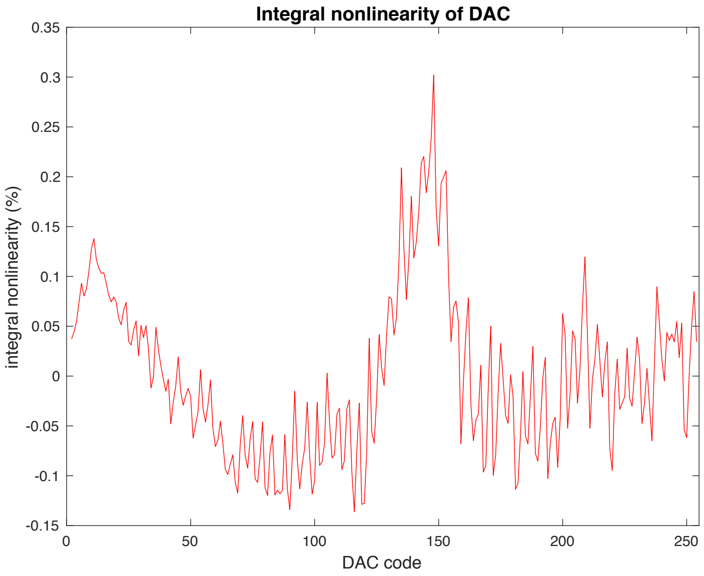
Measurement on 15 chips before and after ionizing radiation (TID).

	DNL	INL
NO_IRR	12%	40%
1 MRad	18%	42%
66 MRad	16%	35%
91 MRad	15%	30%



$91\ MRad$:

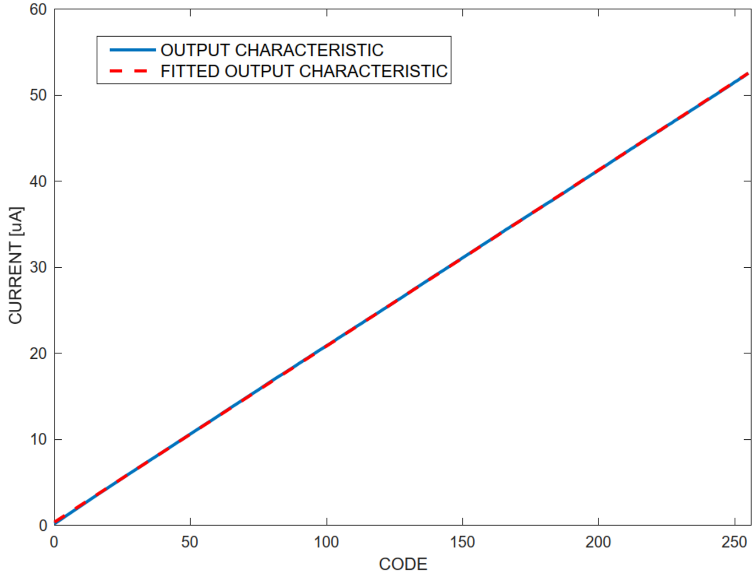




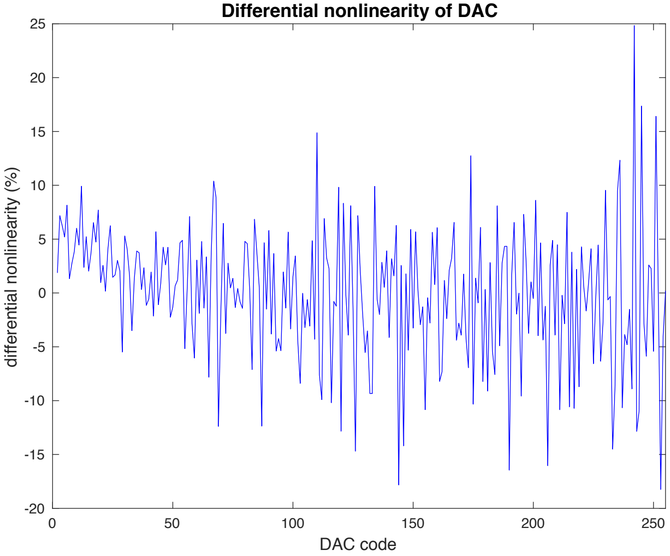
Linearity of the IDACs vs TID

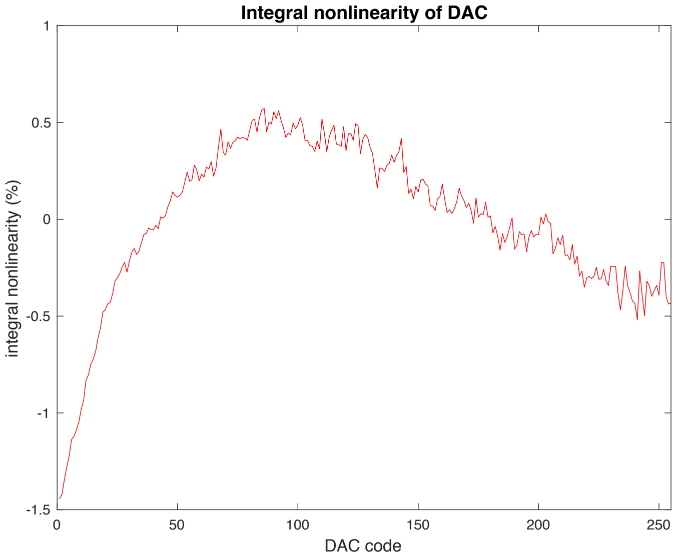
Measurement on 15 chips before and after ionizing radiation (TID).

	DNL	INL
NO_IRR	18%	40%
1 MRad	30%	130%
66 MRad	29%	111%
91 MRad	25%	140%



$91\ MRad$:





IDACs testing - mismatch

Measurement on 15 chips before and after ionizing radiation (TID).

SAMPLE	ITHR [μA]	IRESET [μA]	IDB [μA]	ICASN [μA]	IBIAS [μA]	AVG per sample
#1	57.6	56.6	57.9	56.4	58.3	57.36
#2	54.2	55.2	54.2	54.9	54.9	54.68
#3	59.9	59.9	59.5	59.6	59.3	59.64
#4	59.4	58.8	59.2	59.1	59.4	59.18
AVG per channel T=27°C	57.775	57.625	57.7	57.5	57.975	57.595
T=-30°C	52.7325	52.365	52.565	52.25	52.85	52.5525
After irradiation	51.092	51.80	51.200	51.3287	51.82	51.448

Current ranges are dependent on process, temperature and also ionizing radiation dose.

Similar values of average currents for the different channels indicate no design issue.

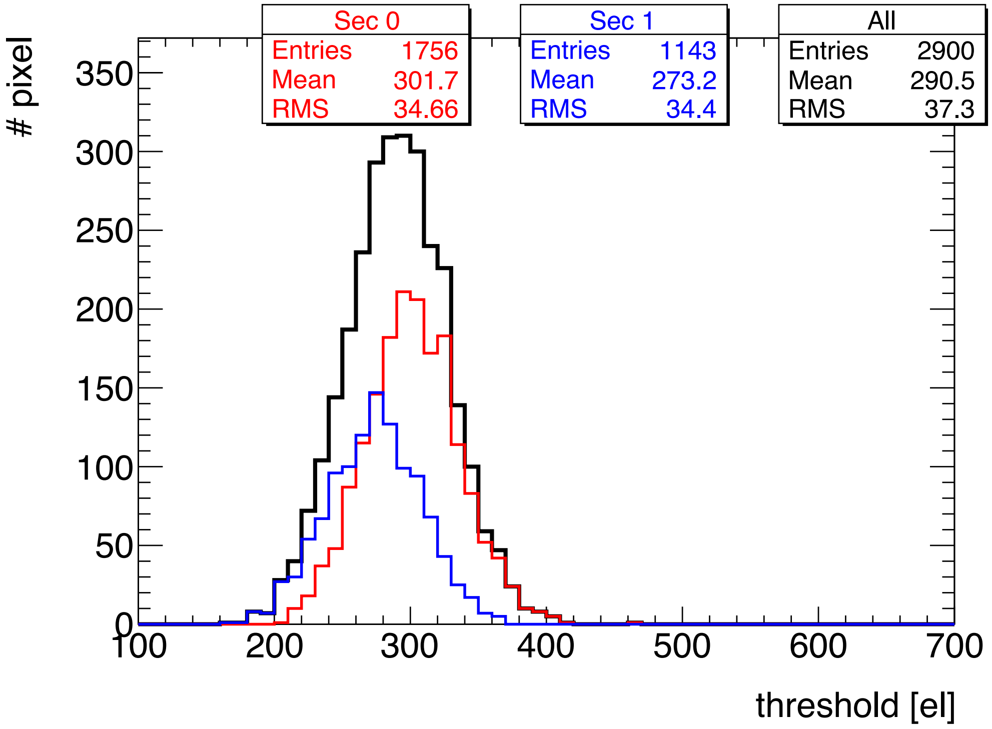
→ Possibility to use it with a Bandgap reference for a better PVT independence.

Threshold dispersion and noise

The DACs are setting global references to the pixel matrix but there is a pixel to pixel variability due to the process variations.

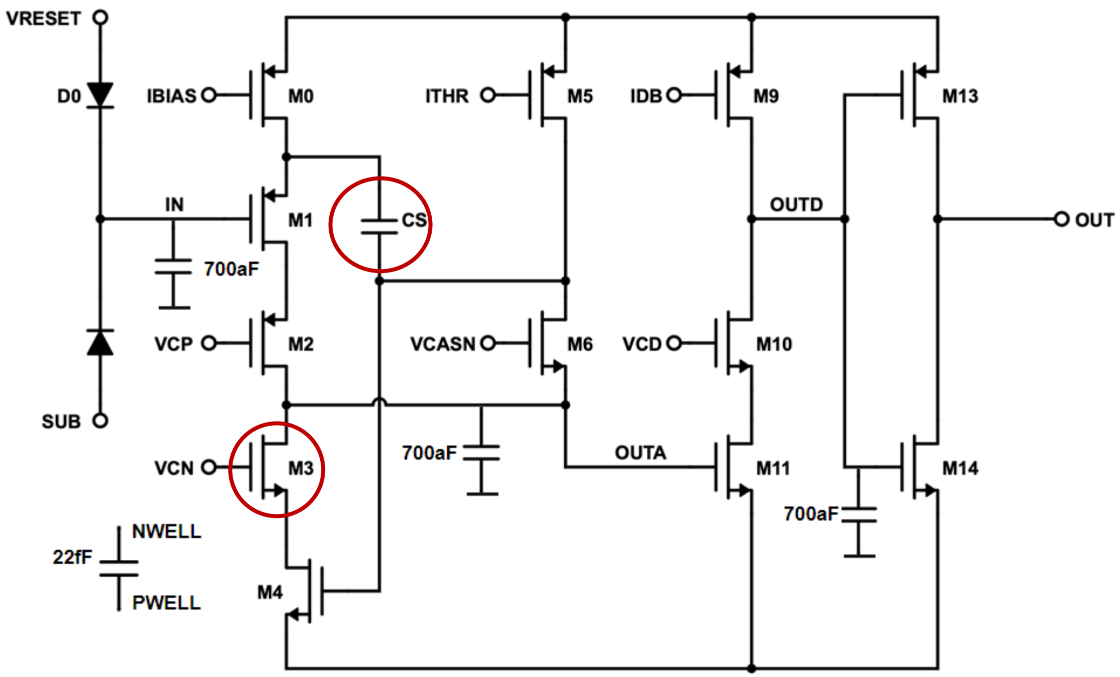
Noise and transistor mismatch cause a variation on important Front-End characteristics as gain, threshold etc.

The behavior over the chip has to be as uniform as possible.



Front-End threshold dispersion

FE study to improve overall performance, focusing on threshold dispersion.



Main sources of Mismatch are:

- the discriminator input transistor M11

$$\sqrt{\left(\sigma_{IN}\cdot\frac{dA_Q}{dQ}\right)^2+\sigma^2_{OUTA}+\sigma^2_{VTH_{M11}}}\cdot g_m=\sigma_I$$

- the output conductance of the sink transistor

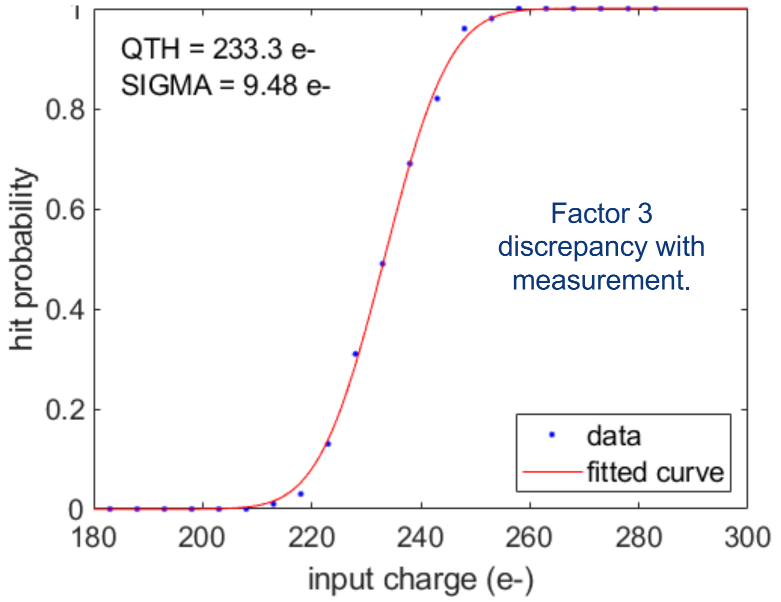
Added M3 to cascode sink transistor M4

Relevant RTS contributor, transistor M4: enlarged for next developments

Larger (4x) filtering capacitance CS from previous version: further improvement on the gain and better stability

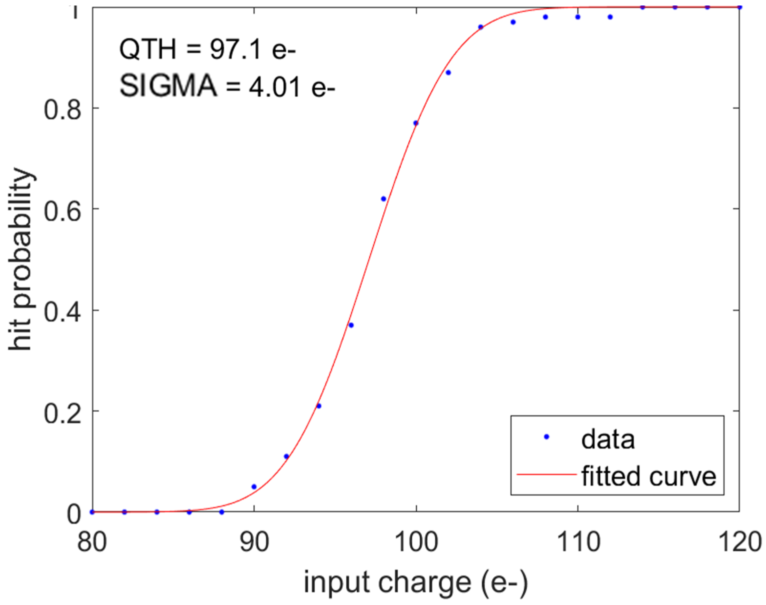
Front-End - simulations

w/o cascode (MALTA/MiniMALTA)



Factor 3 discrepancy with measurement.

w cascade, bigger cap



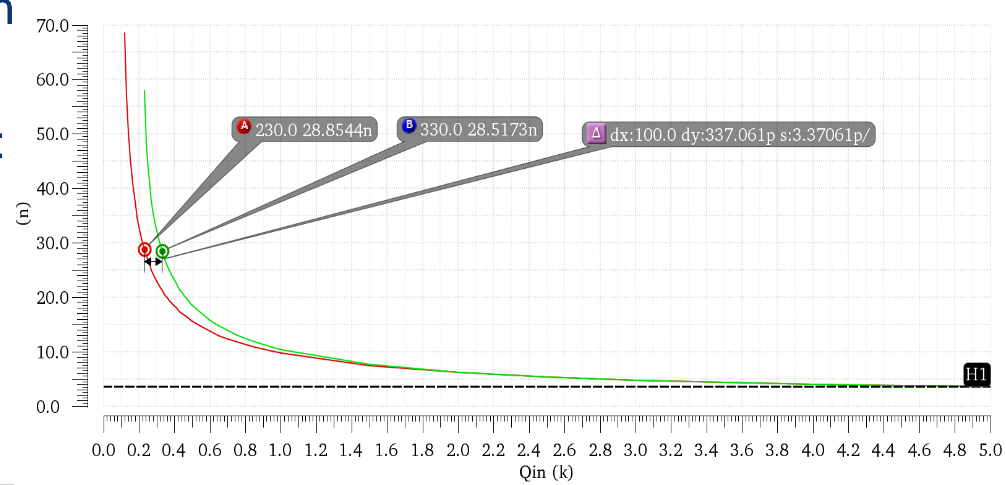
2x more signal for the same charge with cascode.

Faster Front-End with the same charge: lower Time Walk and in time threshold.

Potentially higher efficiency.

Improved time resolution.

TIME WALK curve

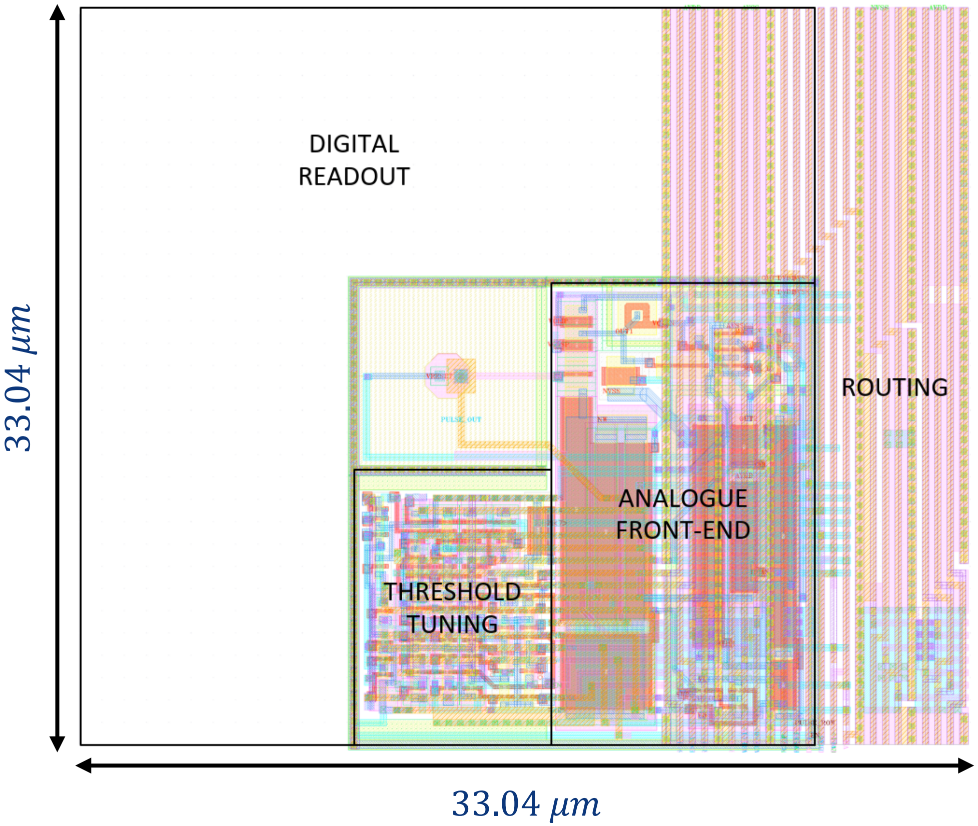


Pixel design

To further reduce the dispersion a local adjustment is implemented.

A three bit DAC has been integrated “in pixel”.

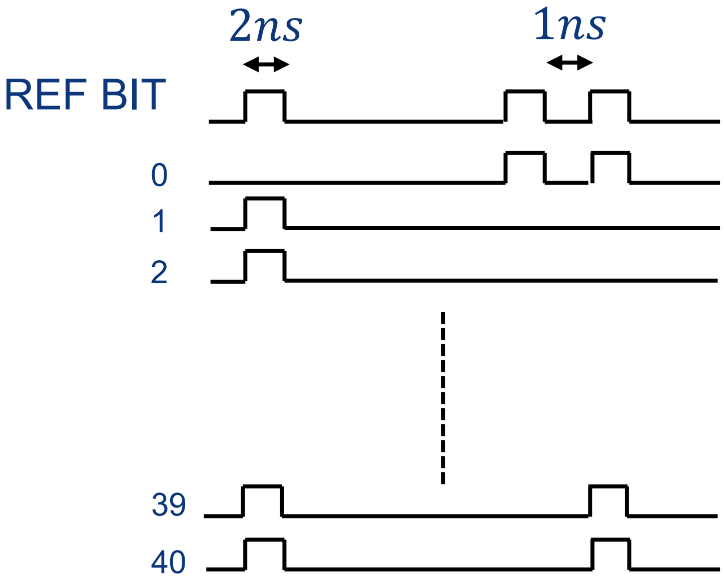
Reduction by a x7 factor of the threshold dispersion.



Timing measurements MALTA+PicoTDC

Malta gives output data asynchronously on a 40 bits bus to provide information on hit position on the matrix.

The outputs are LVDS-compatible (LAPA drivers, see R. Cardella's presentation).



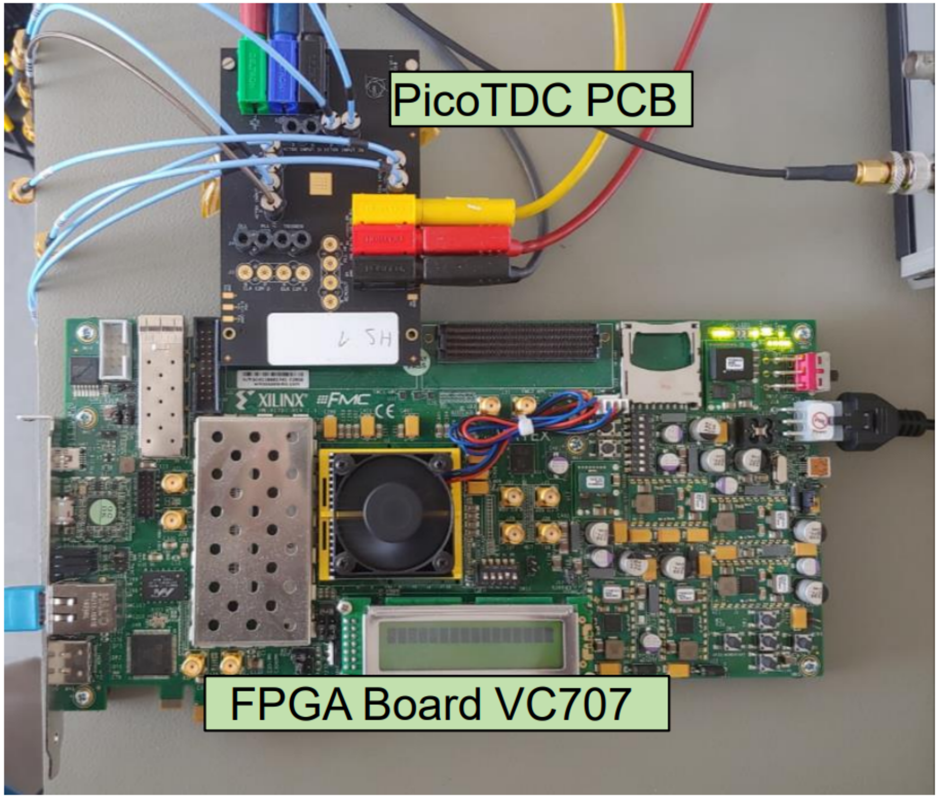
The REF bit is a fast OR signal, high whenever a hit has occurred on the matrix.

PicoTDC features

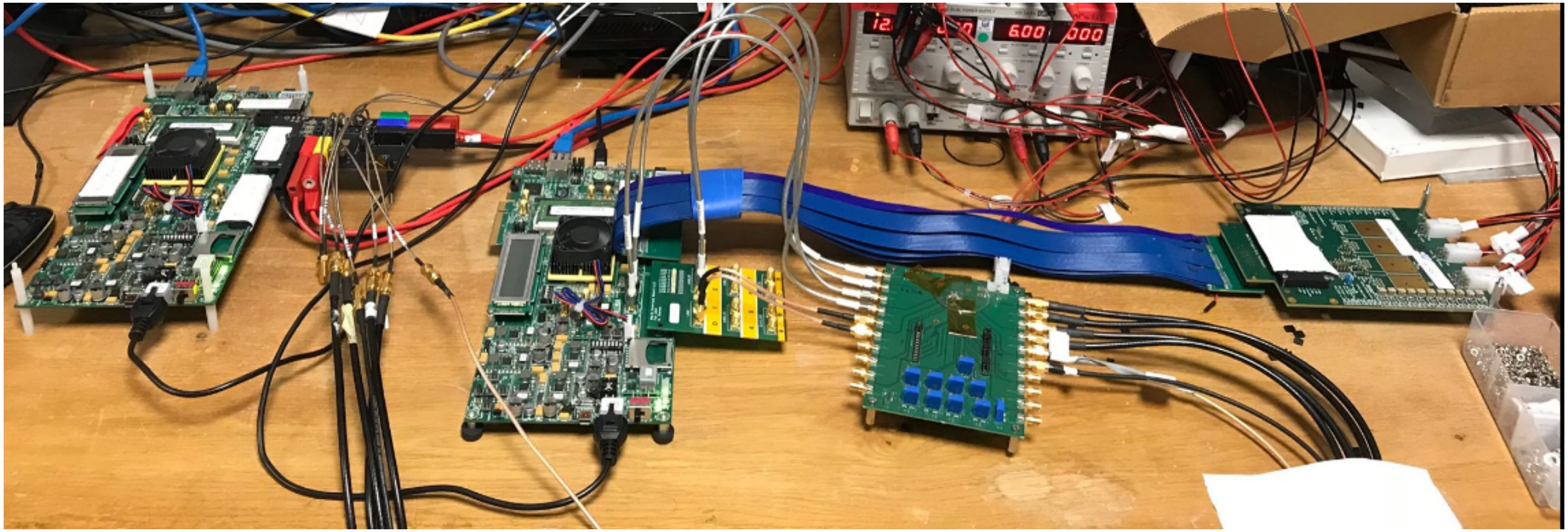
The PicoTDC is a Time to Digital Converter with a 3 ps binning capability.

It has 64 LVDS input channels, compatible with LAPA.

The data are stored in a FIFO and sent out serially through an 8 bit port.



Lab setup



FPGA for PicoTDC

PicoTDC

FPGA for MALTA

LAPA board

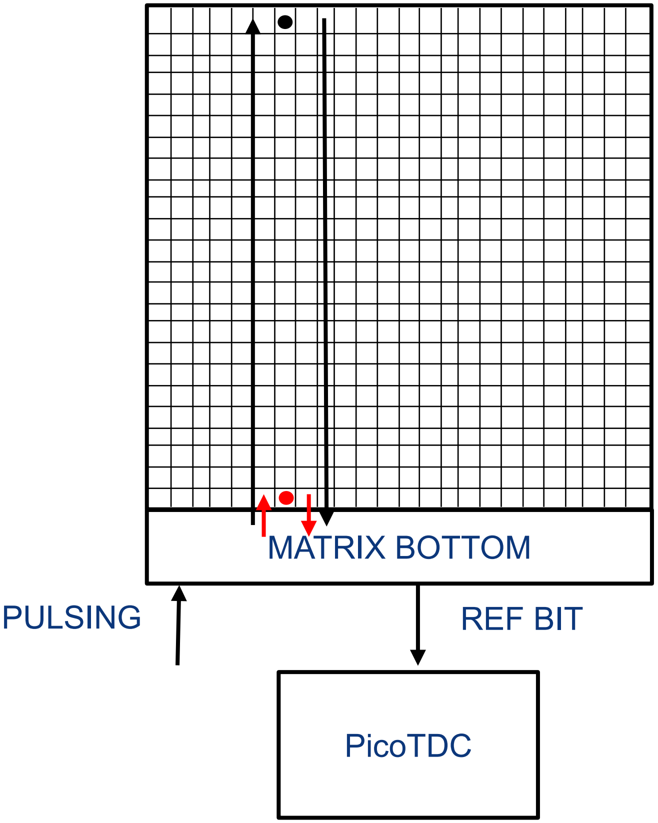
MALTA

LAPA board needed to adapt signals levels to MALTA

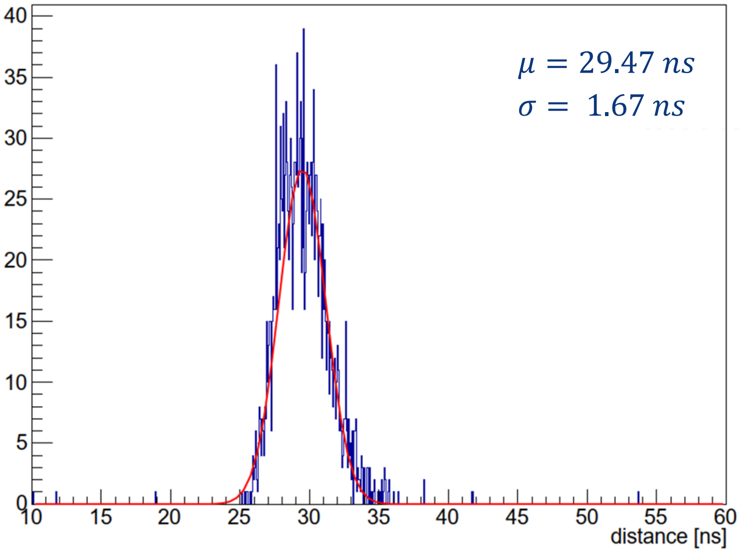
Timing characterization of MALTA

Time of arrival characterization of the REF signal with test pulses.

Pulsed two pixels in the same column.



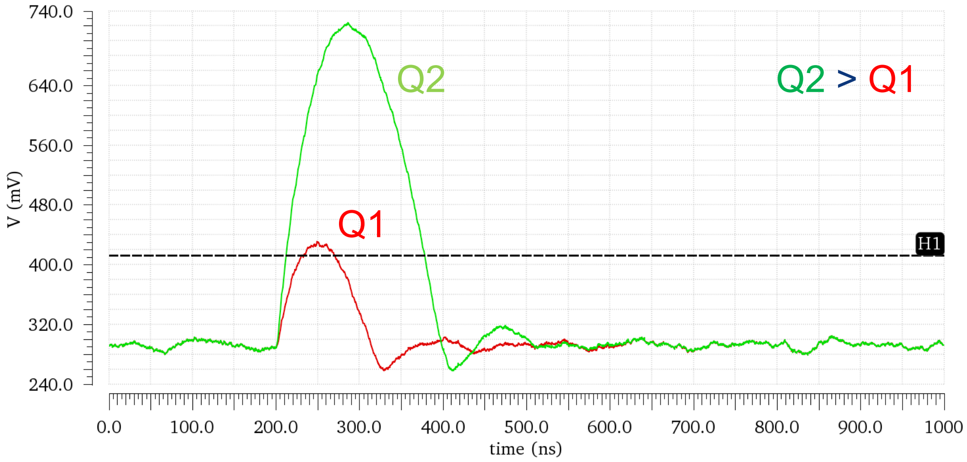
Distribution of REF time of arrival difference



Sigma of the distribution is the Front-End and read out circuitry jitter

Front-End time resolution

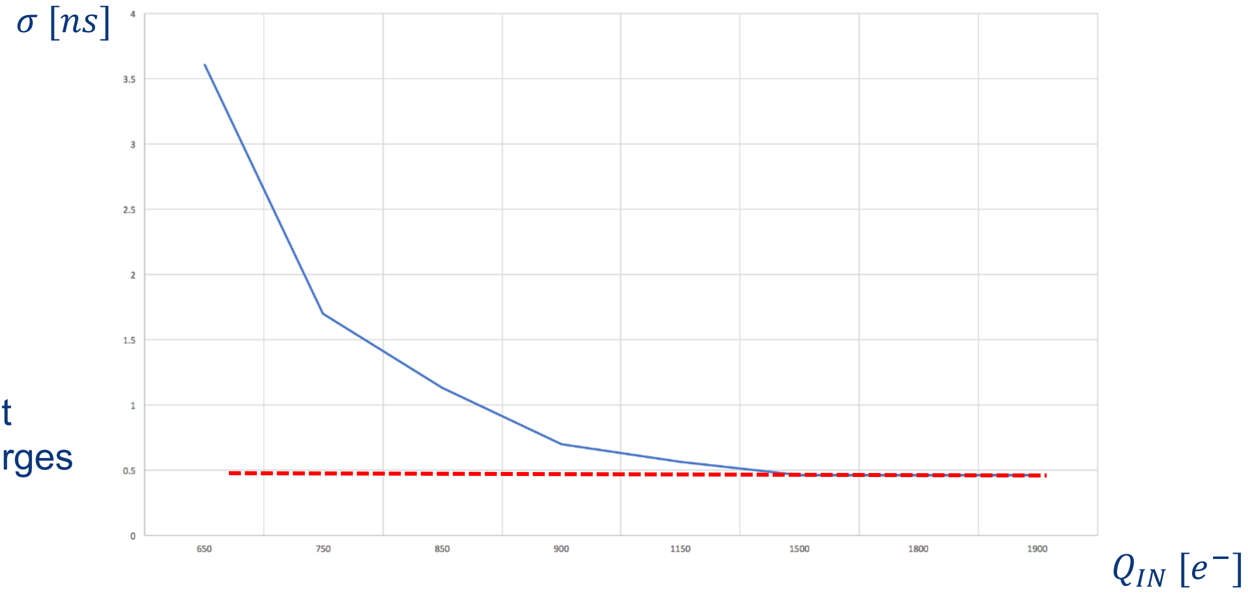
The level of noise and signal speed affect the time resolution



Time jitter

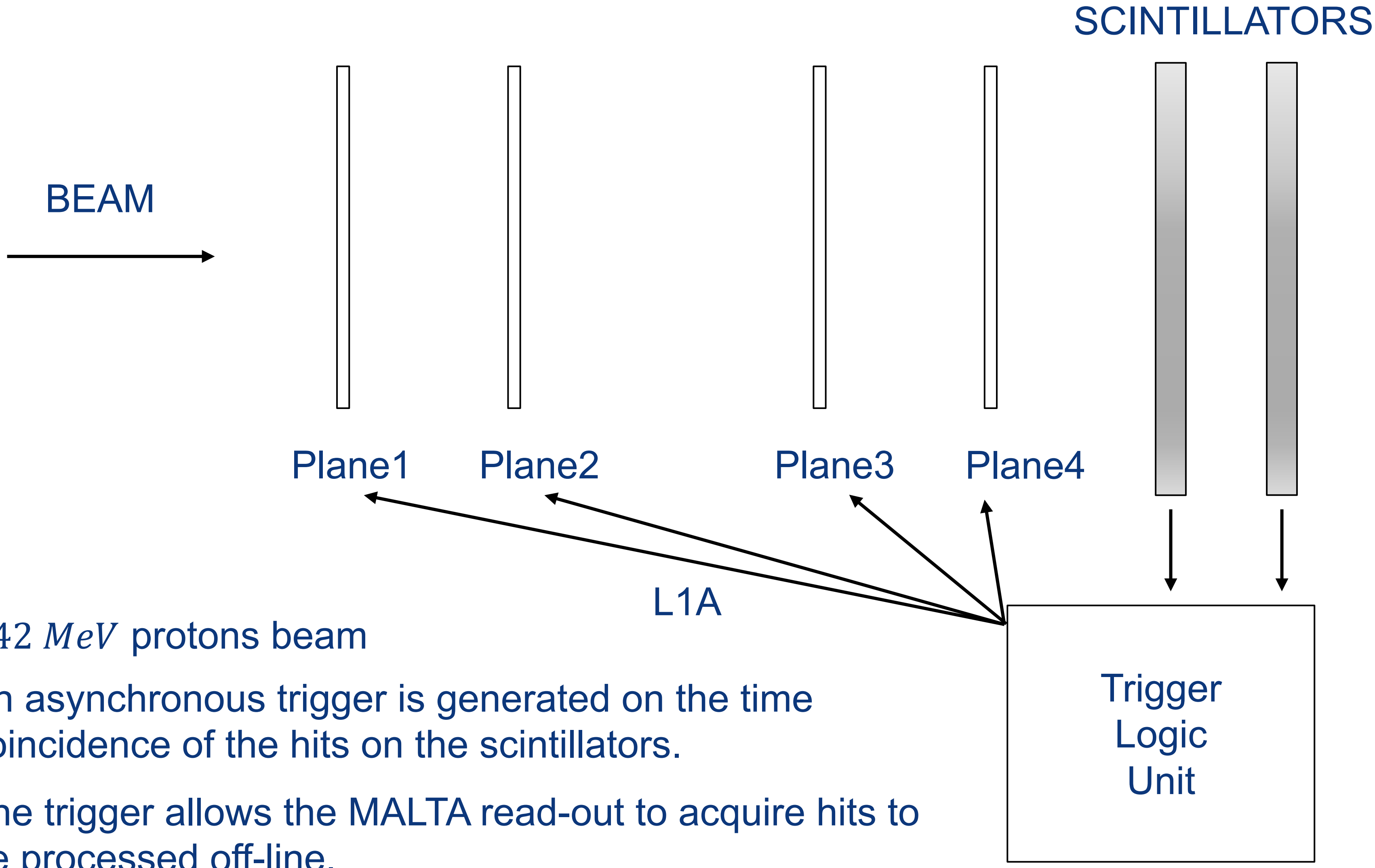
$$\sigma_t = \sigma_{vn} \ / \ \frac{dV}{dT}$$

Jitter vs injected charge



Flattens out at 500ps for charges > 1.5ke

Test beam - setup

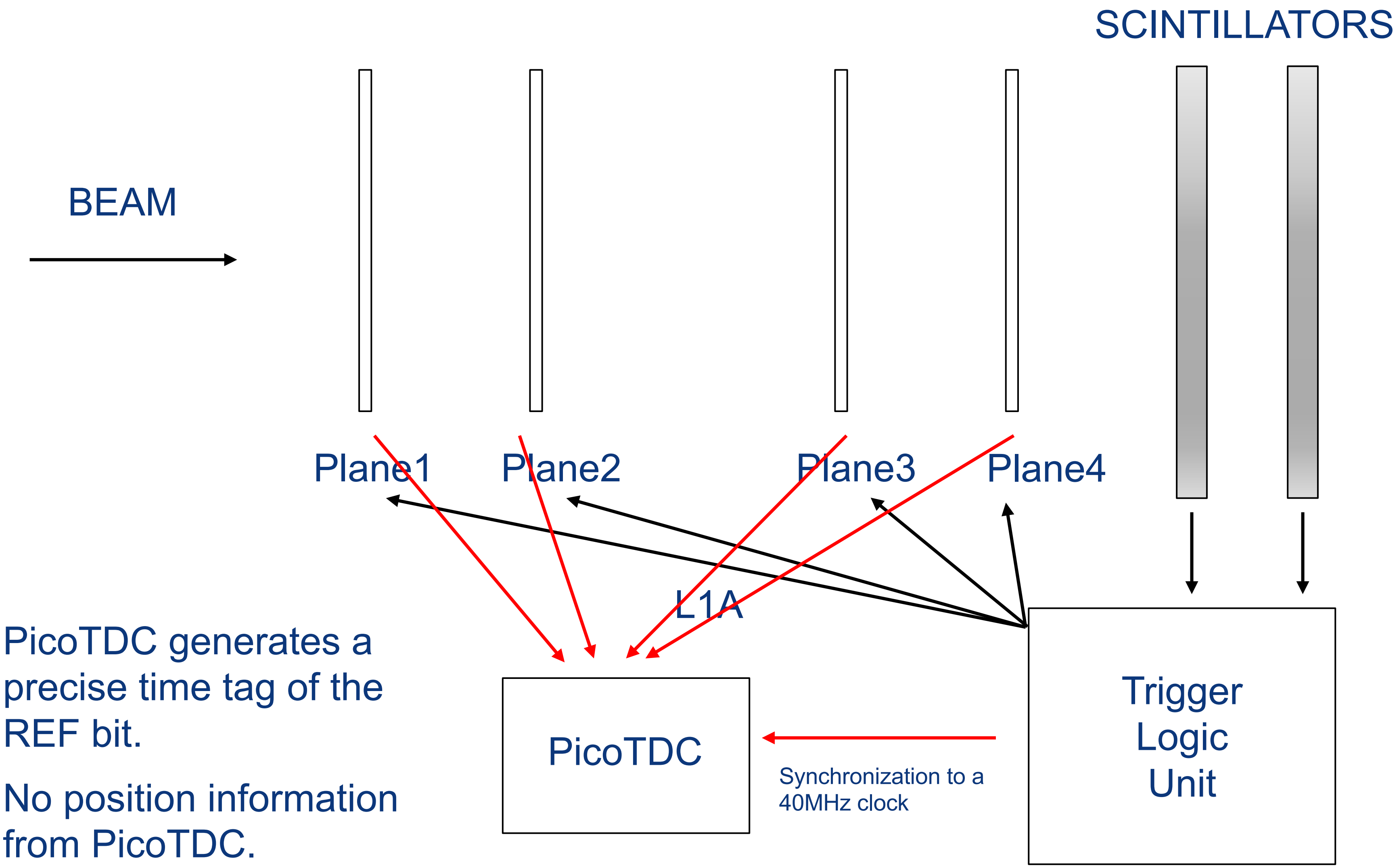


$142\ MeV$ protons beam

An asynchronous trigger is generated on the time coincidence of the hits on the scintillators.

The trigger allows the MALTA read-out to acquire hits to be processed off-line.

PicoTDC – integration in setup



SCINTILLATORS

BEAM

Plane1

Plane2

Plane3

Plane4

L1A

PicoTDC

Synchronization to a 40MHz clock

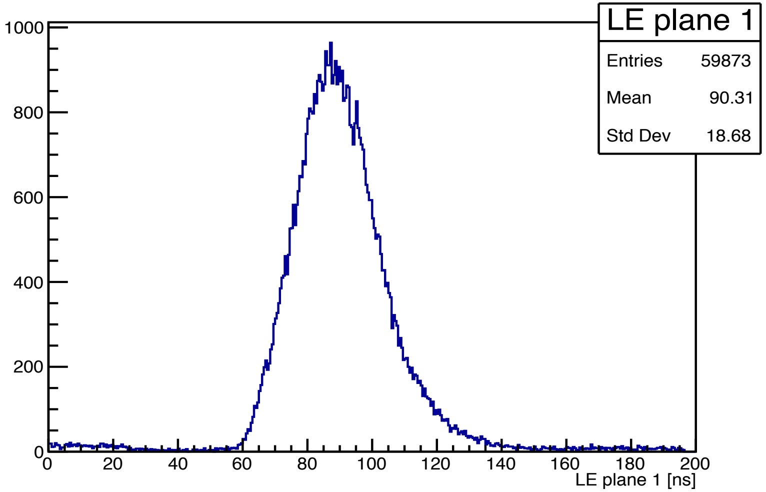
Trigger Logic Unit

PicoTDC generates a precise time tag of the REF bit.

No position information from PicoTDC.

TestBeam - results

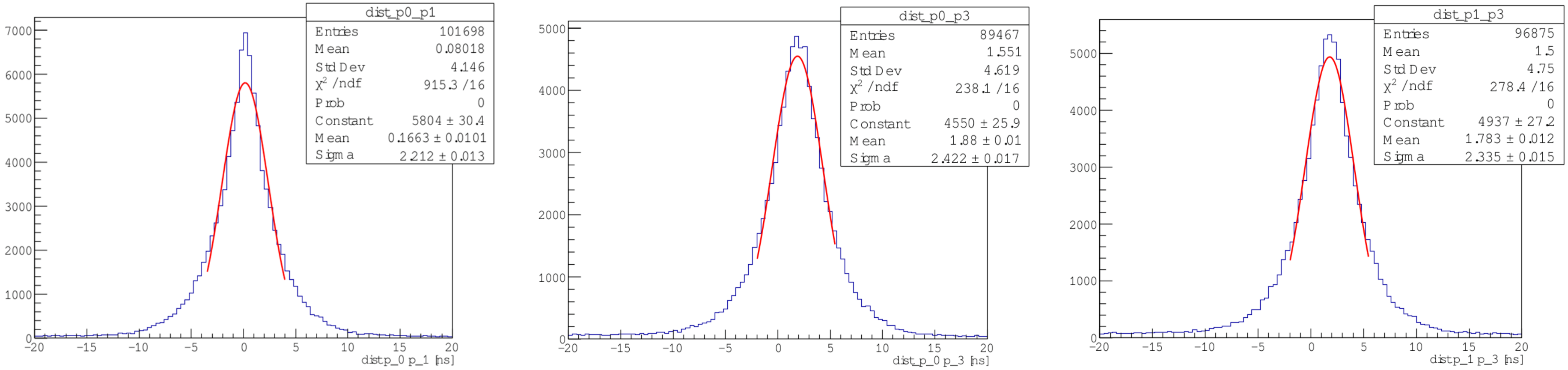
Distribution of the REF bits with respect to the trigger.



Two contributions to the sigma:

- MALTA jitter
- Jitter due to the trigger synchronization with a 40 MHz clock (dominant).

Timing difference between planes (first of the cluster in case of multiple hits).

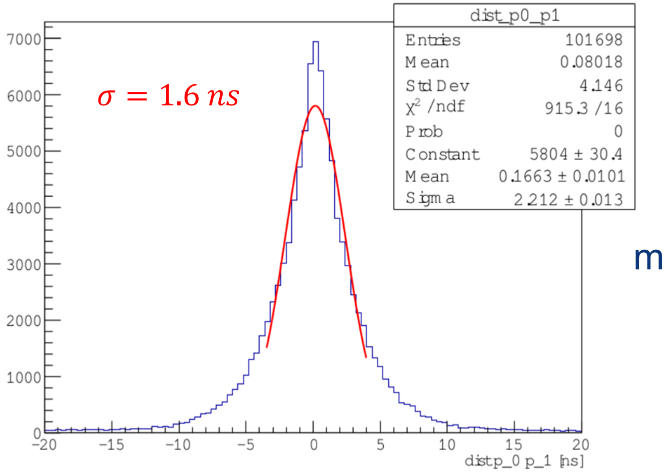


Assuming the different planes uncorrelated: $\sigma_t = 1.6\, ns$

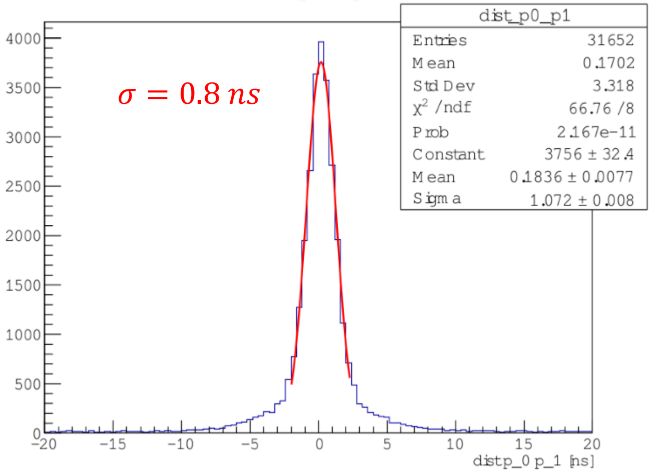
TestBeam - results

Protons beam at 142 MeV -> $\approx x3\ MIP$

The resolution is improved considering only higher charges (single pixel cluster)



After cutting on multiple hits clusters



No information on hit position:

Non gaussian tails due to noisy hits

Shifted average due to column propagation

Future measurements will include correlation between PicoTDC and Malta.

Conclusions

Designed biasing circuits for monolithic pixel sensors (MiniMALTA, MONOPIX2).

extensively characterized with lab measurements and show good results in terms of linearity and radiation hardness.

A thorough study on the Front-End has been carried out, achieving a factor 2 improvement in threshold dispersion in simulations.

The Front-End modification have been implemented in a new layout including a in-pixel tuning DAC and will be used for future TowerJazz developments.

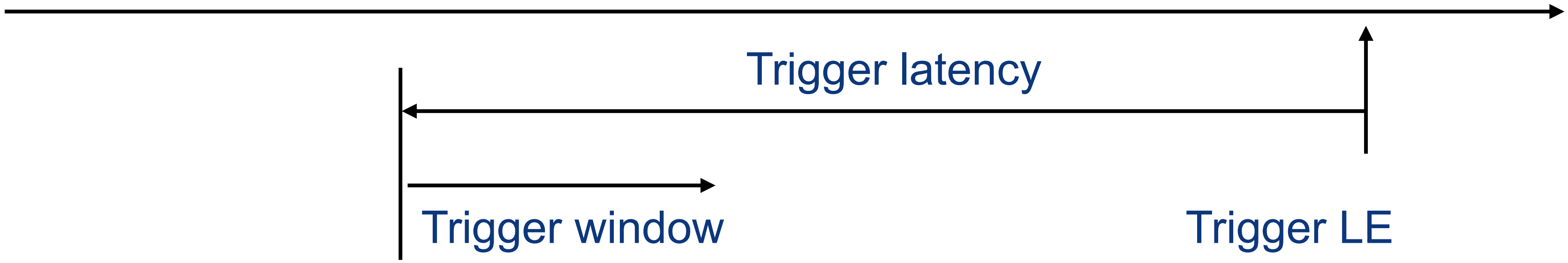
A testing system for MALTA timing characterization which includes a fast timing ASIC (PicoTDC) has been implemented.

A sub ns time resolution has been achieved with lab measurements and a $1.6\ ns$ resolution with testbeams.

BACKUP

PicoTDC settings

Trigger mode enabled:



In the trigger window, picoTDC detects the LE with respect to the trigger LE and its pulse width for each channel.

Trigger window limited to $200\ ns$

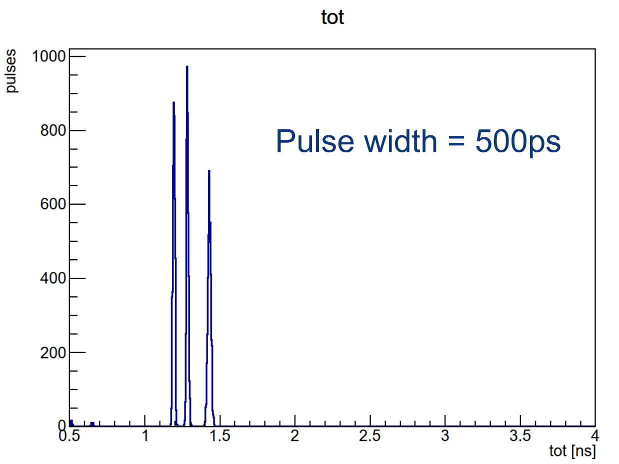
Trigger latency $\approx 600\ ns$ (the trigger signal is delayed because the TLU sends a 16 bit address + processing time)

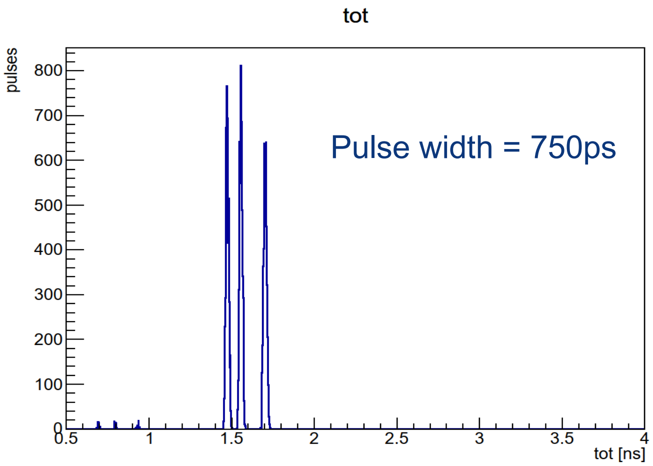
The asynchronous trigger coming from the TLU is synchronized to a 40 MHz clock by one of the four FPGA of the telescope -> huge jitter introduced by the synchronization and by using different clocks for picoTDC and the trigger.

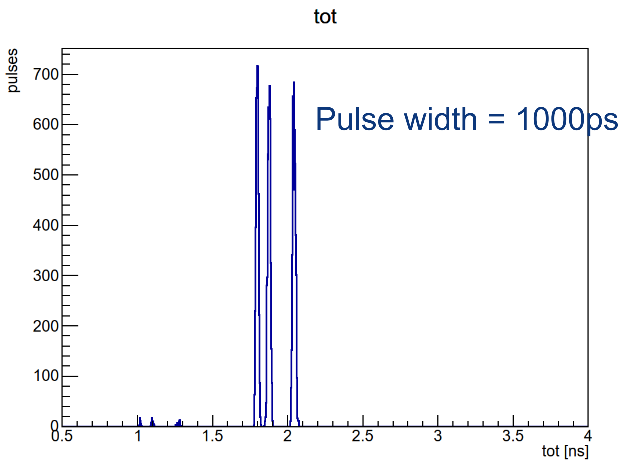
First results

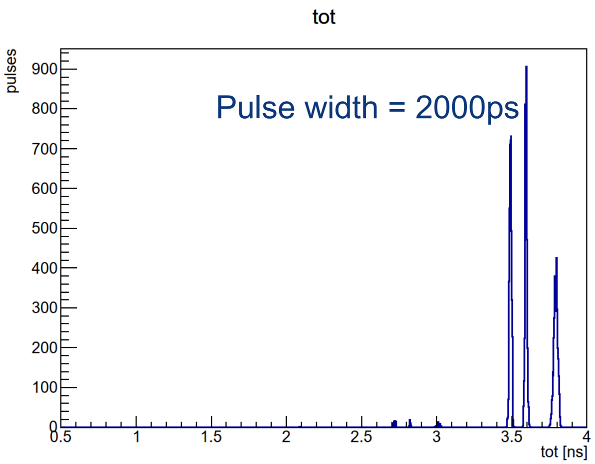
Pulsed three pixels at the top, middle and bottom of the matrix

Pulse width distributions:



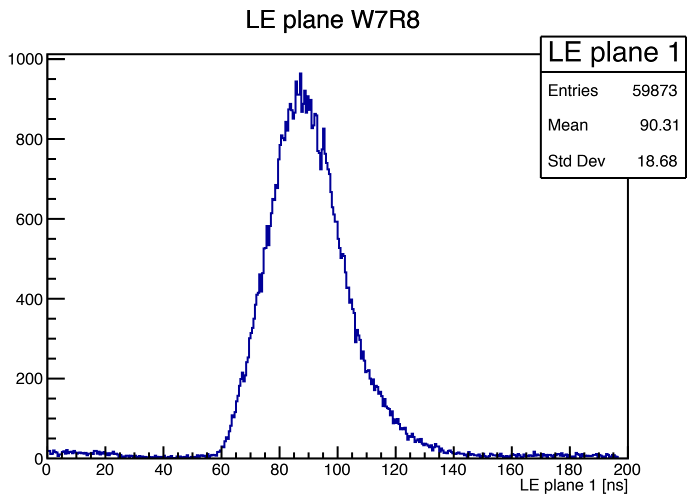


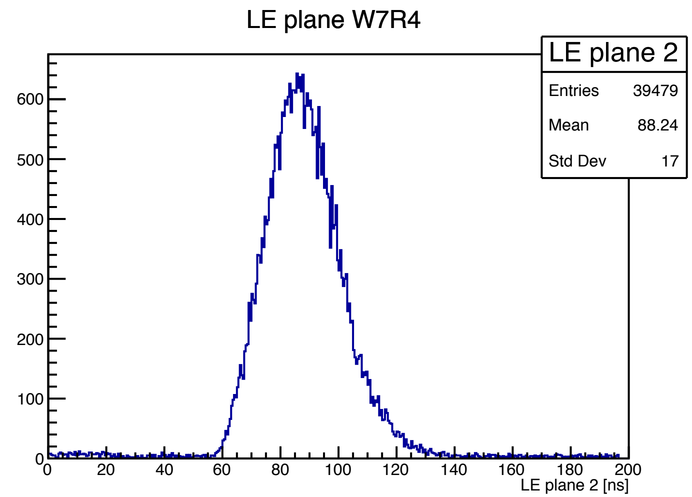


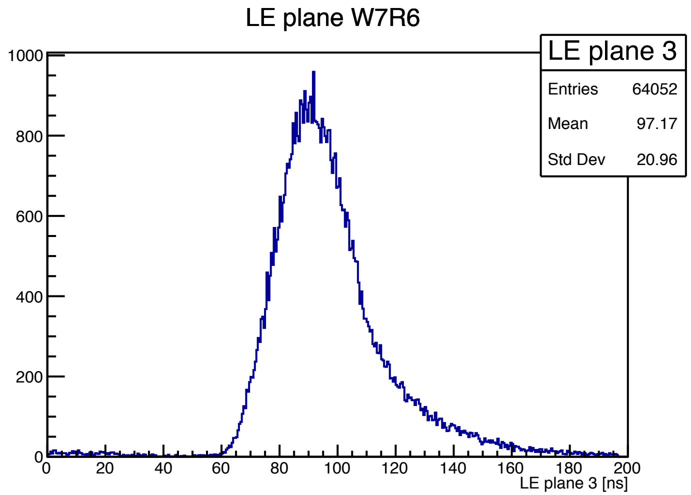


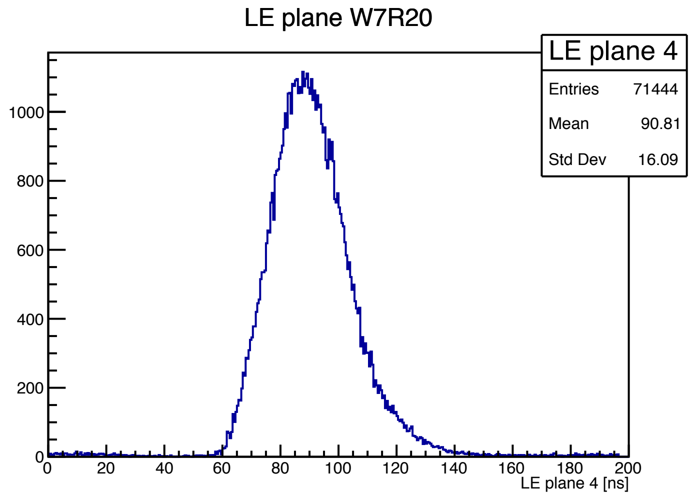
Tested with different LAPA configurations, no change in the jitter

Le distributions after cleaning


LE plane W7R8


LE plane W7R4


LE plane W7R6

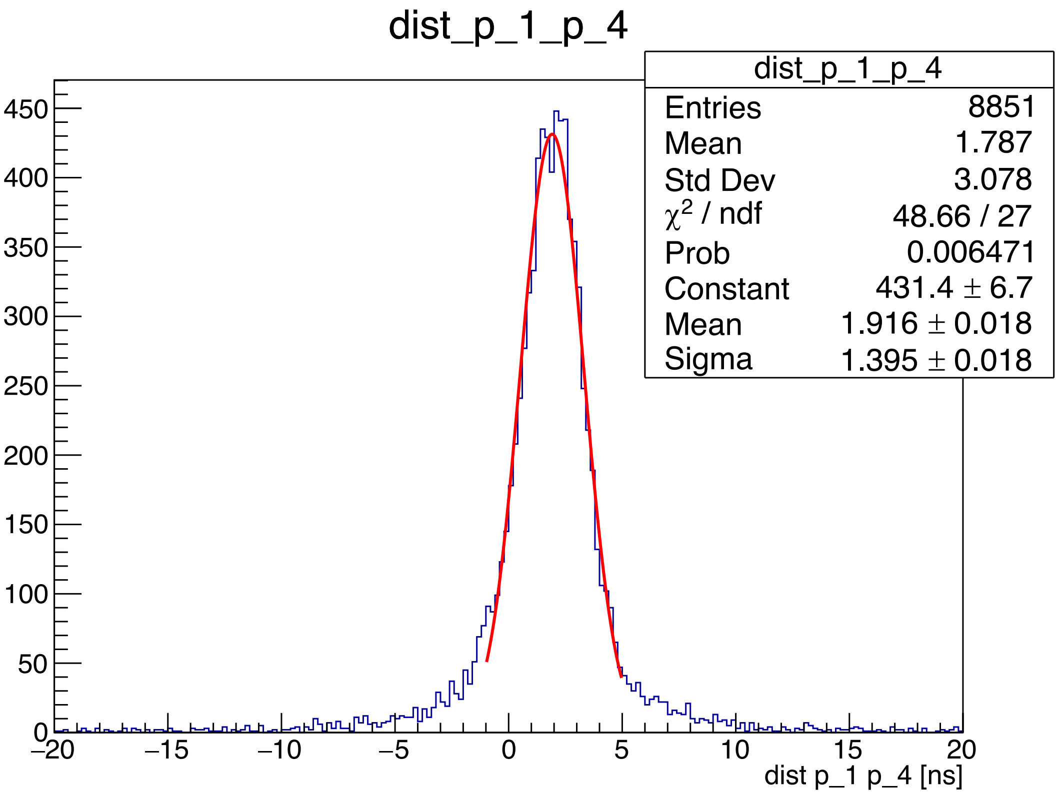

LE plane W7R20

Relative timing difference

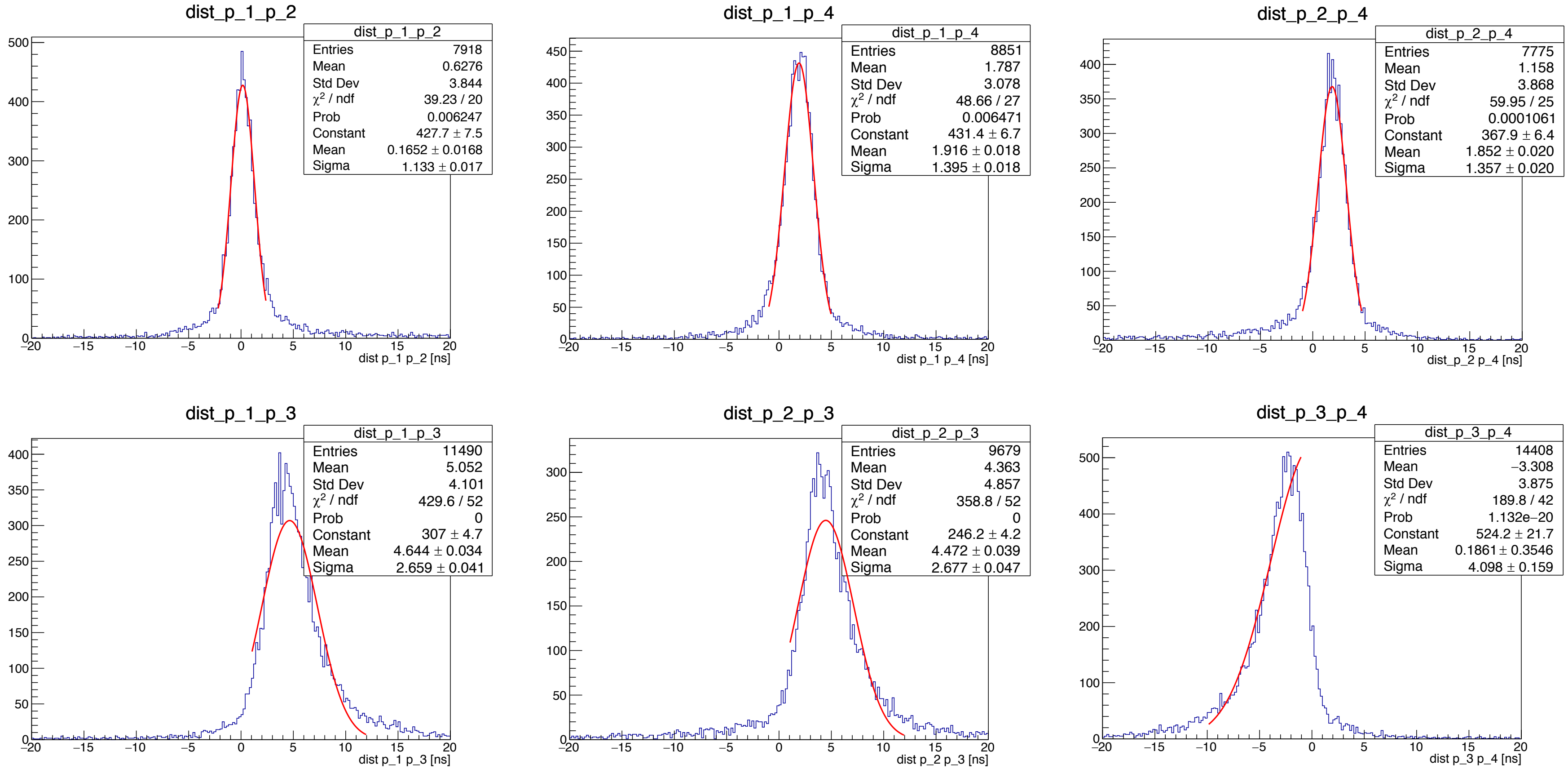
Hit by hit difference for the different planes.

Fitting only the core of the distribution to keep the Gaussian component, clear tails are visible due to different TWs (thresholds) of the planes.

Keeping only the trigger events with 1 hit in both planes to filter the noise



Relative timing difference for all the planes

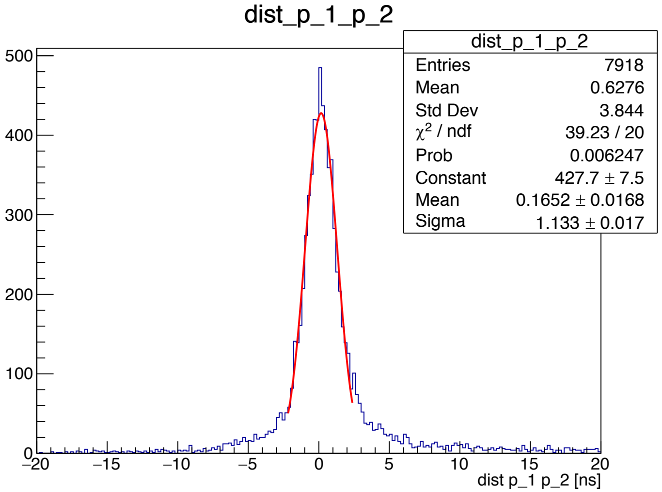


Plane 3 has a worse resolution due to a much higher threshold

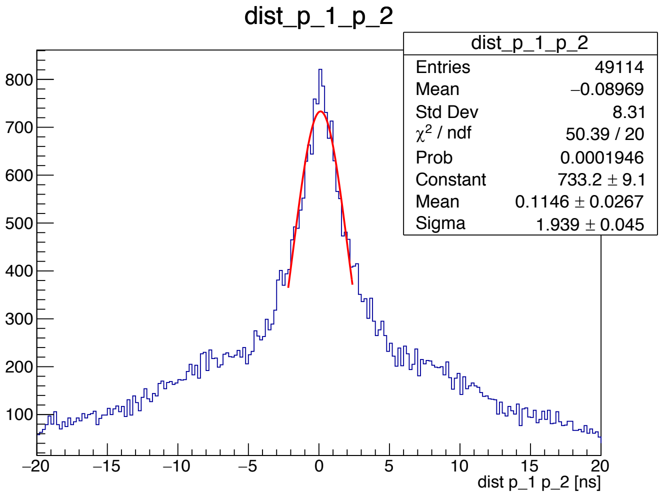
Plane 4 has a higher RMS possibly due to either different threshold or beam defocusing effect and column propagation

Smallest RMS between the first two planes possibly due to their proximity

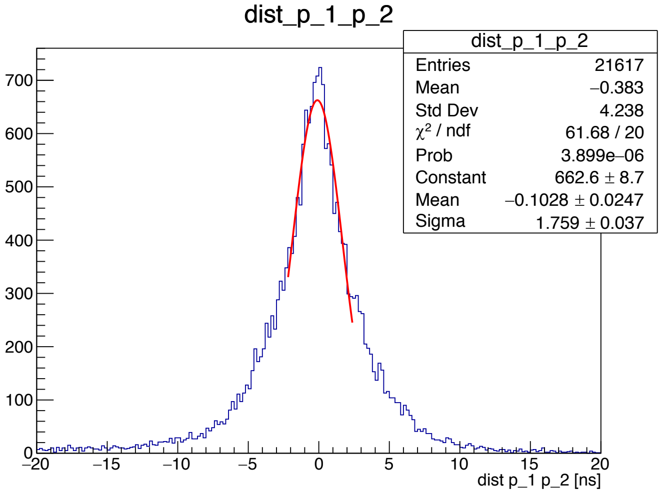
Possible ways to plot



considering events with only one hit per plane (largest possible signal = smallest possible TW)



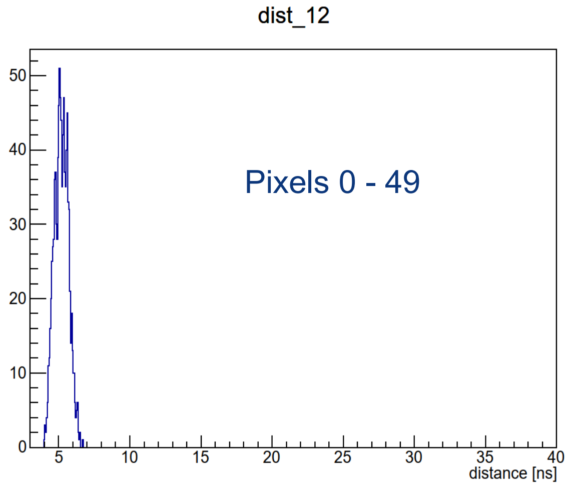
All combinations (including very low energy signals)

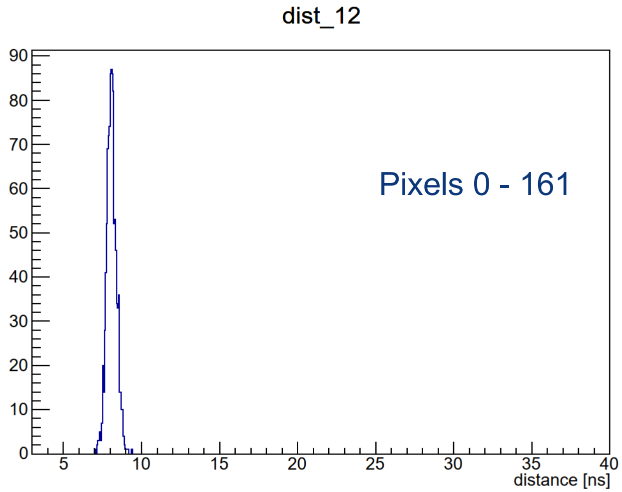


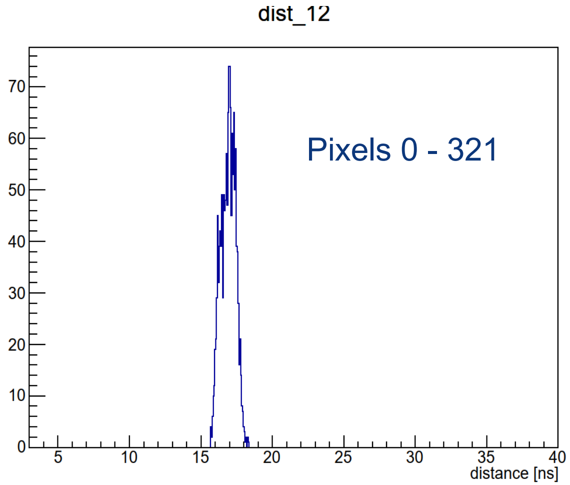
Considering all events but comparing only the leading signals of fastest

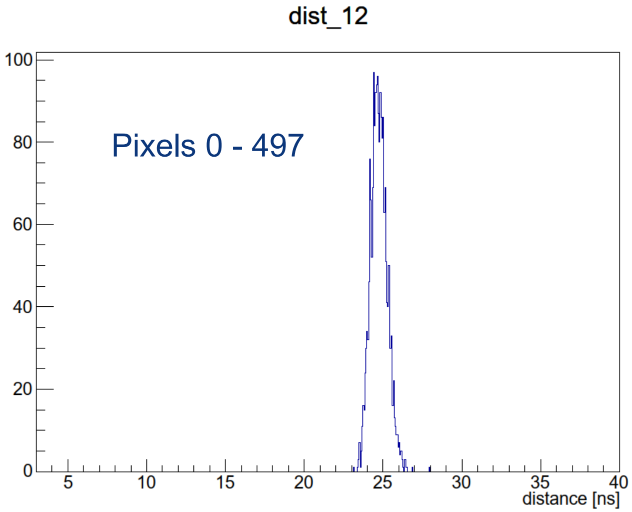
First results

Delay between the pixel on the top and different pixels within the column 0





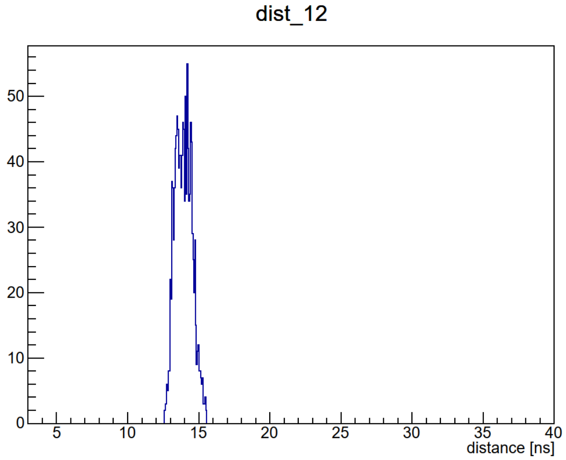


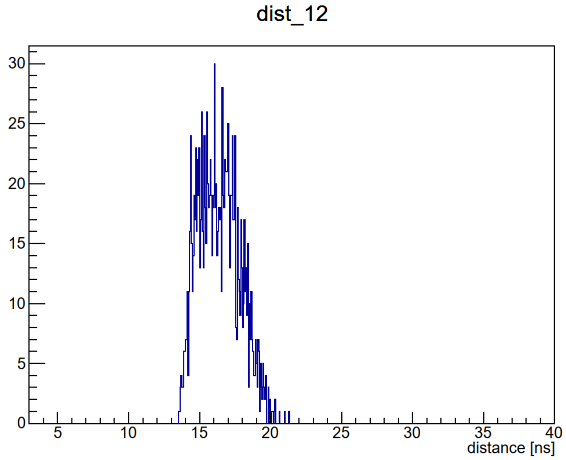


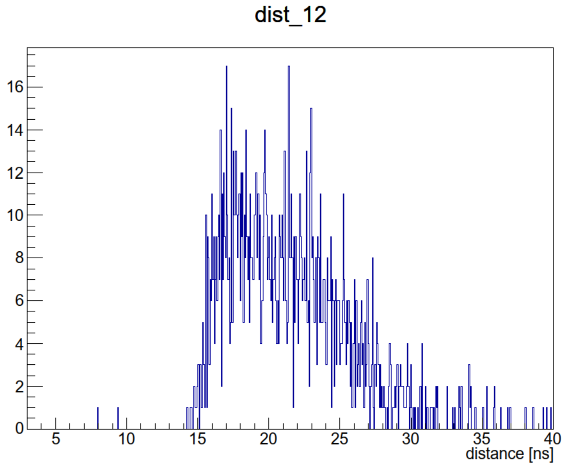
The delay takes into account the injection pulse delay up and the data propagation down the column.

First results

The distribution takes into account the jitter of the discriminator leading edge which is worse close to the threshold







For smaller pulses

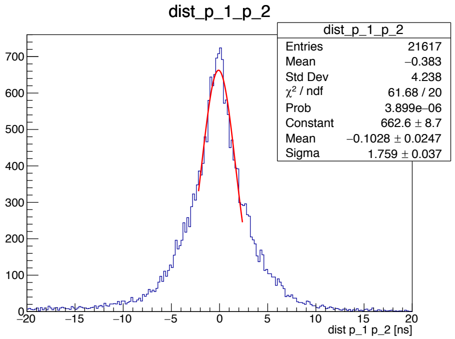
Longer tail towards higher values

Mean values increases

under investigation

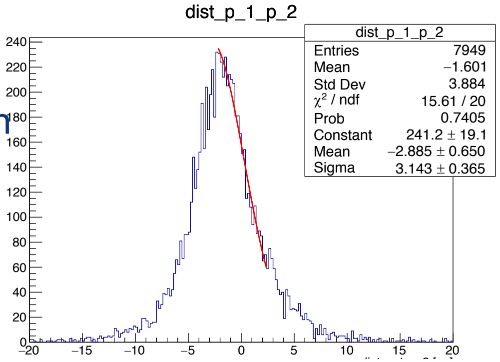
Resolution vs energy

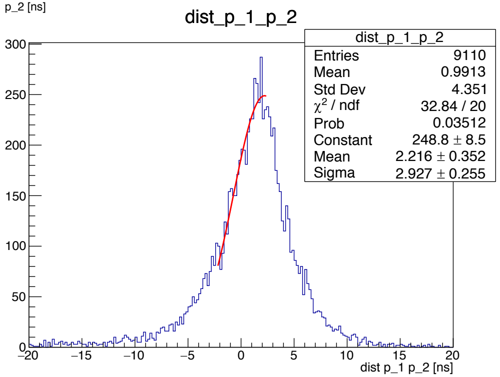
Artificially increasing the effect of the TW, things behave as expected.



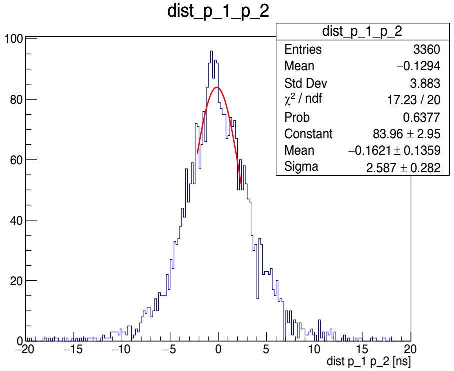
Considering events with at least 1 hit per plane

Considering events with at least 1 hit on the second but at least 2 on the first plane.





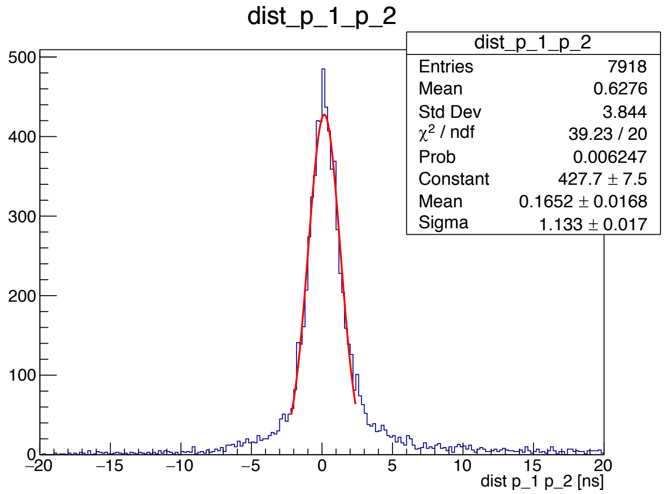
Considering events with at least 1 hit on the first but at least 2 on the second plane



Considering events with at least 2 hit on both planes

Summary

For high charge deposition the time resolution is in the order of one ns.



$$\sigma = \frac{1.133ns}{\sqrt{(2)}} \approx 800ps$$

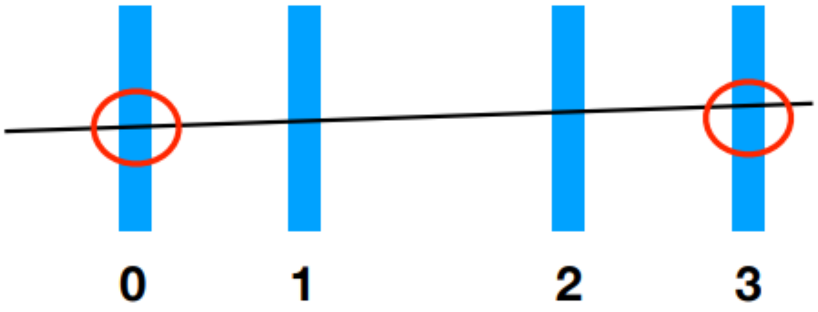
In-time efficiency with PicoTDC

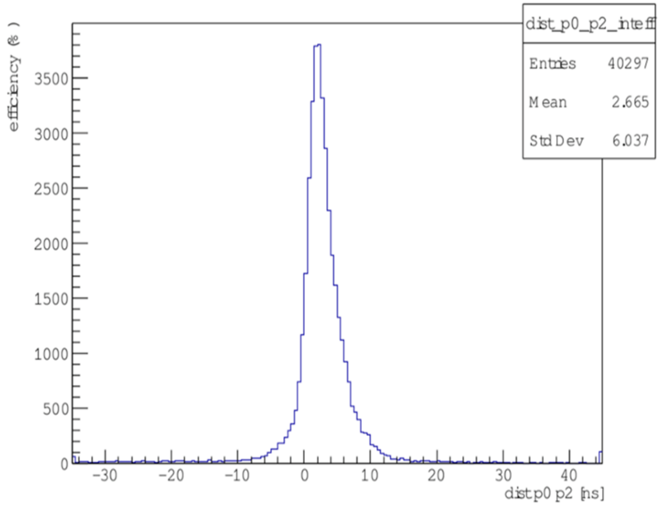
Important information can be extracted from PicoTDC analysis.

How to define a track:

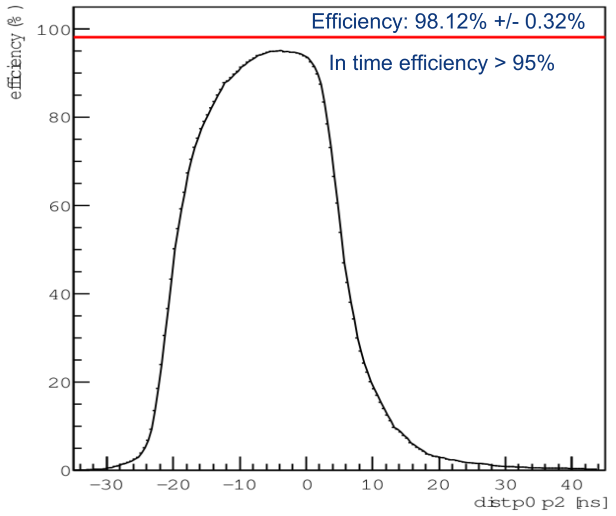
Require one hit on the first (origin) and last plane

Efficiency= fraction of tracks seen on other planes





Integration on a moving window of 25ns



Efficiency compatible with other analysis (see R. Cardella’s presentation)

Next step: correlation with position information to cut noisy hits.