Advances on Integration of Monolithic Silicon Sensors in Pixel Trackers

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ESR 9
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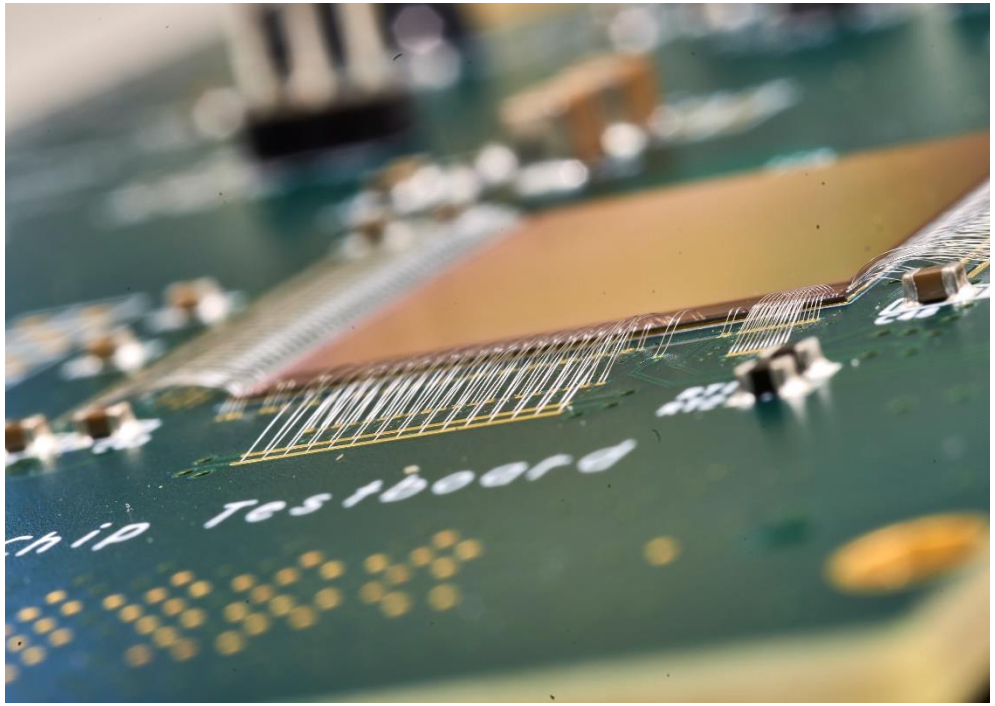
CERN EP-DT-DD

Outline

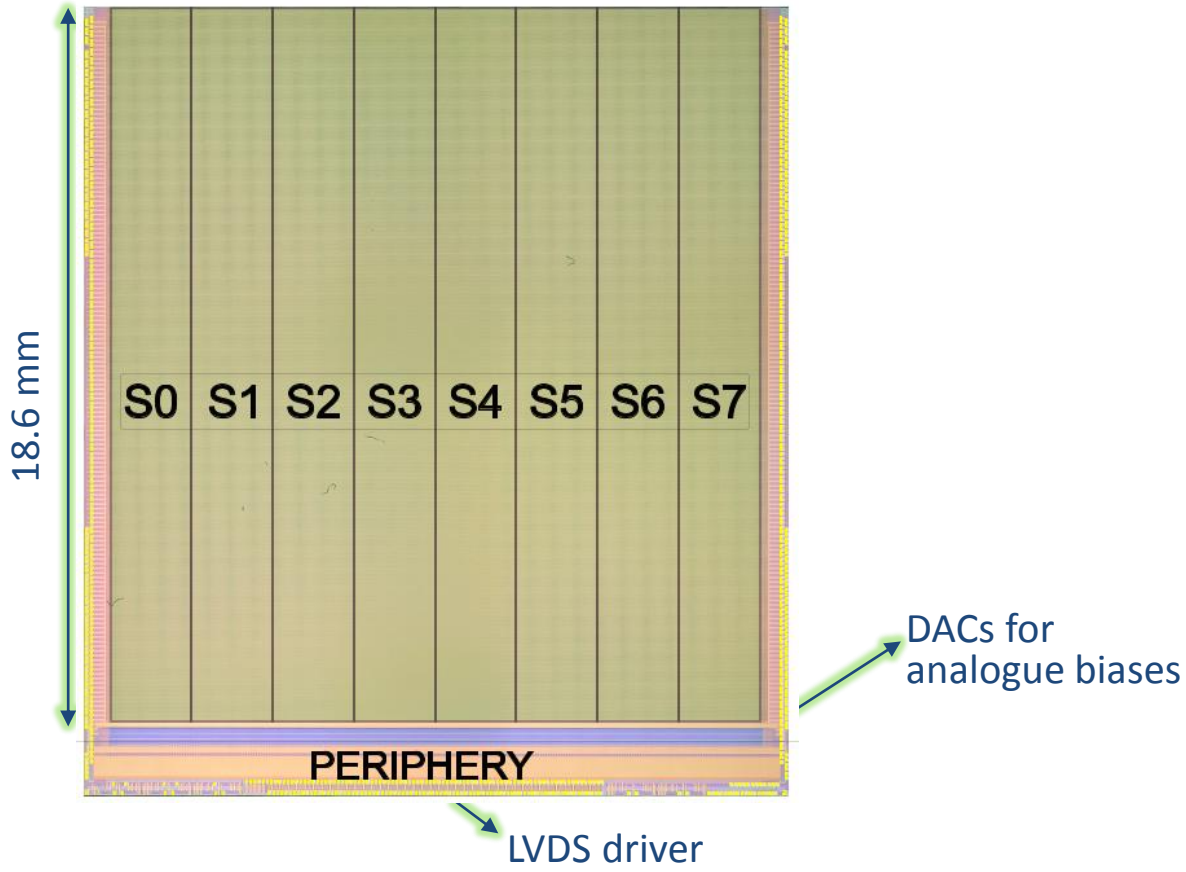
1. MALTA and MiniMALTA sensors
   - From Assembly to Efficiency
   - Rad Hardness studies
   - Improvements and MiniMalta
2. A large area CMOS module
   - Buried Microchannel in CMOS Devices
   - Chip To Chip Communication
   - High Speed Data Transmission in Trackers
3. Conclusions

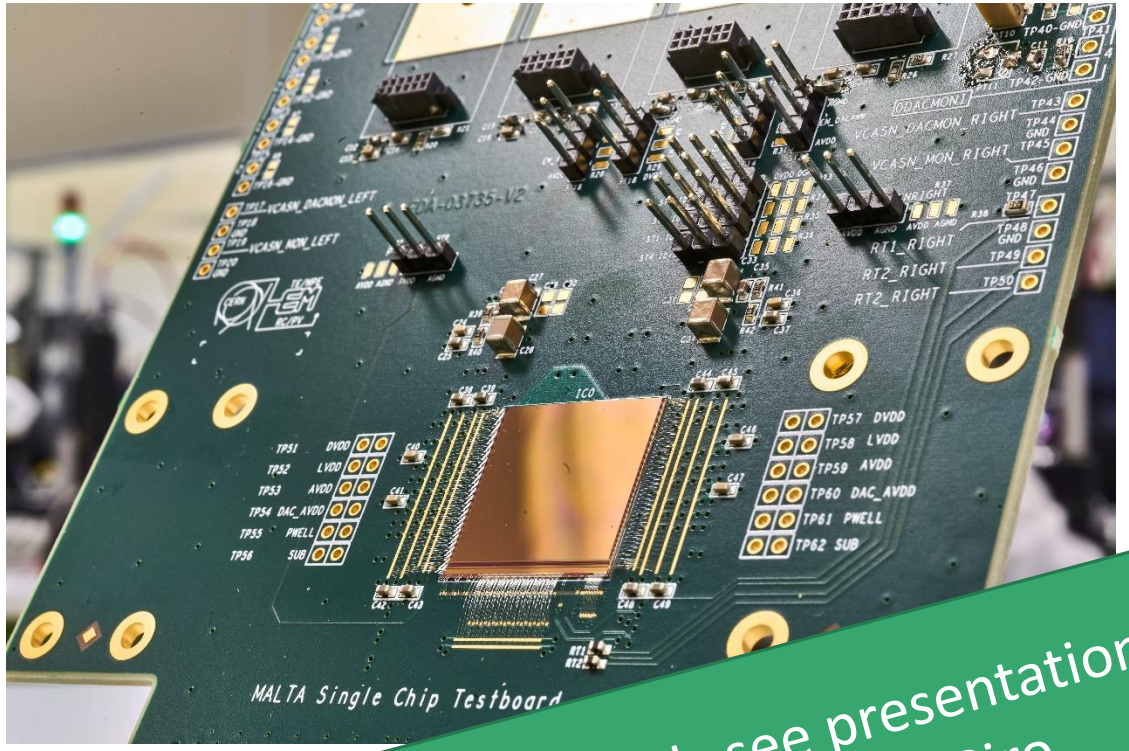


MALTA: Monolithic pixel detector from ALICE to ATLAS

The 512x512 pixel $36.4\ \mu m^2$ - 8 sectors

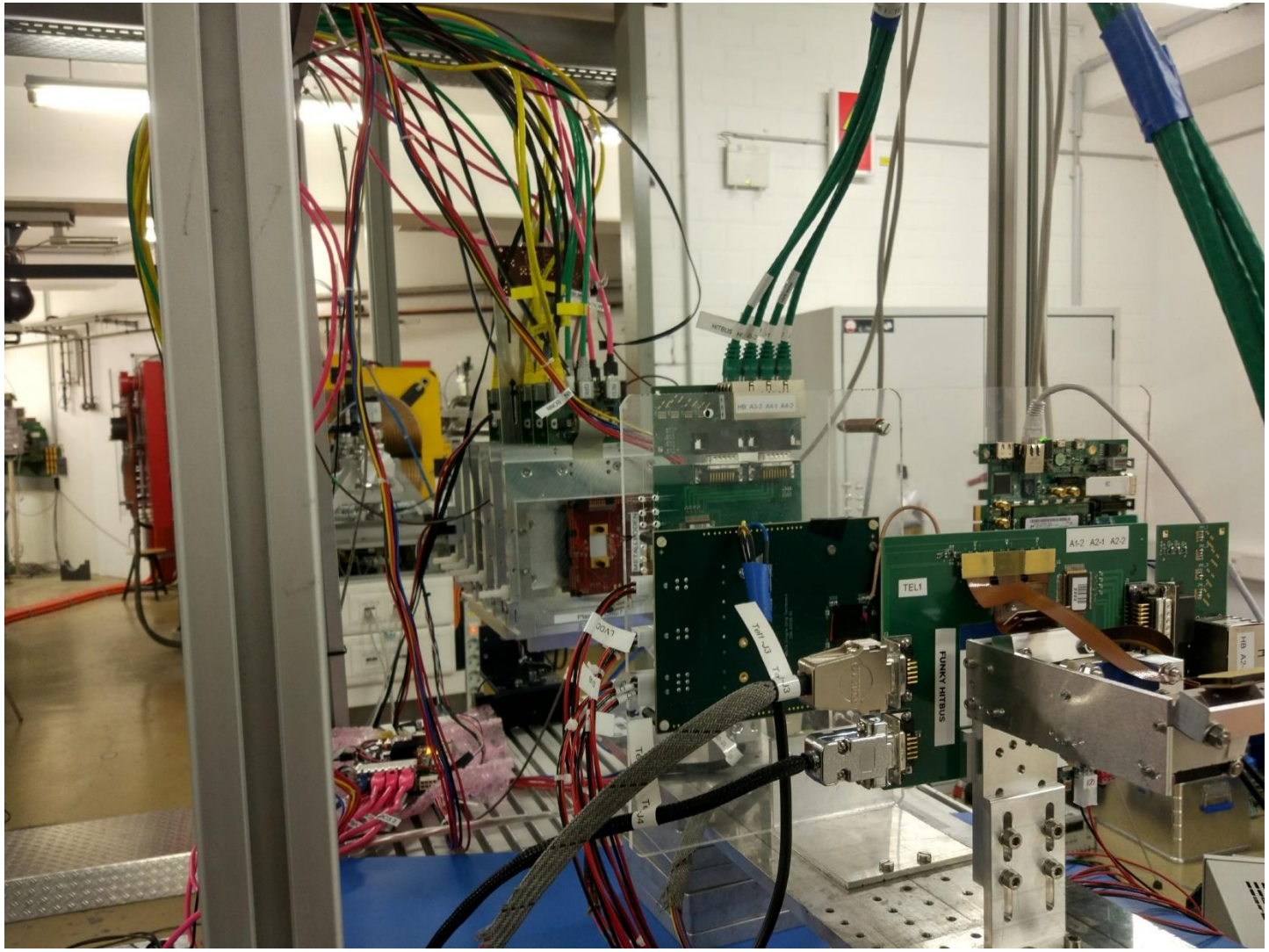
- Small collection electrode sensor (shared with MONOPIX)
- Low-power front-end (shared with MONOPIX)
- Novel Asynchronous Readout architecture





For more details see presentation of I.Berdalovic and F.Piro

Collection Efficiency Characterization - MALTA



ELSA-BONN Exposed MALTA to a 2.5 GeV electron beam during 3 days

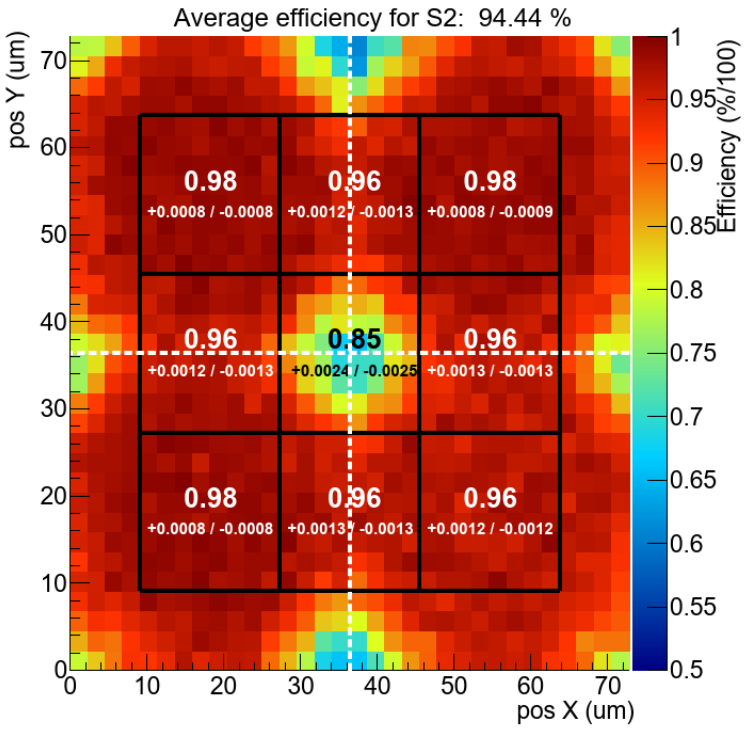
SPS- CERN Down to in-pixel efficiency

Target Efficiency

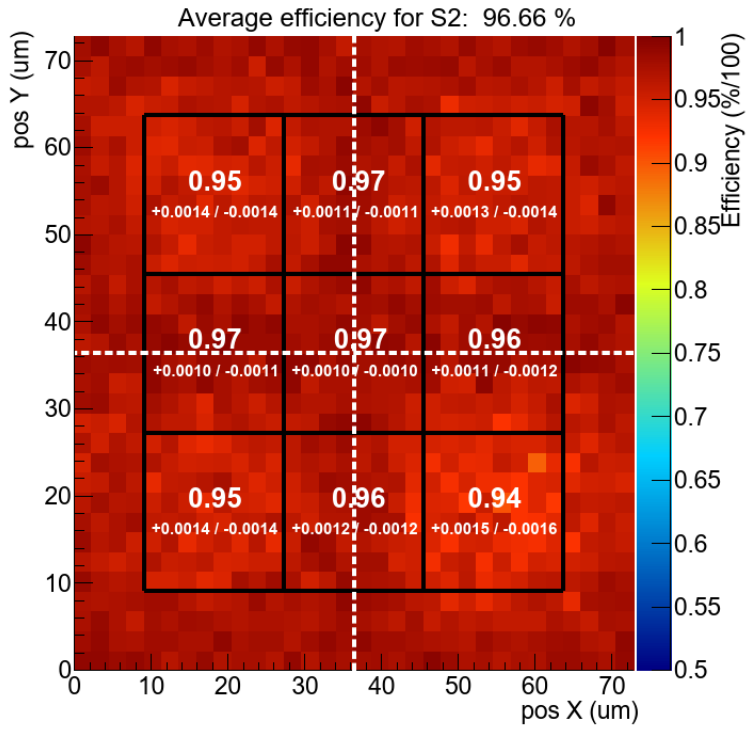
>97% after $1 \times 10^{15}\ n_{eq} cm^{-2}$

Collection Efficiency Characterization - MALTA

Unirradiated: lowering the threshold gives full efficiency



600 e^-



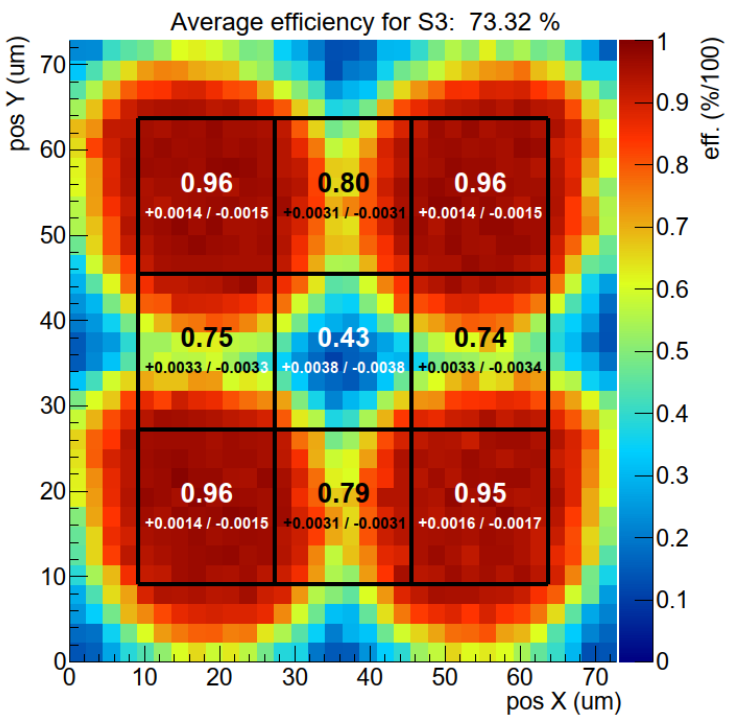
250 e^-

Cannot go lower with threshold because of RTS noise and masking issue

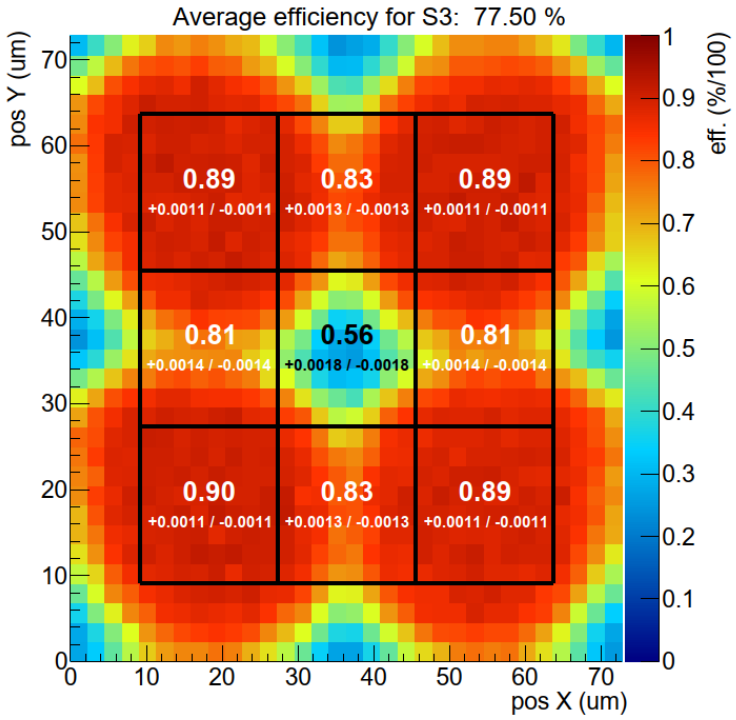
See I.Berdalovic presentation

Collection Efficiency Characterization - MALTA

Neutron irradiation $1 \times 10^{15} n_{eq} cm^{-2}$: maximum efficiency 77%



(a) $320\,\mathrm{e}^-$

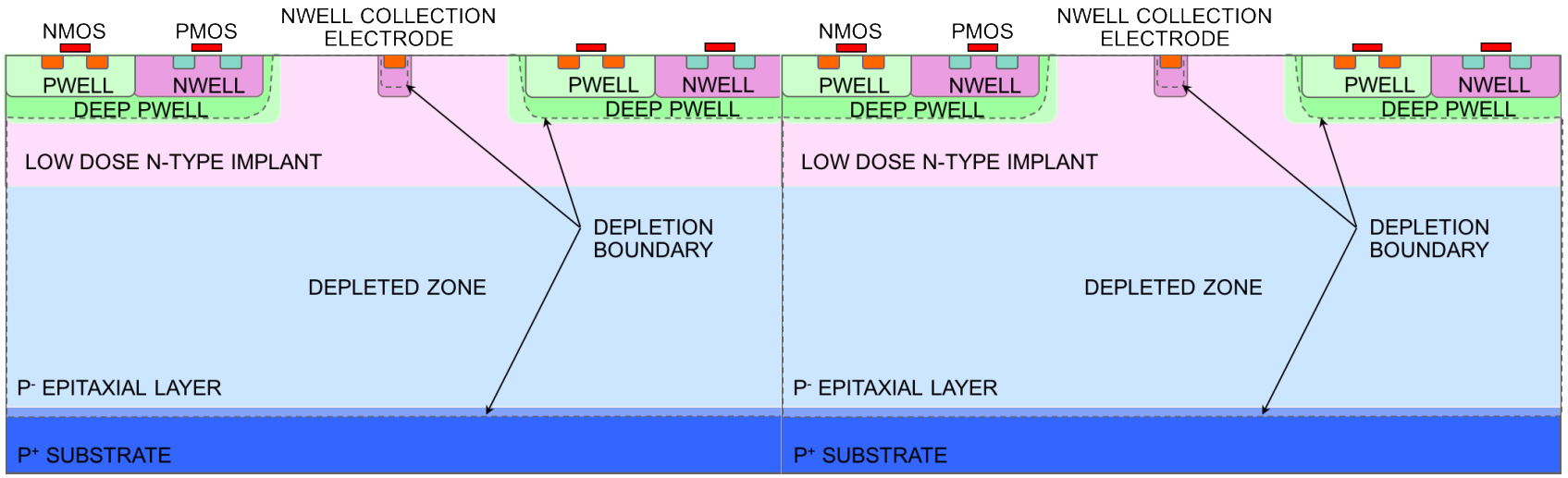


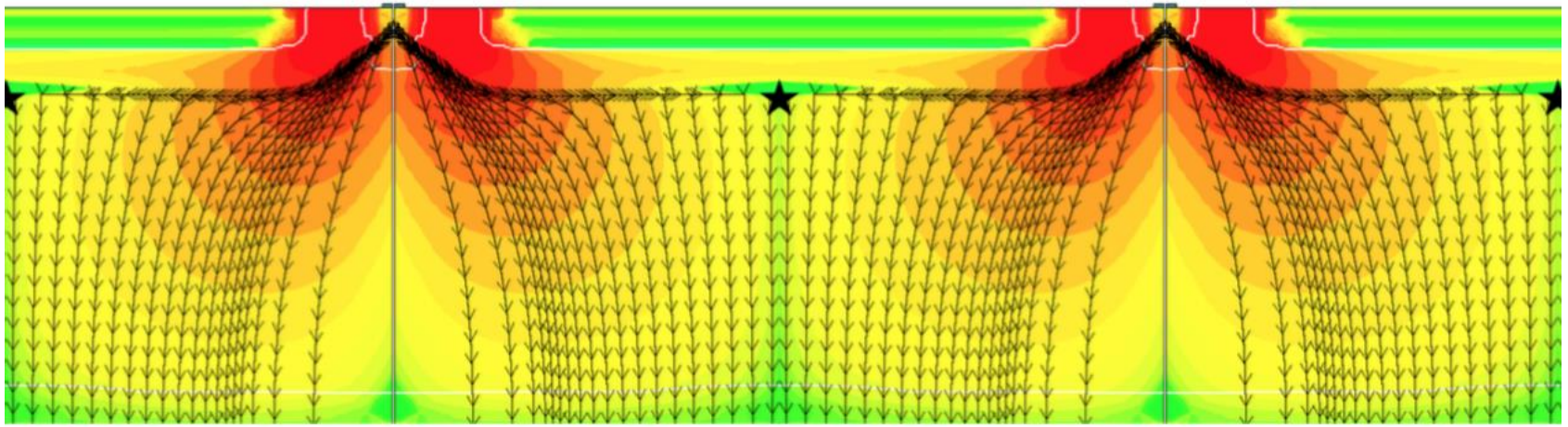
(d) $250\,\mathrm{e}^-$

Cannot go lower with threshold because of RTS noise and masking issue

See I.Berdalovic presentation

Efficiency Loss After Irradiation





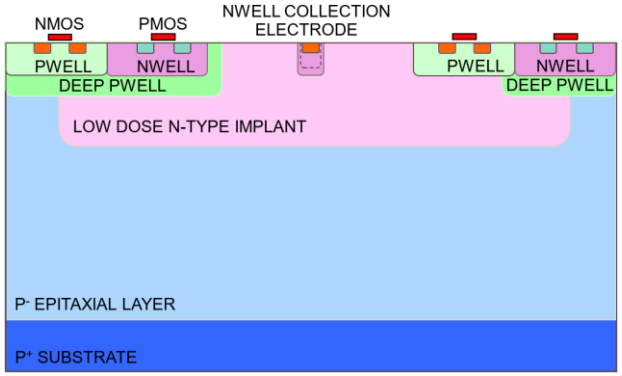
Very low electric field at the edge of the pixel causes charge loss after irradiation.

Same results with TJ-MONOPIX (I.Caicedo presentation)

Pixel design improvements

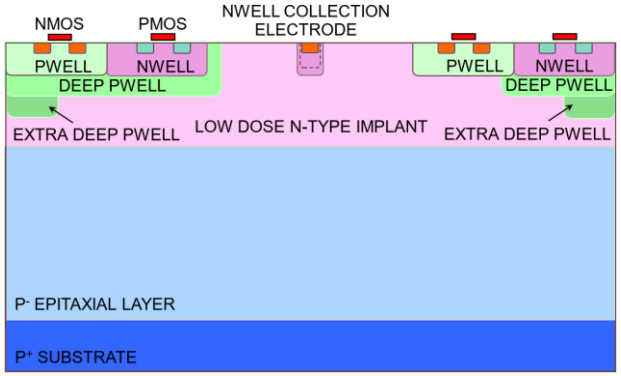
Additional “extra-deep p-well” layer

- Already known by TowerJazz: no process R&D needed

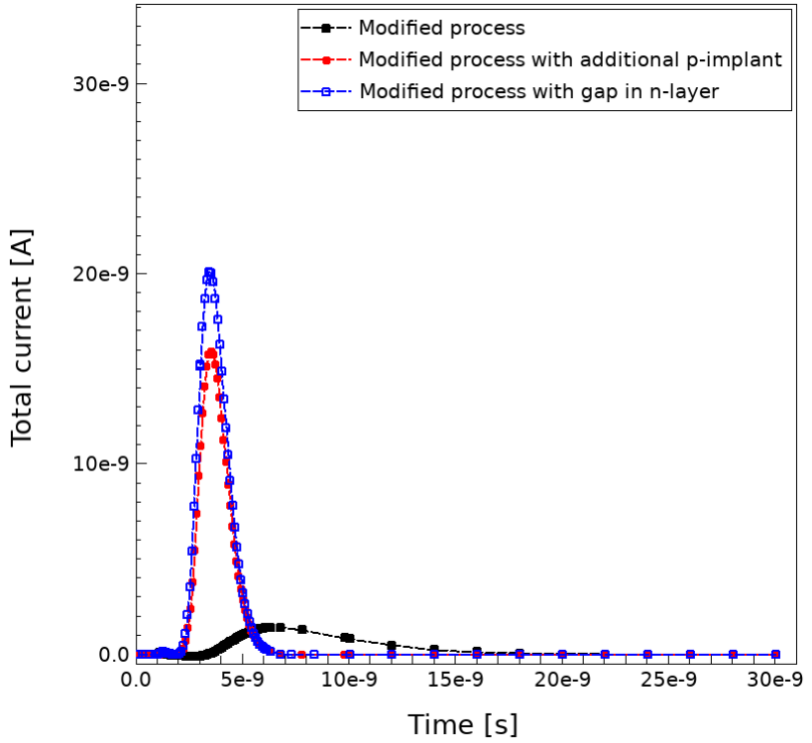


Gap in the n- layer

- requires only a change of the existing mask for the n-layer



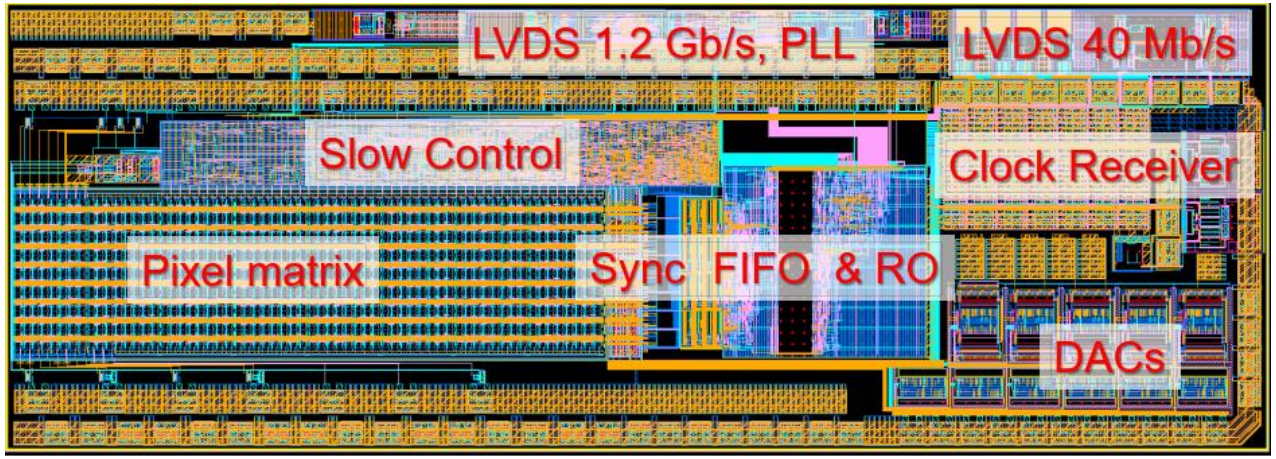
After irradiation simulated current pulse



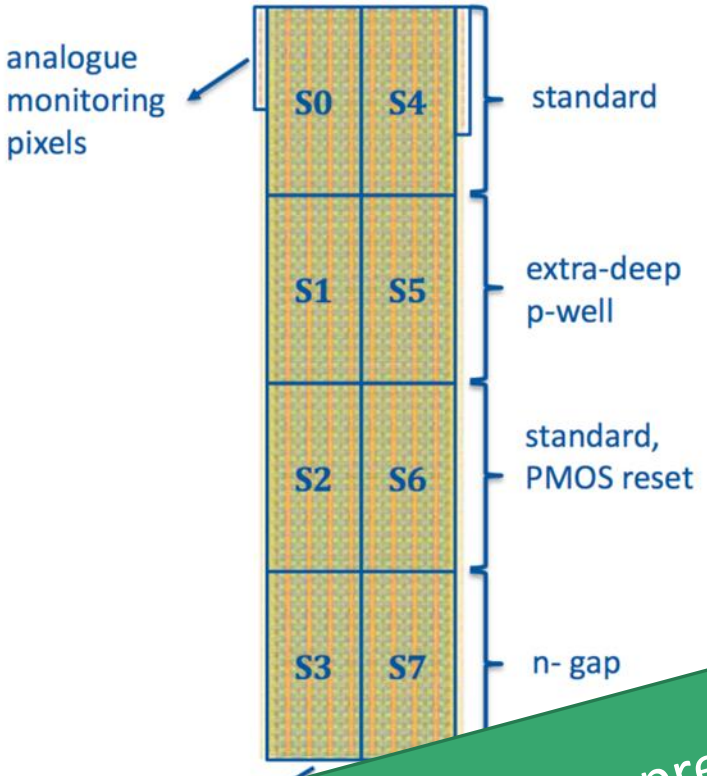
Magdalena Munker

Mini MALTA pixel matrix

- Pixel size: 36.4 µm x 36.4 µm
- 64x16 pixel matrix includes 8 sectors with splits on analogue front-end design, reset mechanism and process



MiniMALTA with synchronization
and fixes for improved charge collection



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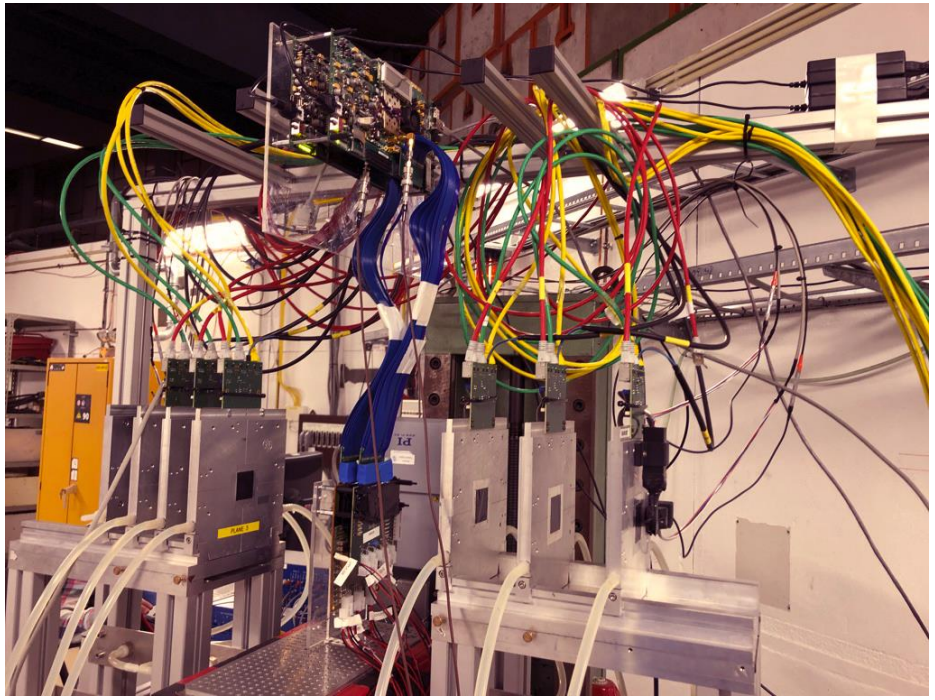
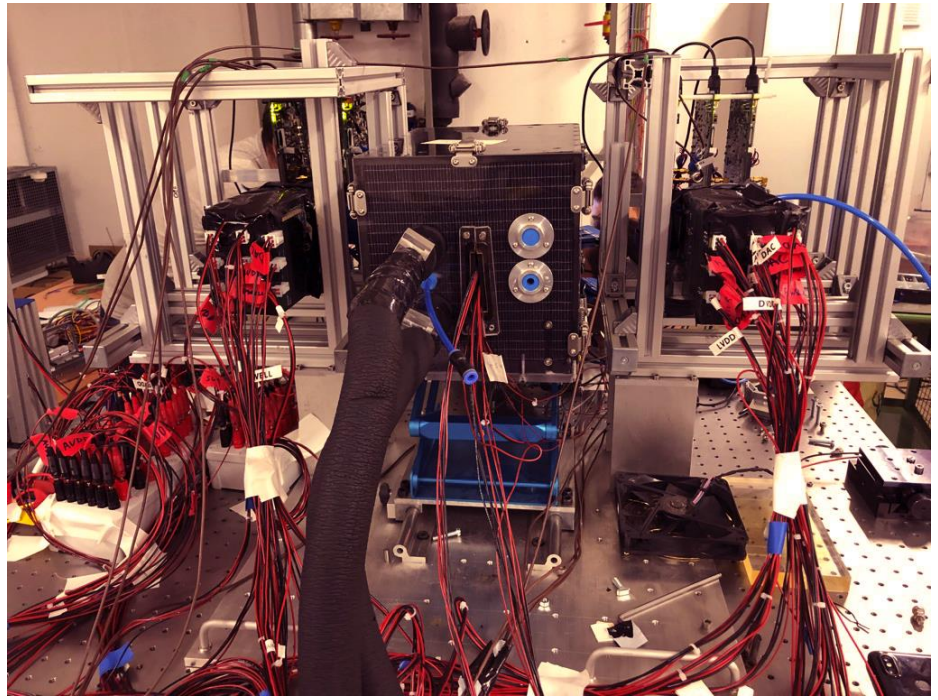
Testbeam campaigns



EUDAQ DURANTA telescope in DESY



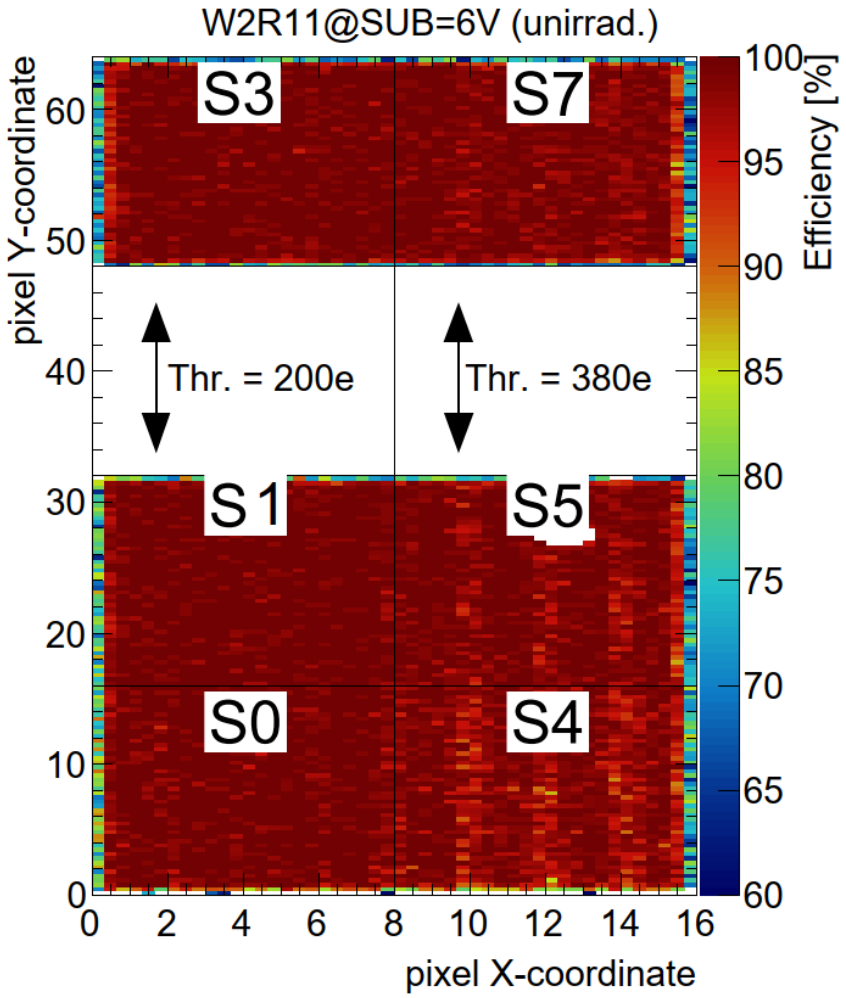
MALTA telescope in ELSA

Mini MALTA Collection Efficiency

Before Irradiation

Sector ID	Front-End	Sensor	Reset Mechanism
S0	Enlarged	Standard	Diode
S1	Enlarged	Extra Deep p-well	Diode
S2	Enlarged	Standard	PMOS
S3	Enlarged	n^- Fap	Diode
S4	Standard	Standard	Diode
S5	Standard	Extra Deep p-well	Diode
S6	Standard	Standard	PMOS
S7	Standard	n^- Gap	Diode

Process modification	Efficiency (enlarged trans. region) [%] / threshold [e^-]	Efficiency (standard trans. region) [%] / threshold [e^-]
n-gap	99.6 ± 0.1 / $200e^-$	99.1 ± 0.1 / $380e^-$
extra deep p-well	99.6 ± 0.1 / $200e^-$	98.9 ± 0.1 / $380e^-$
continuous n^-	99.6 ± 0.1 / $200e^-$	97.9 ± 0.1 / $380e^-$



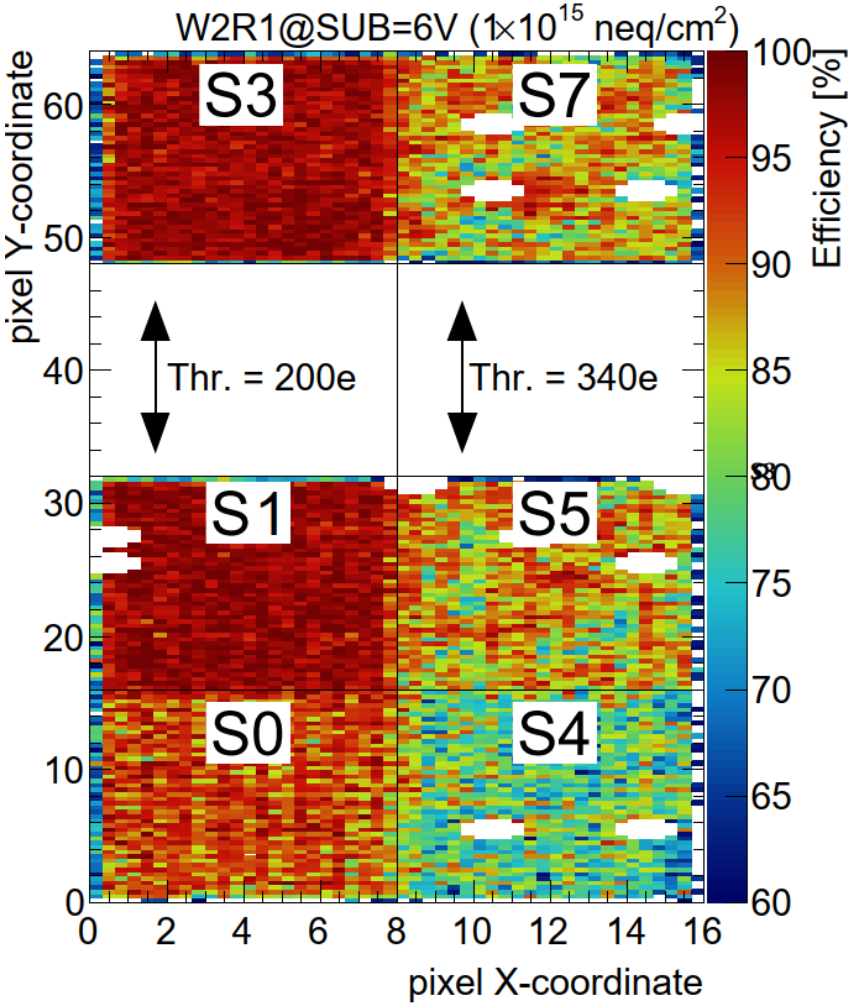
Mini MALTA Collection Efficiency

Neutron Irradiated

$1 \times 10^{15} n_{eq} cm^{-2}$

Sector ID	Front-End	Sensor	Reset Mechanism
S0	Enlarged	Standard	Diode
S1	Enlarged	Extra Deep p-well	Diode
S2	Enlarged	Standard	PMOS
S3	Enlarged	n^- Fap	Diode
S4	Standard	Standard	Diode
S5	Standard	Extra Deep p-well	Diode
S6	Standard	Standard	PMOS
S7	Standard	n^- Gap	Diode

Process modification	Efficiency (enlarged trans. region) [%] / threshold [e^-]	Efficiency (standard trans. region) [%] / threshold [e^-]
n-gap	97.6 ± 0.1 / 105e^-	86.5 ± 0.1 / 210e^-
extra deep p-well	97.9 ± 0.1 / 105e^-	87.0 ± 0.1 / 210e^-
continuous n^-	91.9 ± 0.1 / 105e^-	78.8 ± 0.2 / 210e^-



Mini MALTA Collection Efficiency

Neutron Irradiated

$1 \times 10^{15} n_{eq} cm^{-2}$

Sector ID	Front-End	Sensor	Reset Mechanism
S0	Enlarged	Standard	Diode
S1	Enlarged	Extra Deep p-well	Diode
S2	Enlarged	Standard	PMOS
S3	Enlarged	n^- Fap	Diode
S4	Standard	Standard	Diode
S5	Standard	Extra Deep p-well	Diode
S6	Standard	Standard	PMOS
S7	Standard	n^- Gap	Diode

Process modification	Efficiency (enlarged trans. region) [%] / threshold [e^-]	Efficiency (s… trans. region) [%] / threshold [e^-]
n-gap	97.6 ± 0.1 / 105e^-	86.5 ± 0.1 / 210e^-
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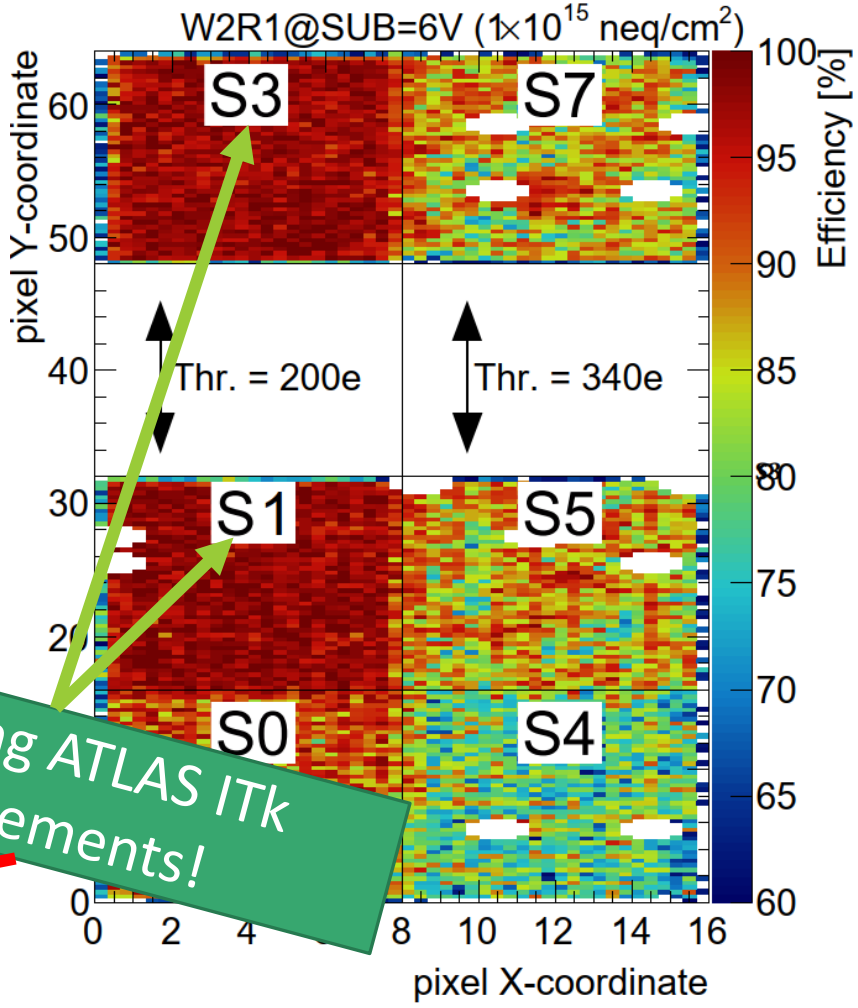
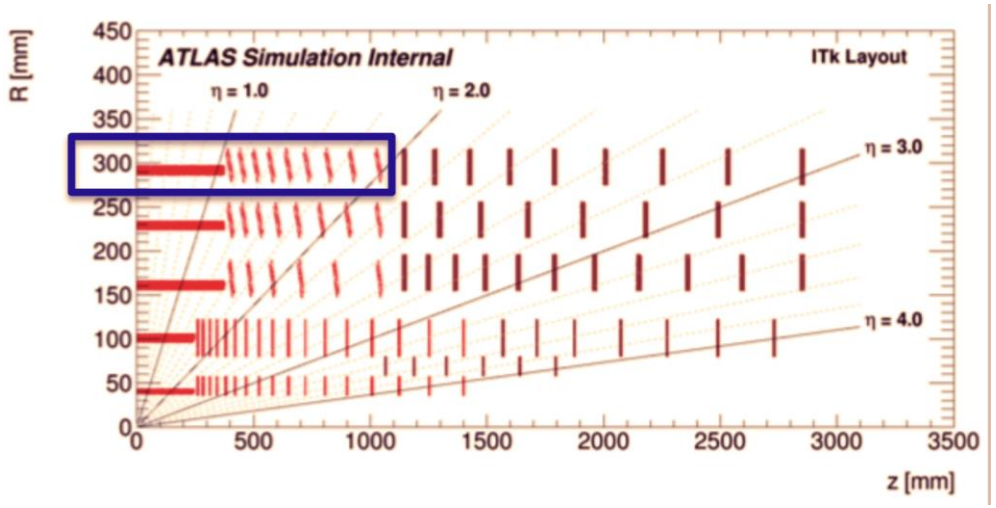


Matching ATLAS ITk requirements!

CMOS development for the ATLAS ITk

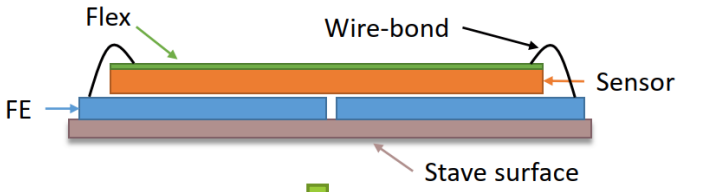
Outermost layer of ITk Pixel Barrel

- 2016 quad modules
- 3m^2 (~45% of outer barrel layers)

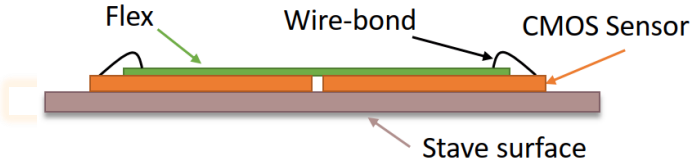


Monolithic CMOS sensors were considered as option for the outermost layer

- Saves bump bonding for ~45% of outer barrel system
- Substantial cost reduction and reduced module assembly time
- Requires “Drop-In” module compatibility to hybrid module



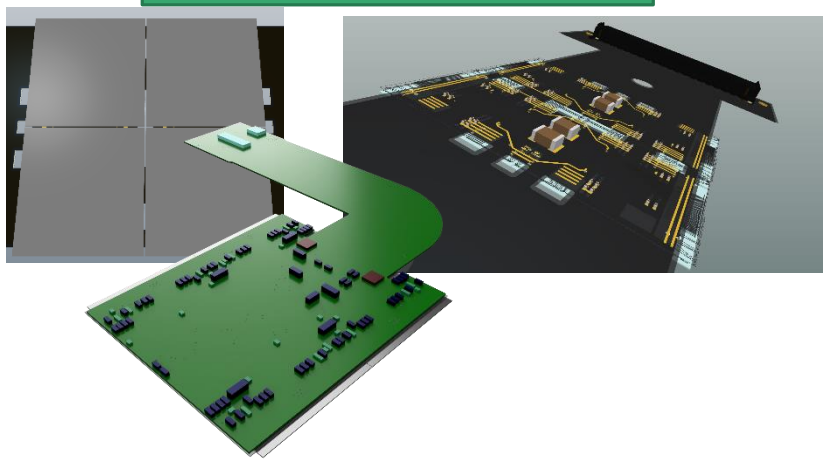
Hybrid Module



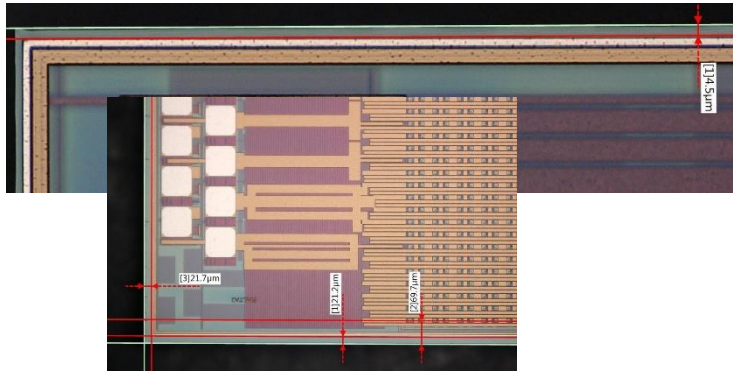
Monolithic Module

Integrating a CMOS Module in a Tracker

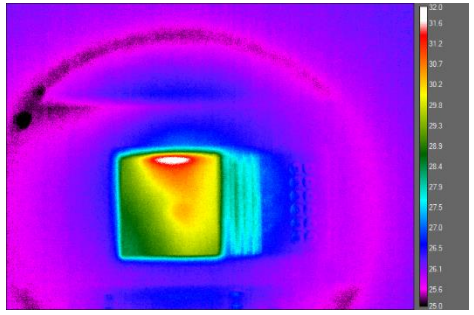
Module Design



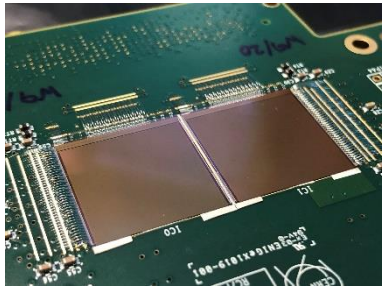
Dead Area Minimization

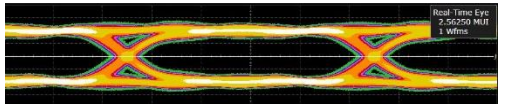


Sensor cooling



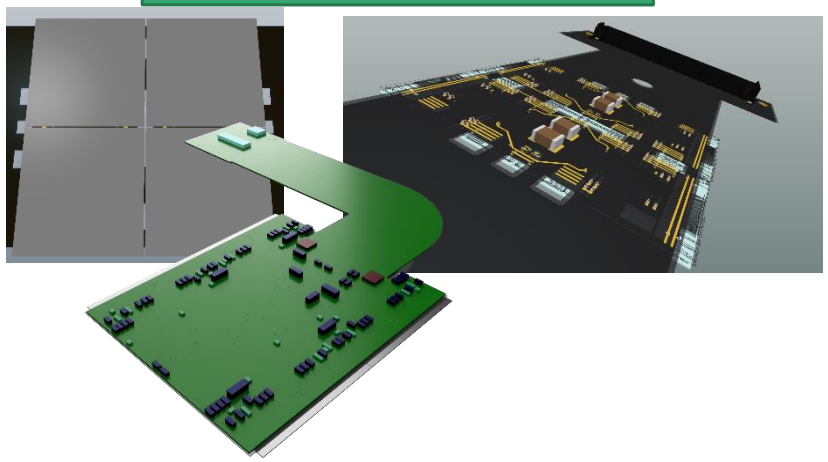
Data Transmission





Integrating a CMOS Module in a Tracker

Module Design



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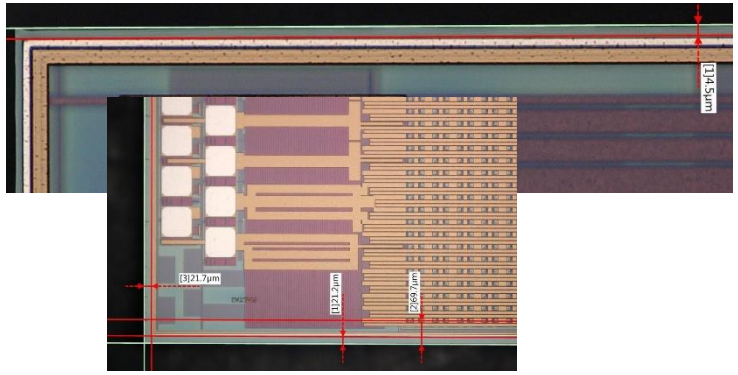

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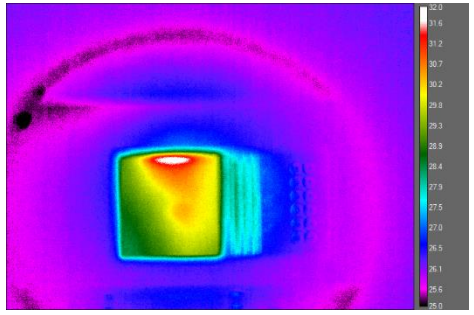

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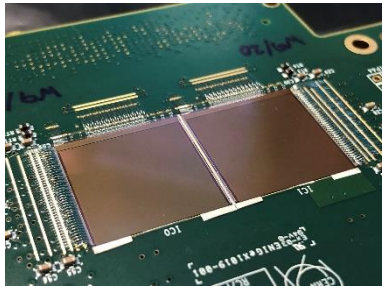
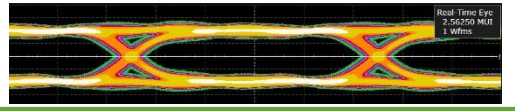




Sensor Cooling in HEP

Pixels operated at -30 ˚C to avoid thermal runaway

Critical Parameters

- Good thermal conductivity
- Low thermal expansion mismatch between parts
- Integration with mechanics

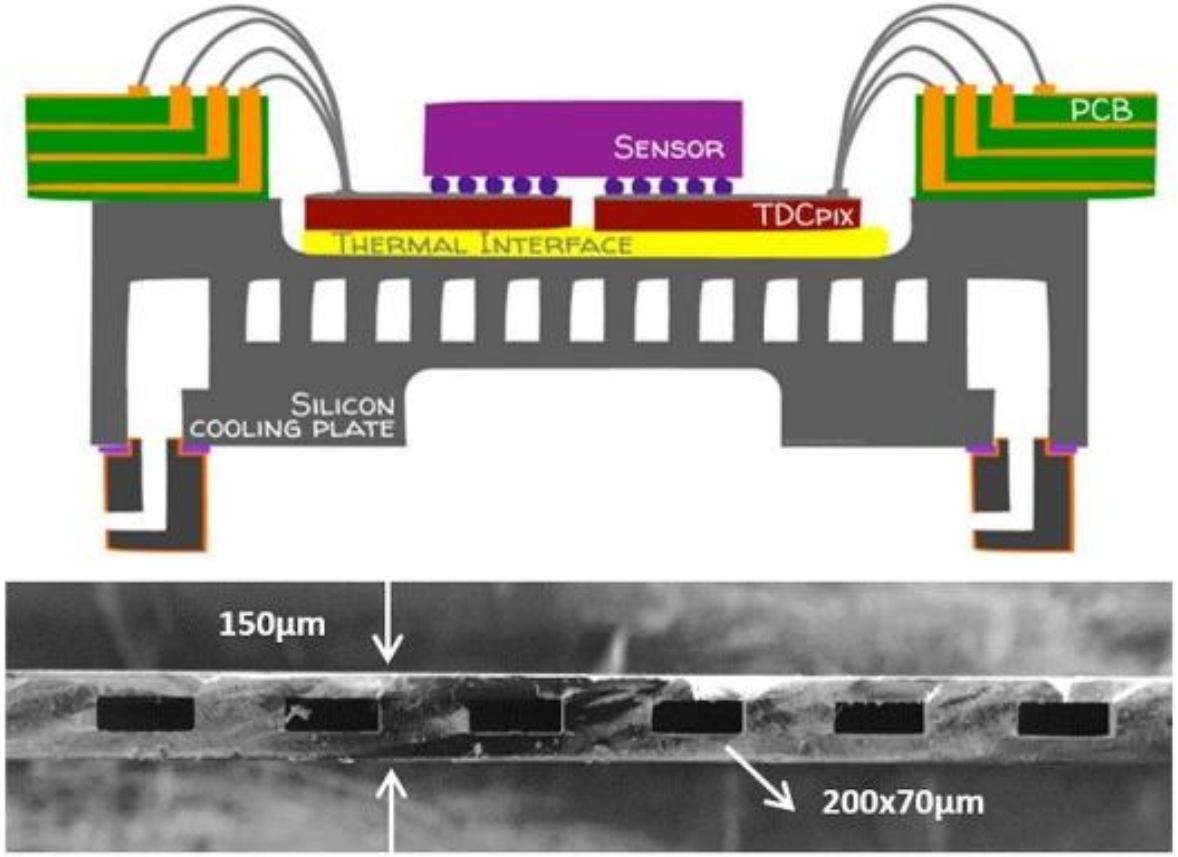
Embedding the channels in the sensor!

Could improve all the three parameters

Buried Channels Technology (BCT)

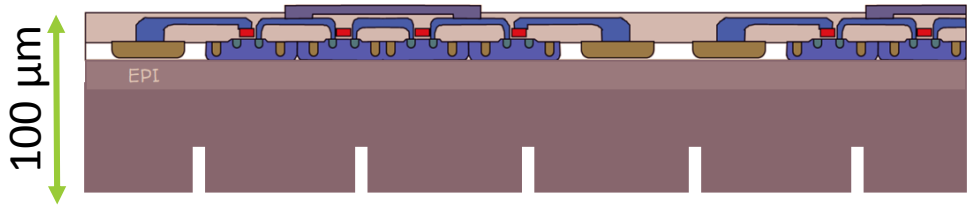
J. Bronuzzi, R. Callegari, R. Cardella, C. Lipp, A. Mapelli, P. Riedler

NA62 Hybrid with Silicon Cooling Plate

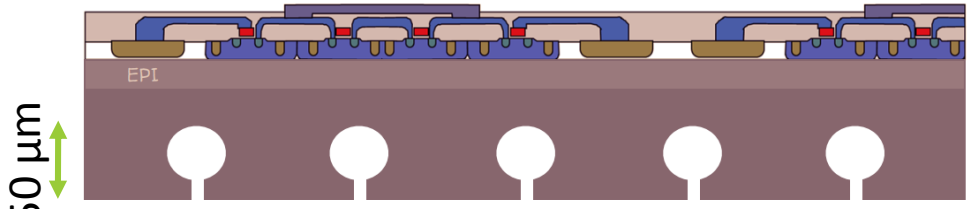


BCT Process

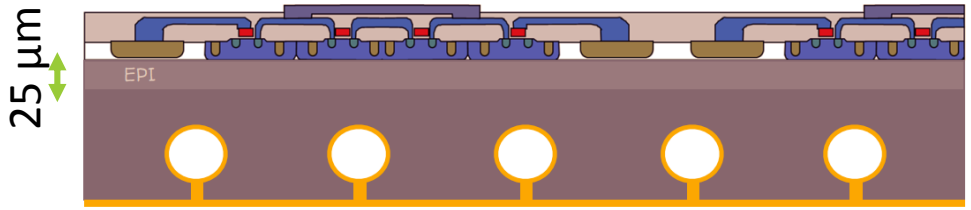
Processed at the CMI – EPFL, Lausanne



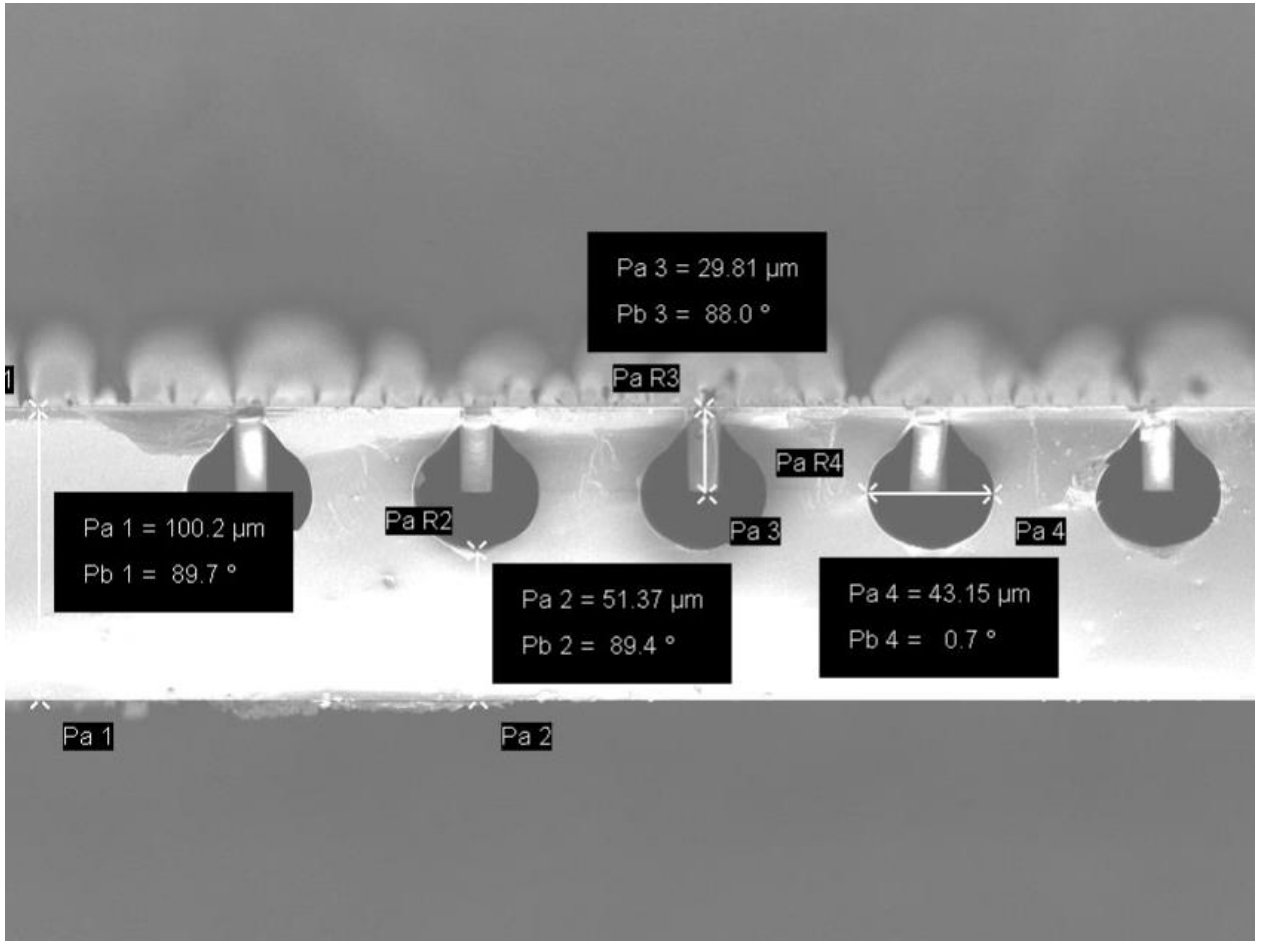
DRIE of 30 µm deep trenches (3 x 10 µm)



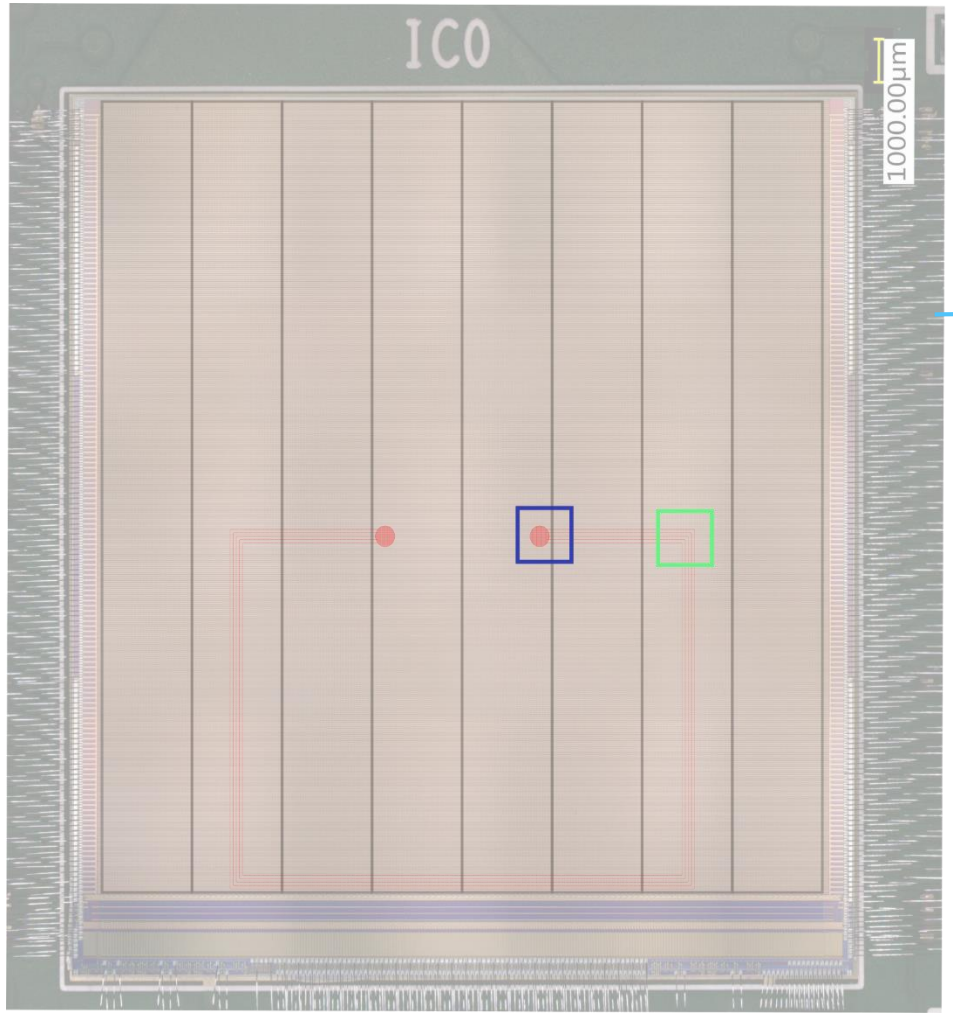
XeF_2 etching of microchannels (diam. 40 µm)

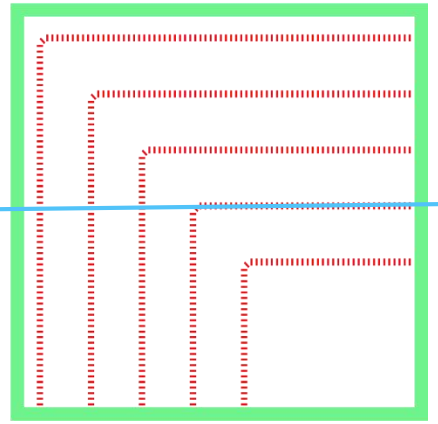


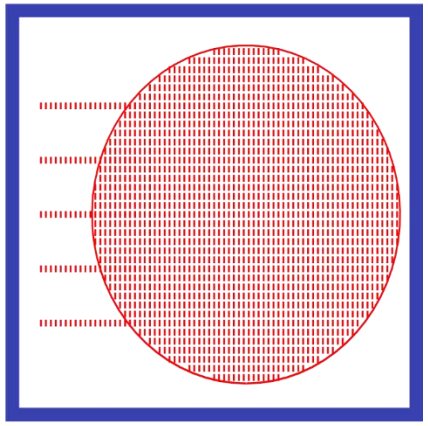
Trenches filled with Parylene (5 µm)

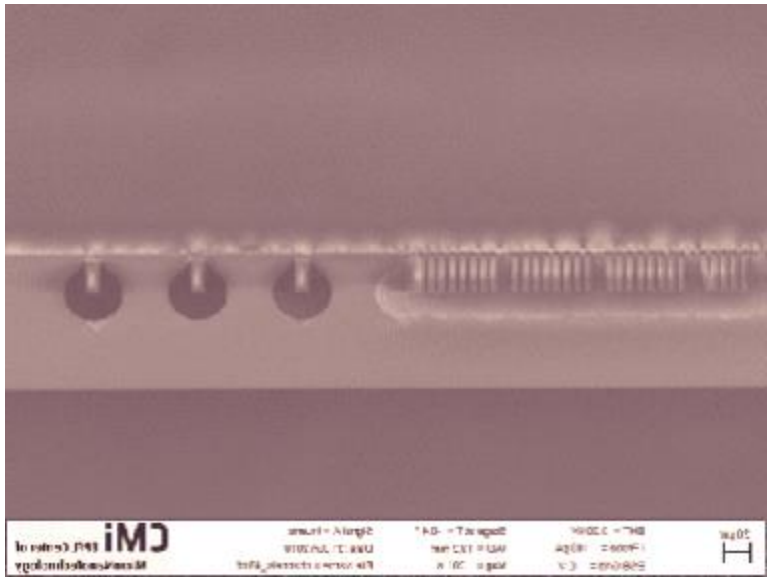


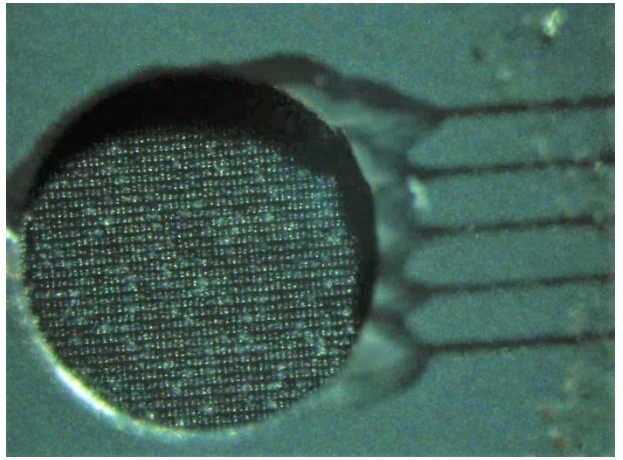
MALTA with BCT



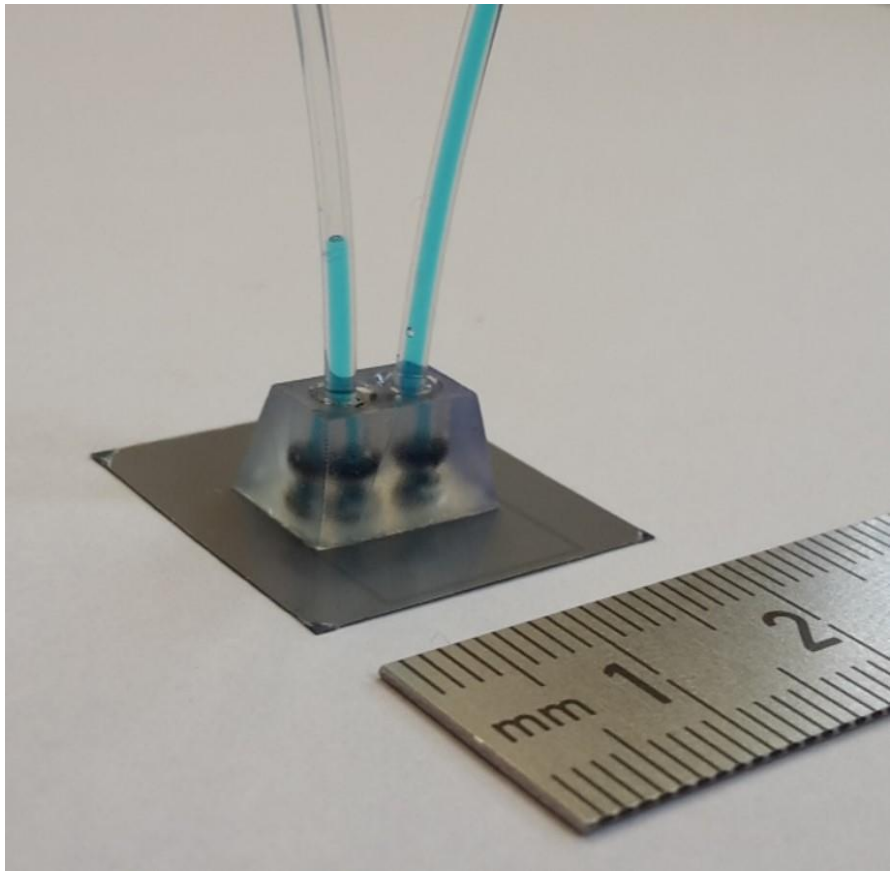


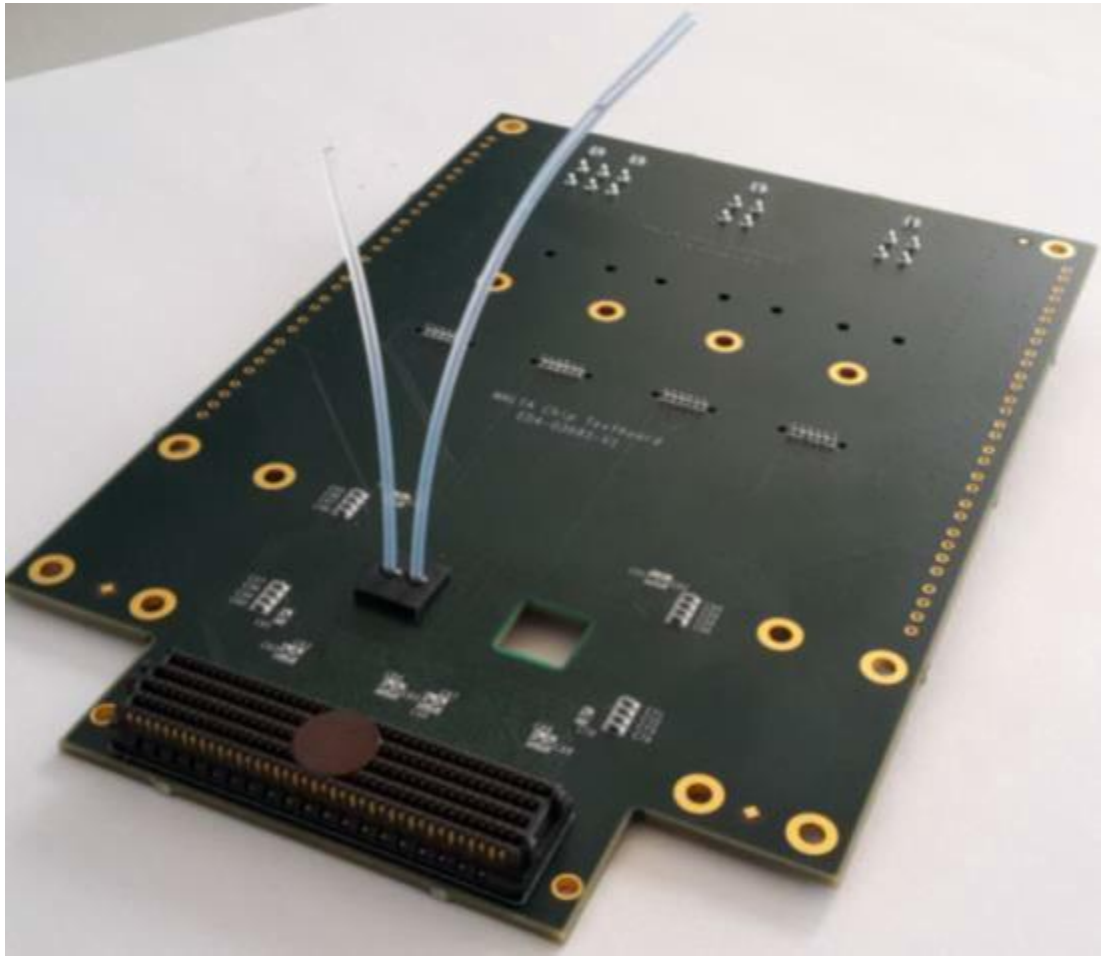


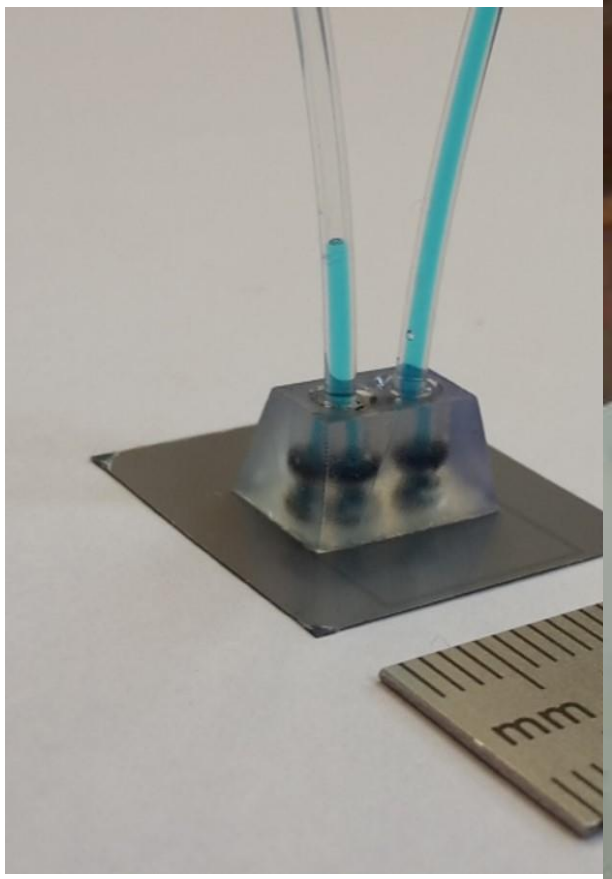


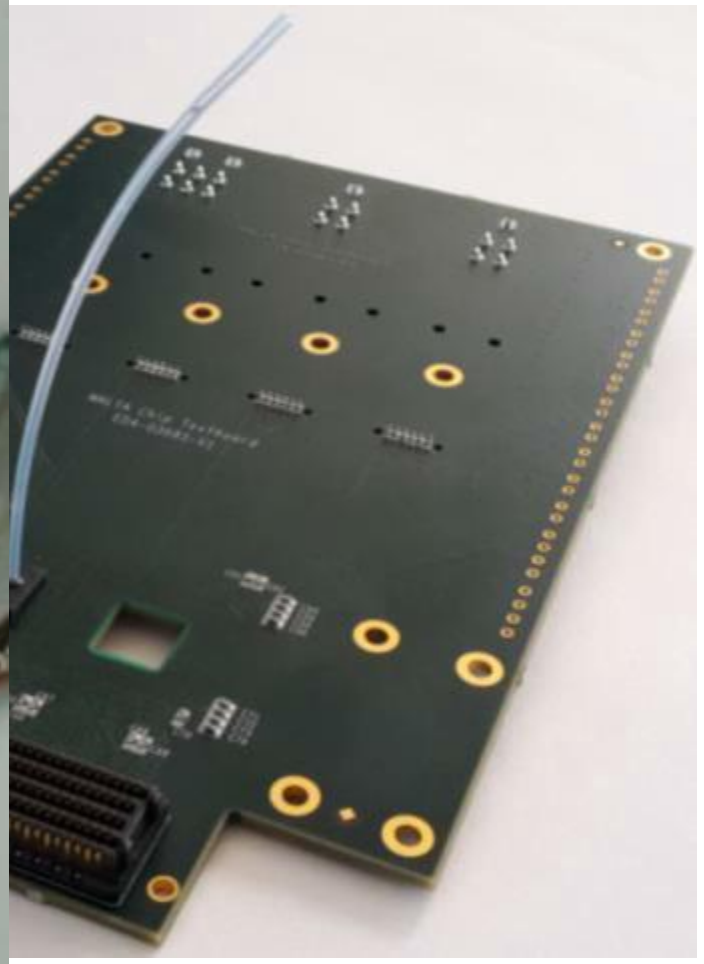


MALTA with BCT

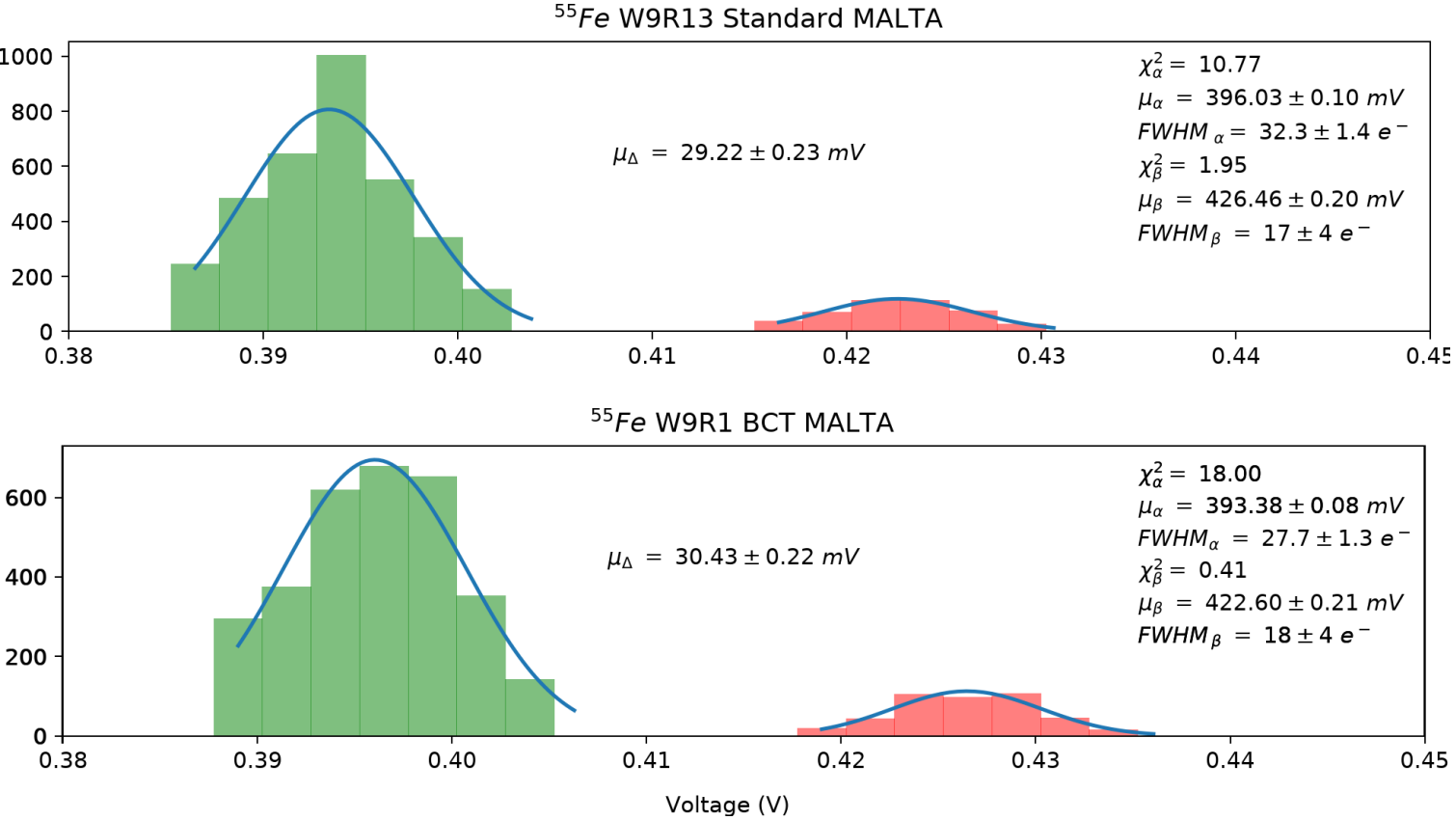





mm



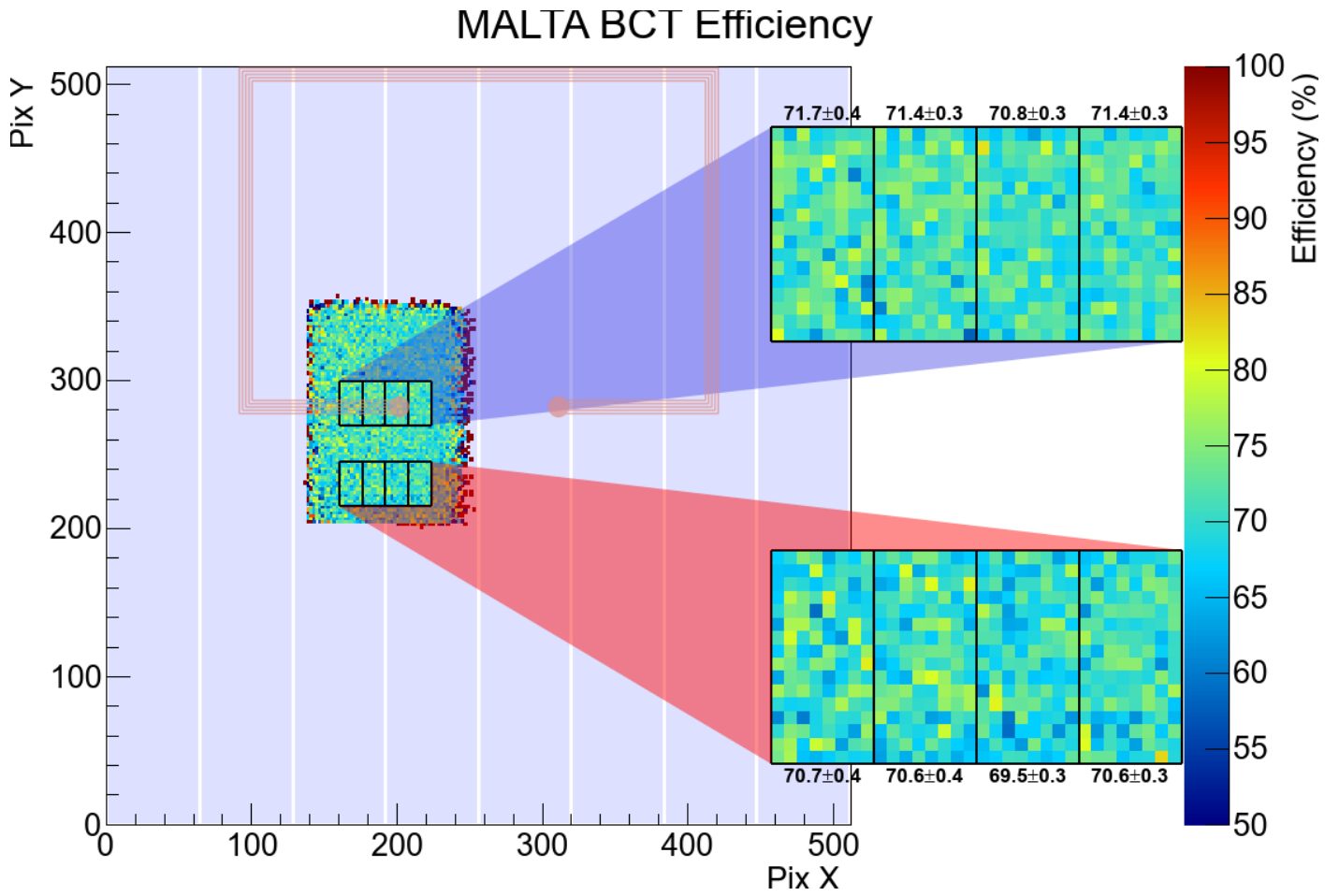
MALTA with BCT – Functional Test



^{55}Fe source scan

- Peaks fit comparable
- Distance of the peaks within the gain dispersion of MALTA

MALTA with BCT – Functional Test



^{55}Fe source scan

- Peaks fit comparable
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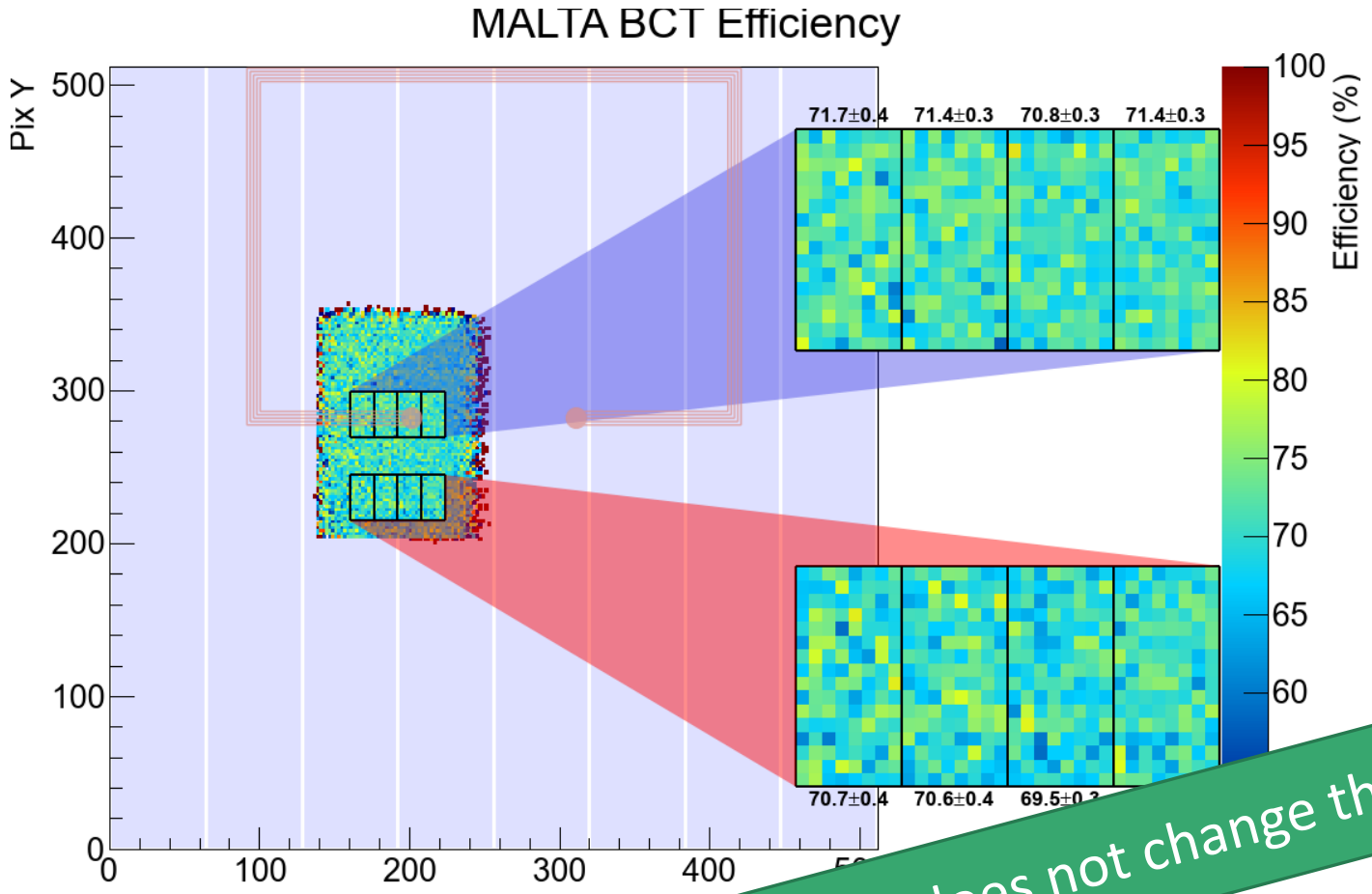
Collection Efficiency

- Readout issue reduced the efficiency of ALL detectors to ~70%
- Comparable efficiency for the different ROIs

MALTA with BCT – Functional Test



^{55}Fe source scan

- Peaks fit comparable
- Distance of the peaks within the gain dispersion of MALTA

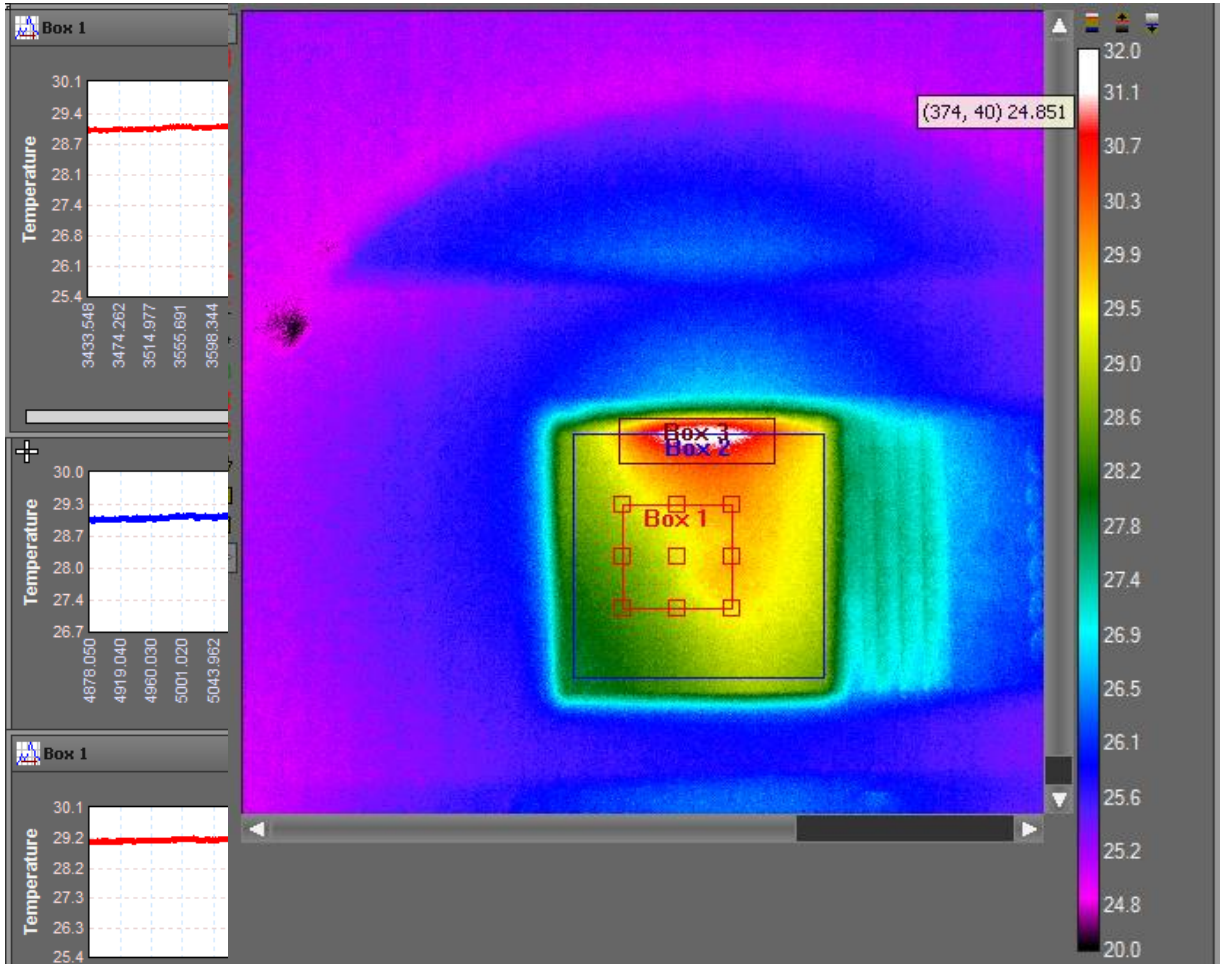
Collection Efficiency

- Readout issue reduced the efficiency of ALL detectors to ~70%
- Comparable efficiency [illegible] the different RO[illegible]

BCT process does not change the device performance!

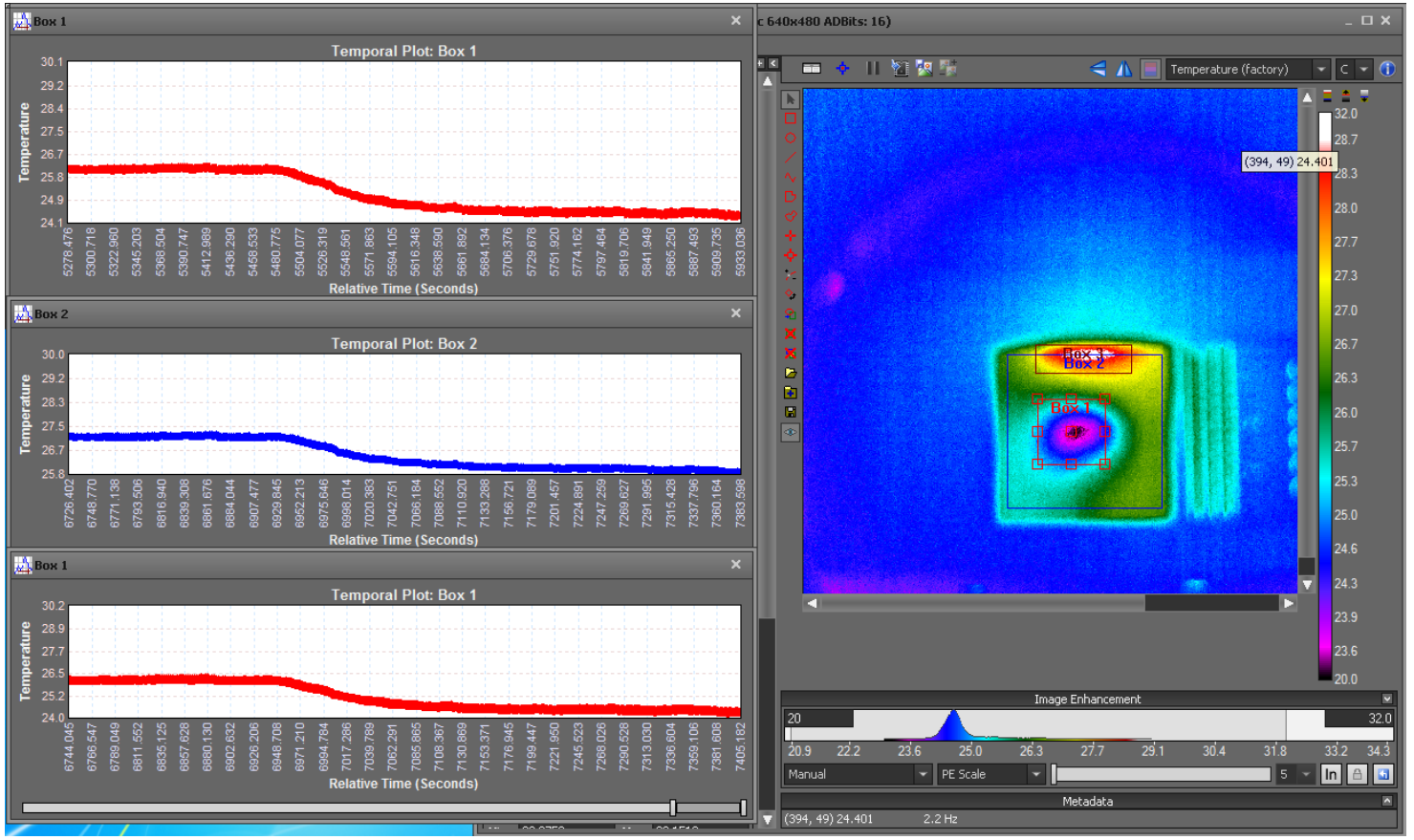
BCT Thermal Test - No Cooling

Hot area about 29˚C



5ml/min -> 10 ml/min

Hot area from 29˚C to 25˚C, using “fresh” water



Data Transmission from Module

HEP pixel trackers need to cope with very high hit rate

The modules need to transmit data over a long distance at high speed
ATLAS ITk FE maximum data rate 5 Gb/s

High power consumption

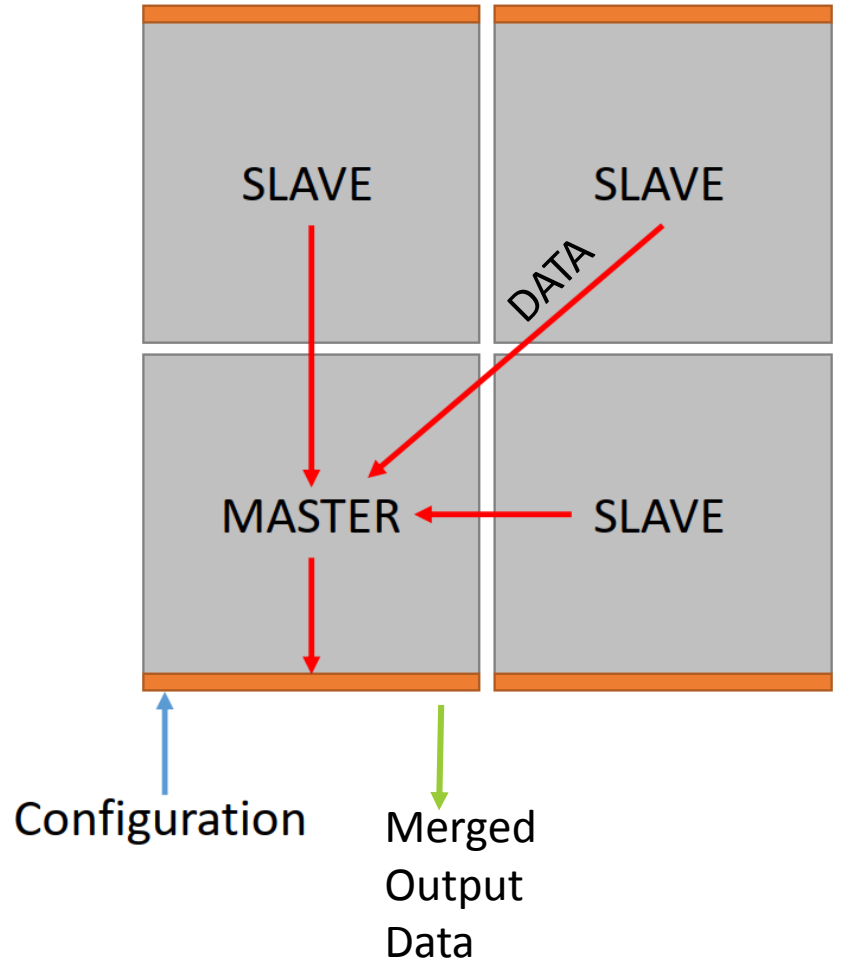
Increase of material budget for power and data cables

Data Transmission from Module

Several solutions to transmit data from a module to the readout

Master/Slaves configuration:

- Avoid large number of output connections
- Could simplify flex design
- Only one sensor transmits data over a long distance



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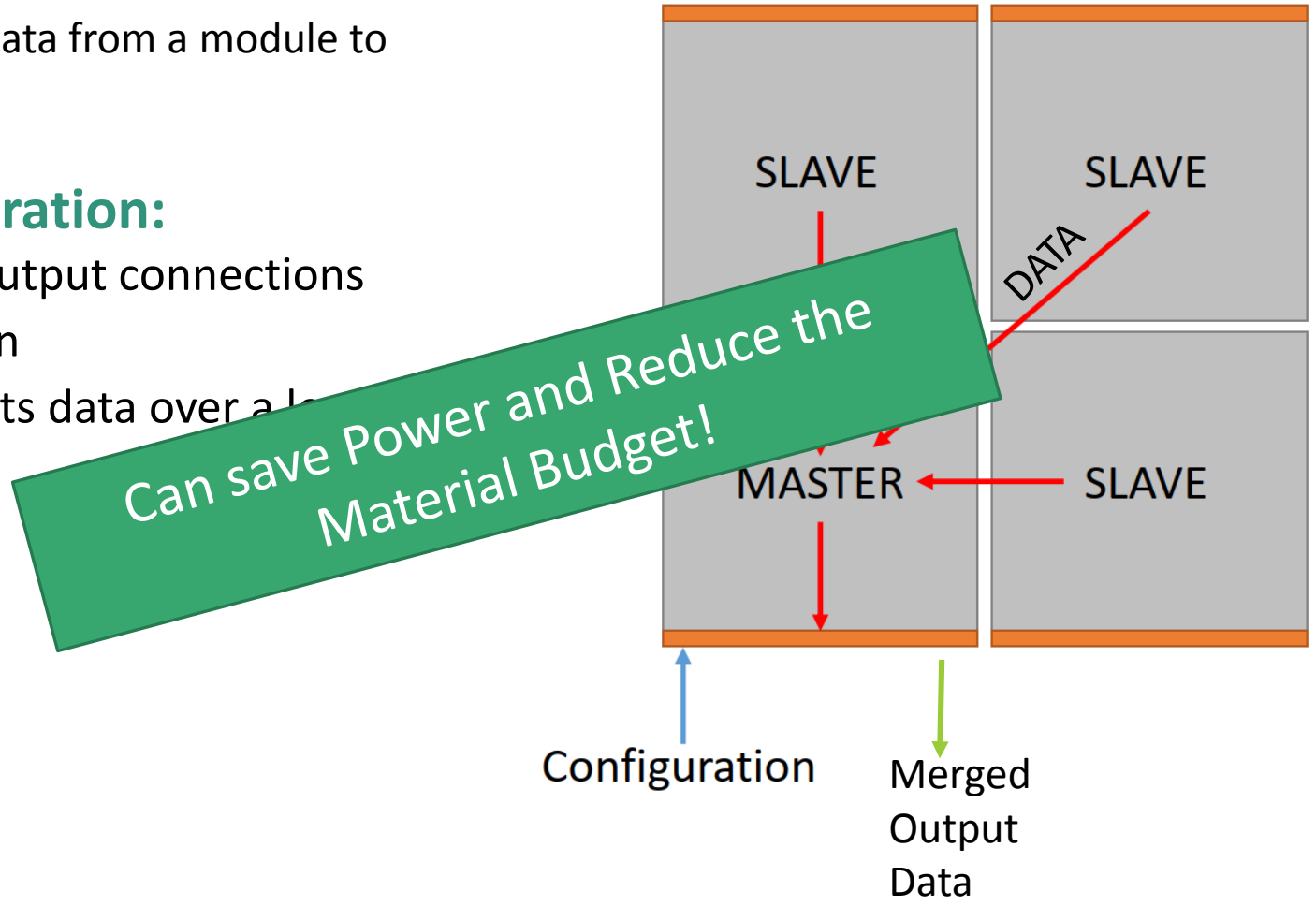
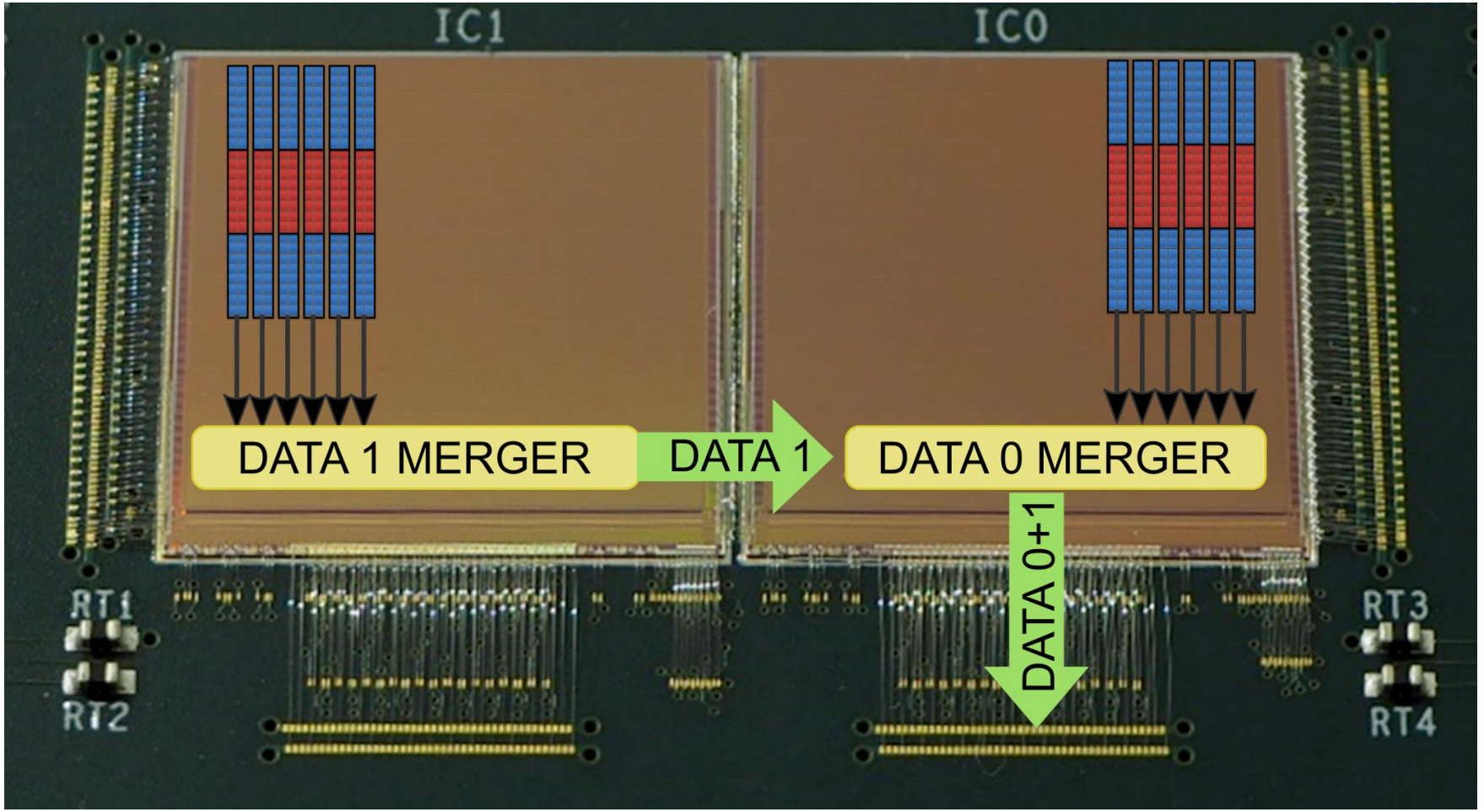


Can save Power and Reduce the Material Budget!

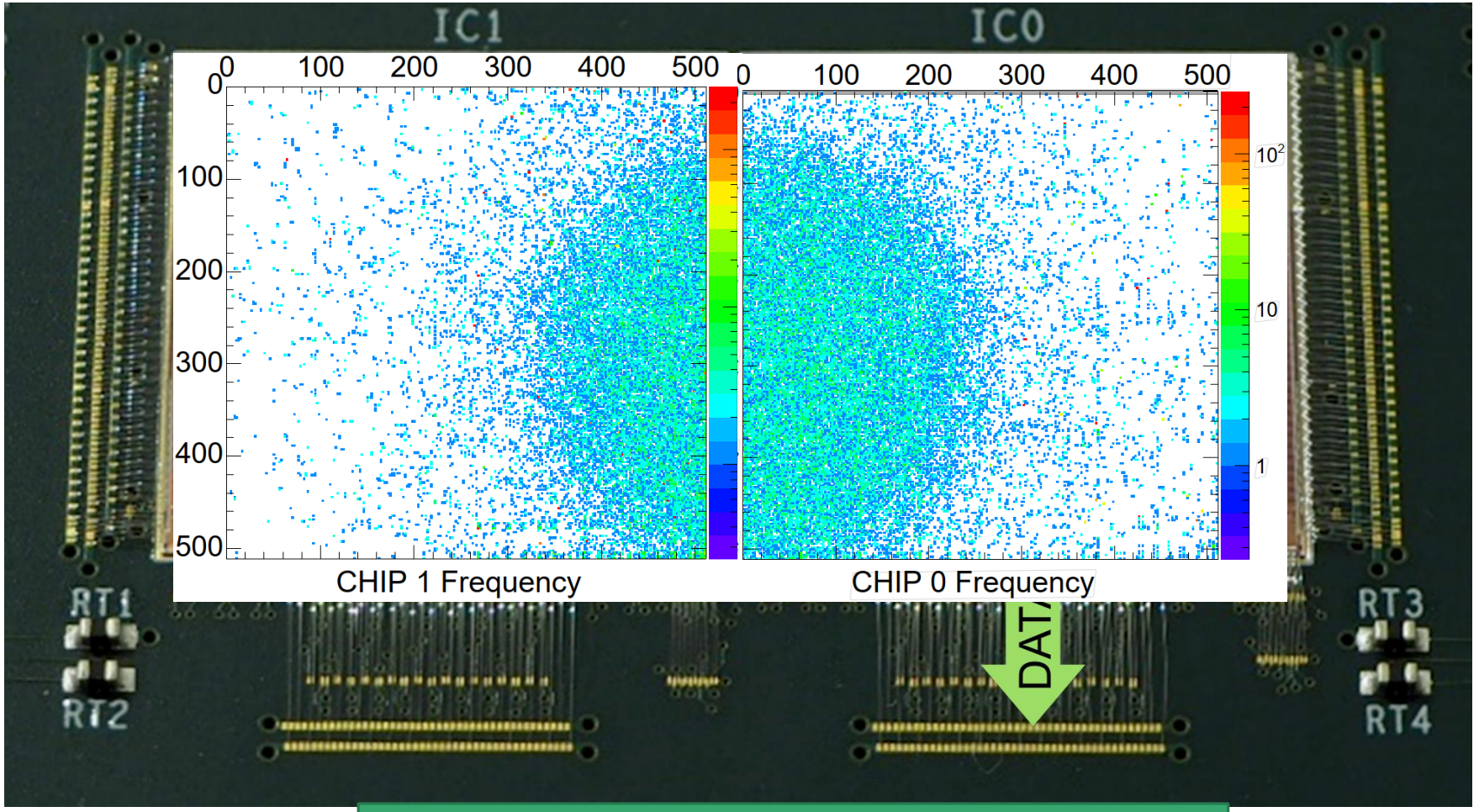
MALTA Chip2Chip data transmission



MALTA_C W7R22 MALTA_C W7R23

MALTA Chip to Chip Data Transmission

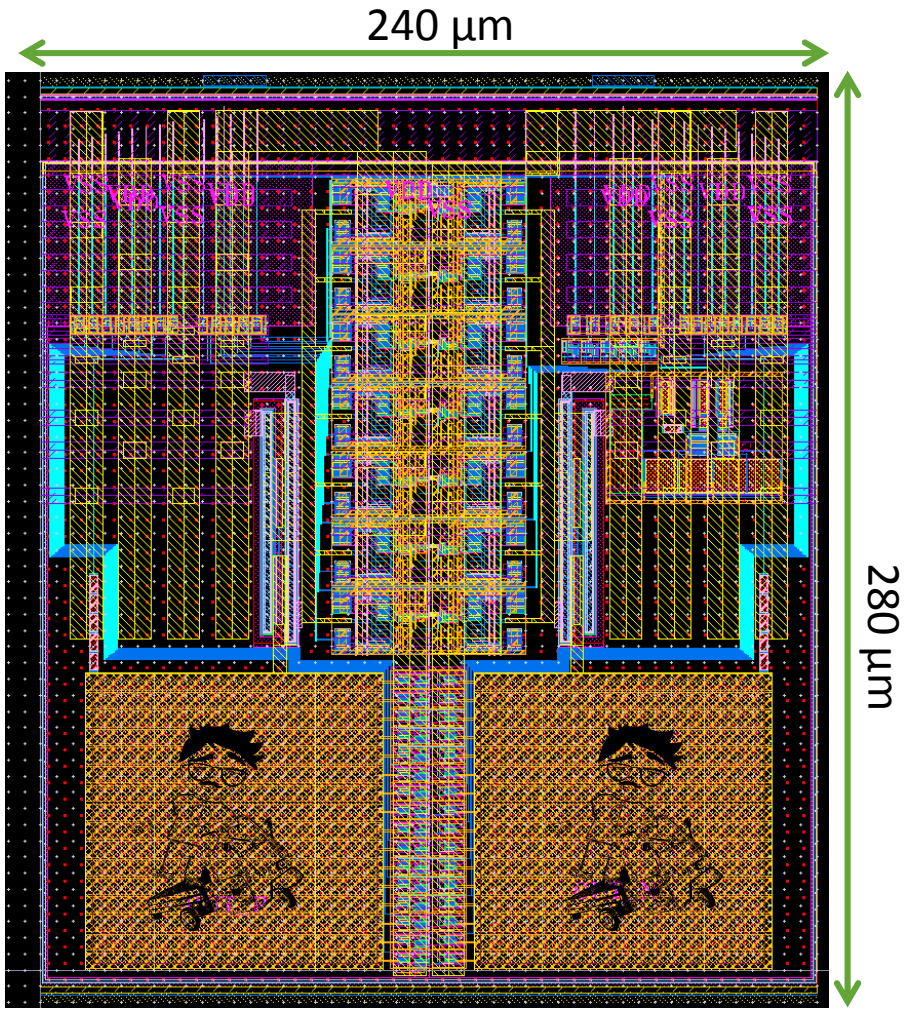
^{90}Sr source



MALTA

Compatible results in both directions

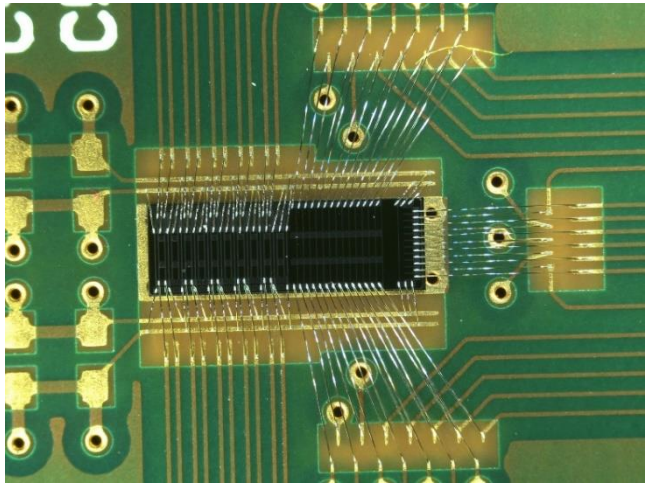
LAPA: pseudo-LVDS for the ATLAS Pixel Apparatus



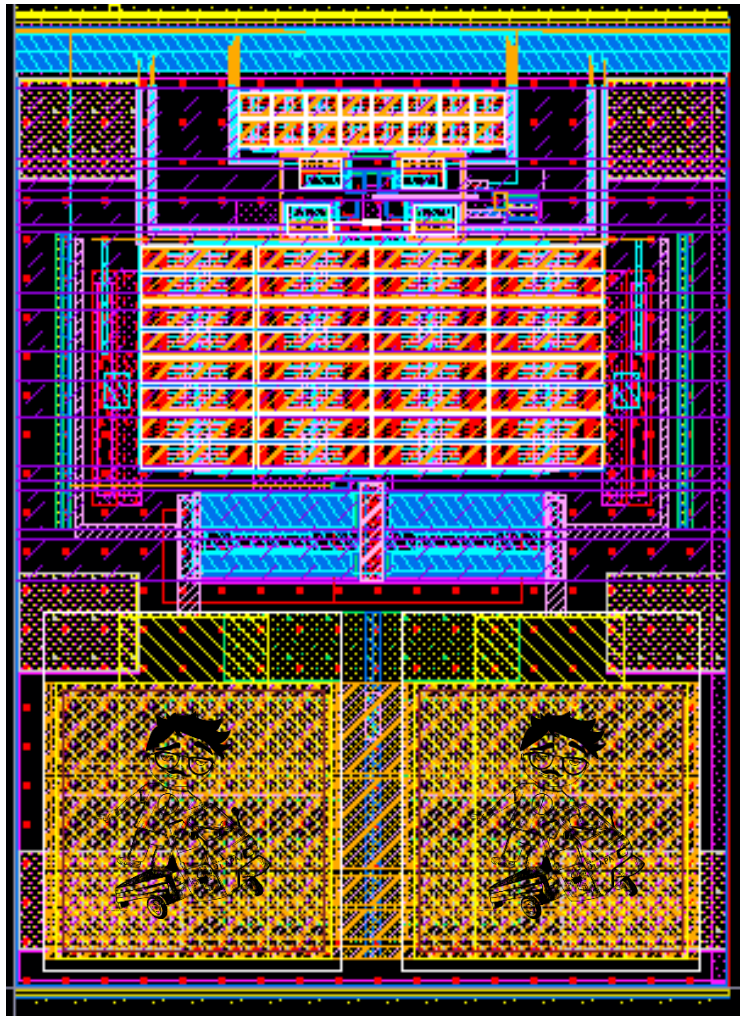
5Gb/s

- 280 X 240µm² (2 pad pixel pitch)
- Tunable DC current (7x 0.8mA)
- Modular capacitive coupled pre-emphasis: 16 blocks driving 25fF each.
- Vcm feedback control at 0.8V.
- Max power consumption: 30mW @ 5Gb/s
- 40 drivers integrated in MALTA (up to 2Gb/s)

Dedicated testchip



LAPA Receiver



5Gb/s

- 320 X 240 {2 pad pixel pitch) μm^2
- Internal selectable 100 Ω termination resistor

SPEC	Min	Max	Tested
VCM	0.7 V	1 V	0.75 V
Vdiff	0.3 V	-	0.4 V
Term Res	-	-	100 Ω
Bit rate	-	-	5 Gbit/s

Power	Current [mA]	Power [mW]	Input
Static	2.69	4.84 V	-
Dynamic	-	0.44	5 Gb/s
Total	-	5.28	5 Gb/s
Bias Static	0.94	1.7 V	-
RX+Bias	-	6.98	5 Gb/s

LAPA eye diagram measurement

5Gb/s

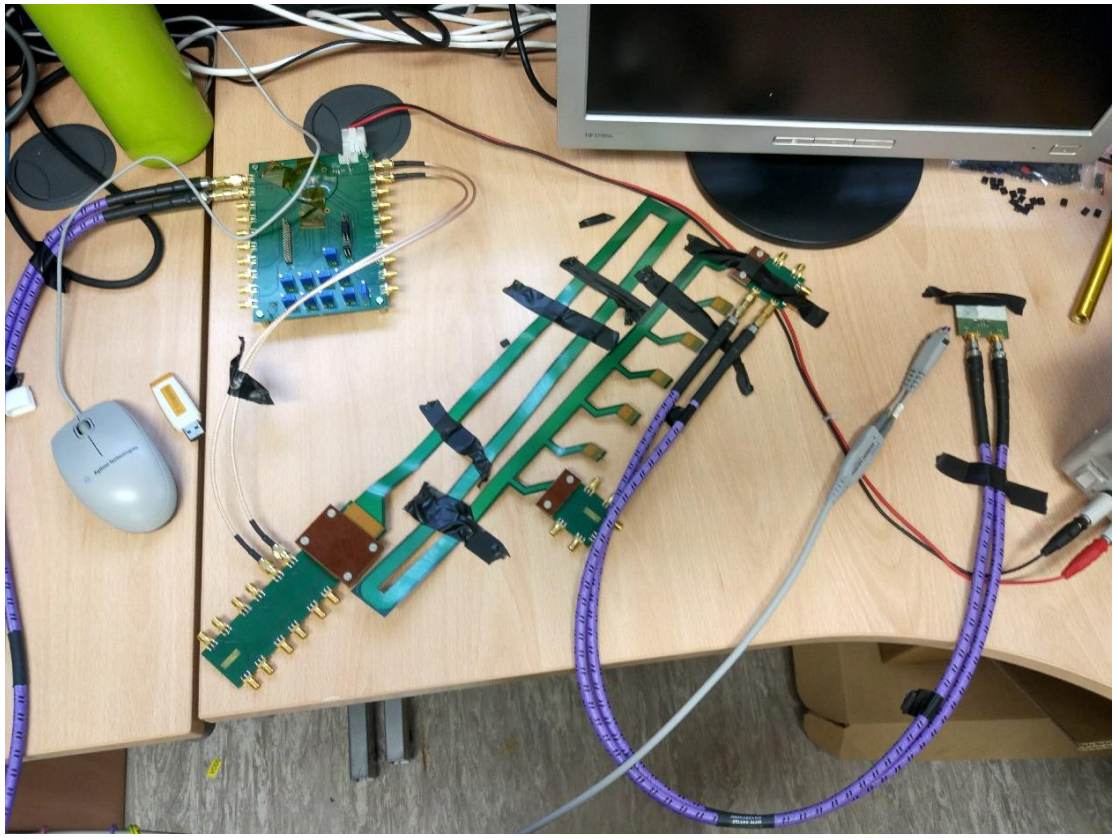
Jitter$_{p-p}$= 71ps

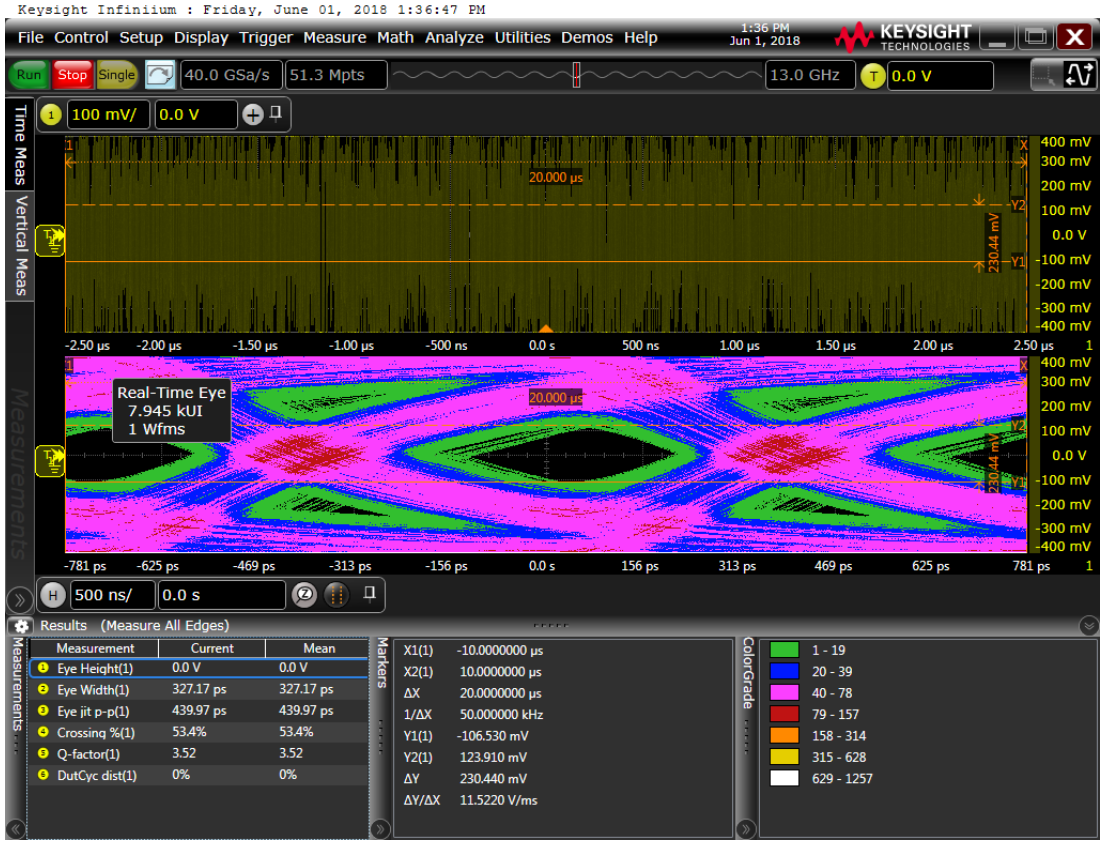
1.28Gb/s (ITk specification)

Jitter$_{p-p}$= 38ps

LAPA @1.28 Gbit/s on FLEX ITk prototype

Flex for data transmission out of the ITk system (length~5m)





Conclusions

The small collection electrode shows a collection efficiency >97% after neutron irradiation to $1 \times 10^{15} n_{eq} cm^{-2}$.

- The first version of the sensor (MALTA), suffers from degraded efficiency in the pixel corners after irradiation.
- Two process modifications have been developed using technology simulations, promising to improve the sensor radiation-hardness.
- The two new versions of the pixel have been implemented in the MiniMALTA sensor, which confirmed the results of the simulations, achieving the target radiation hardness, matching the ATLAS ITk outermost layer requirements. However, the collaboration has chosen to use Hybrid Pixel as baseline solution for the detector upgrade.

Several R&D towards the integration of CMOS pixel sensors have been carried on.

- A CMOS compatible microchannel fabrication process, has been successfully performed with the MALTA sensor. The sensor test demonstrate that the chip performance are not degraded after processing. The preliminary cooling tests demonstrate that this approach could be use in future applications.
- The data transmission in the tracker has been addressed with the development of a chip to chip communication schema and the design of a 5Gb\s low-power LVDS driver and receiver (LAPA). Both are promising to reduce power consumption, hence the overall material budget.
- Studies on a CMOS module have been performed, aiming to define the constrains for the future CMOS sensor design, and minimize the dead area.

My STREAM Experience

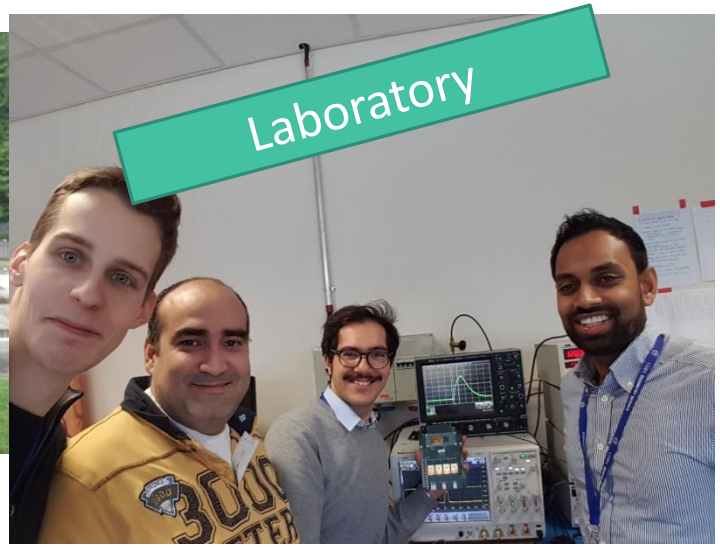
Guiding in ATLAS cavern

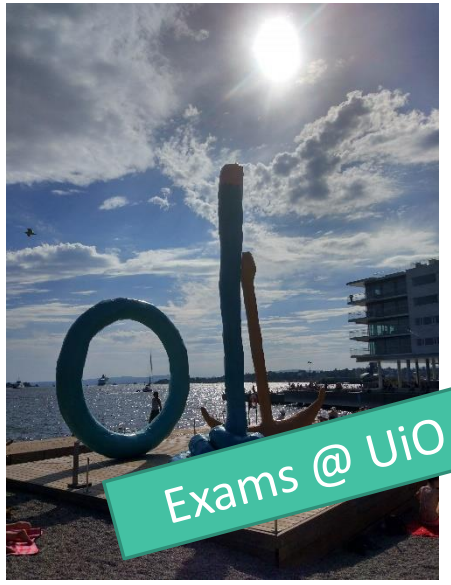
Testbeams

Conferences

Visits to Universities

Laboratory



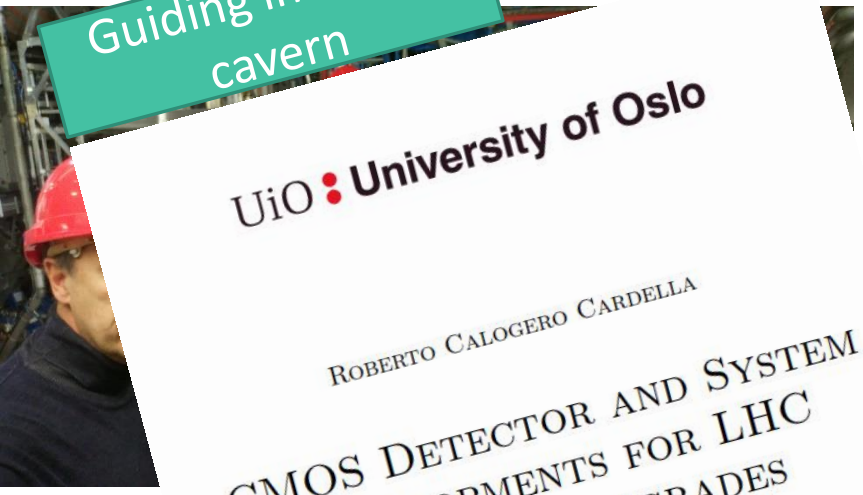


Exams @ UiO

Courses around Europe

My STREAM Experience

Guiding in ATLAS cavern



UiO : University of Oslo

ROBERTO CALOGERO CARDELLA

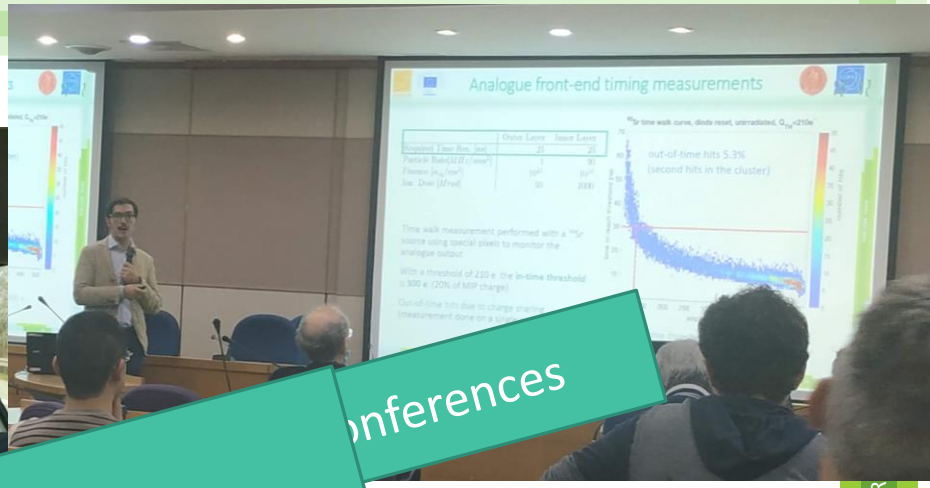
CMOS DETECTOR AND SYSTEM DEVELOPMENTS FOR LHC DETECTOR UPGRADES

Ph.D Thesis

Faculty of Mathematics and N
Department of Phy

AUGUST 2019

Testbeams



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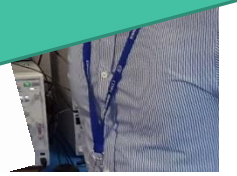
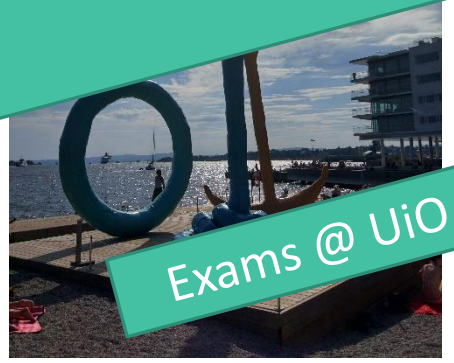
Thank you for the attention

Visits t
Universit





Exams @ UiO

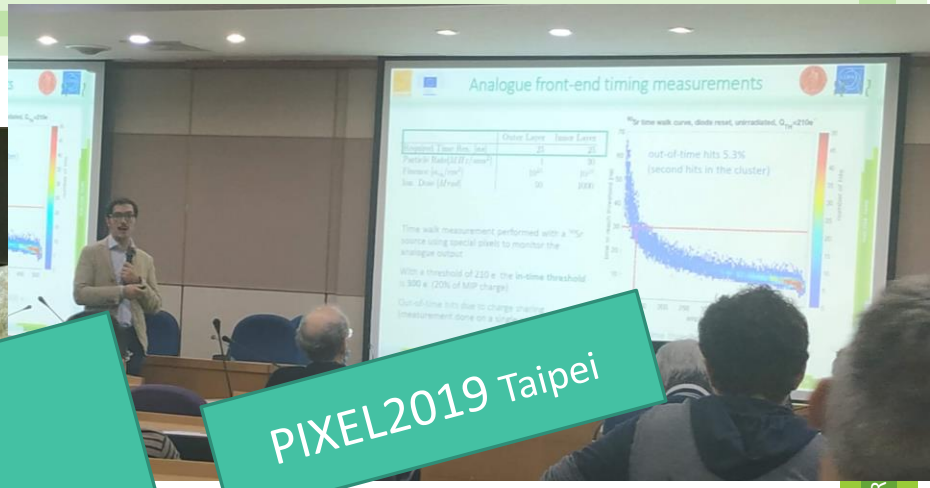
Courses around Europe

STREAM FINAL CONFER

My Year

Guiding in ATLAS cavern

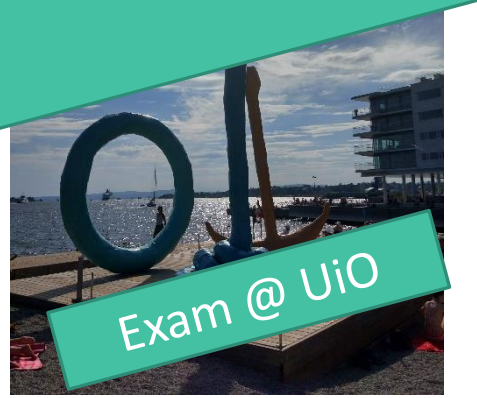
ELSA- TESTBEAM



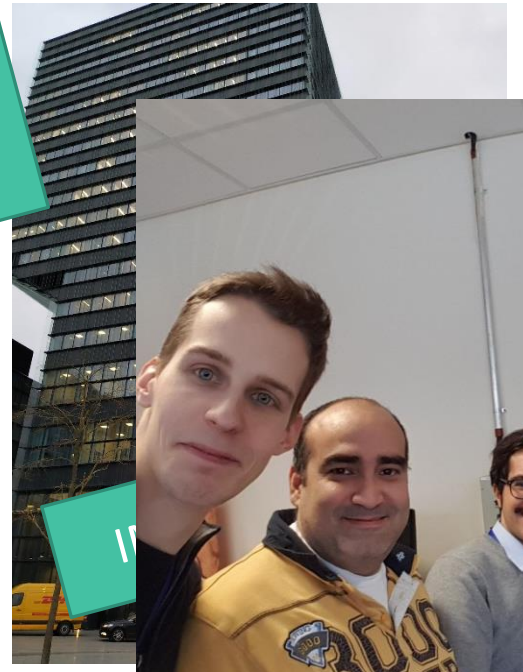
PIXEL2019 Taipei

Thank you for the attention

University of Glasgow

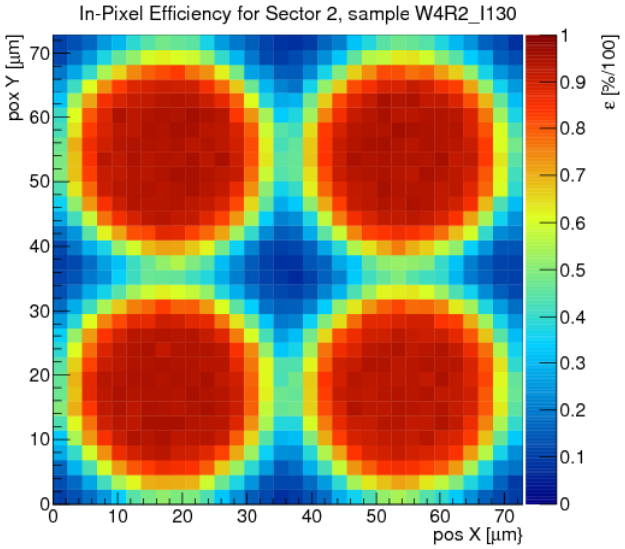


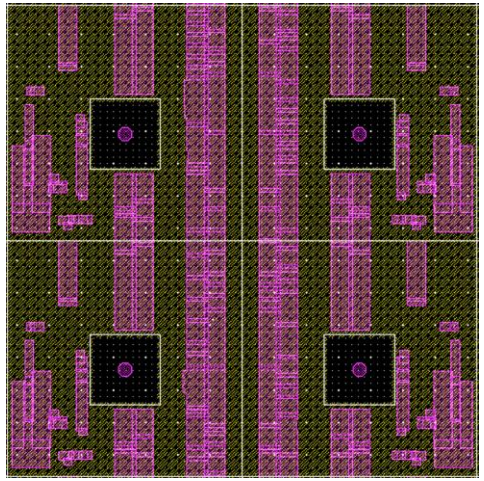
Exam @ UiO

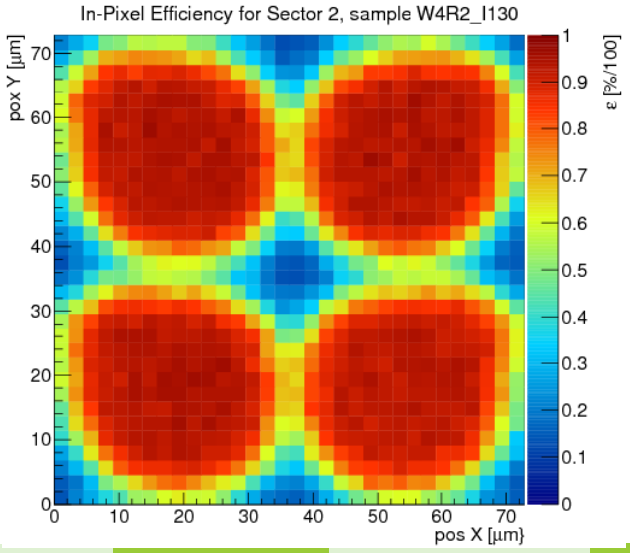


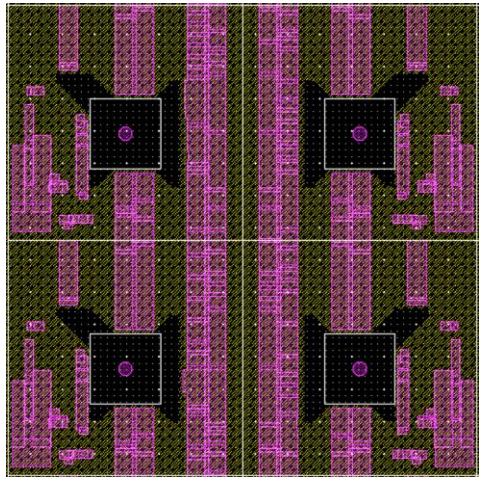
FINAL CONFER

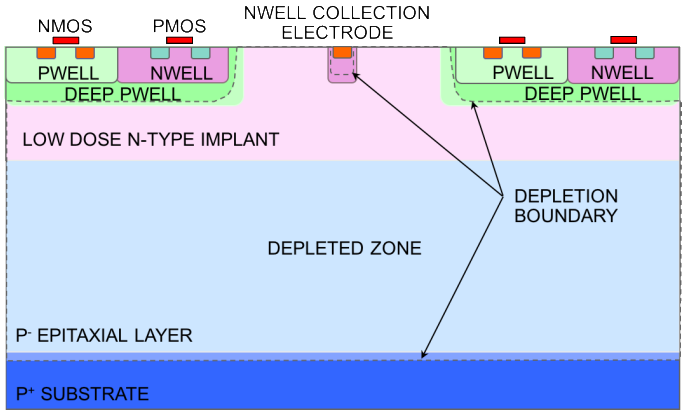
Efficiency vs. deep p-well coverage



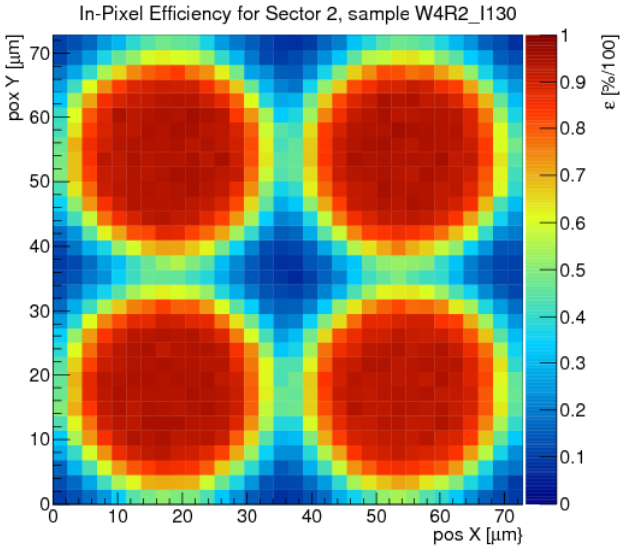


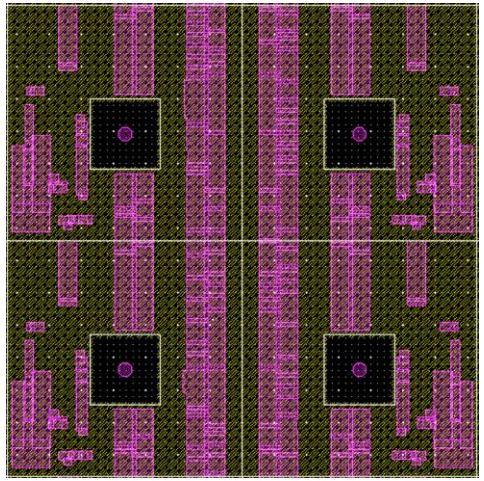


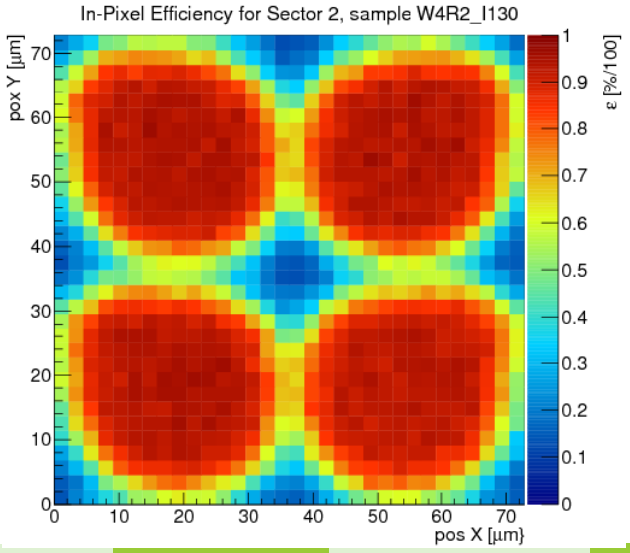


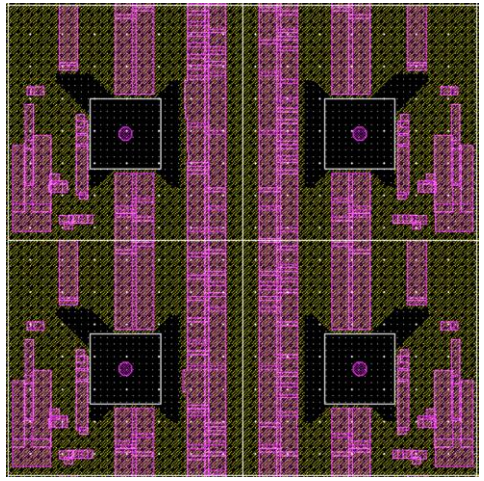


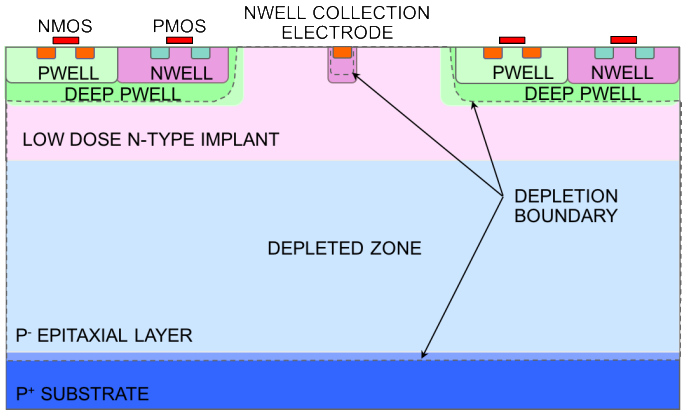
Efficiency vs. deep p-well coverage



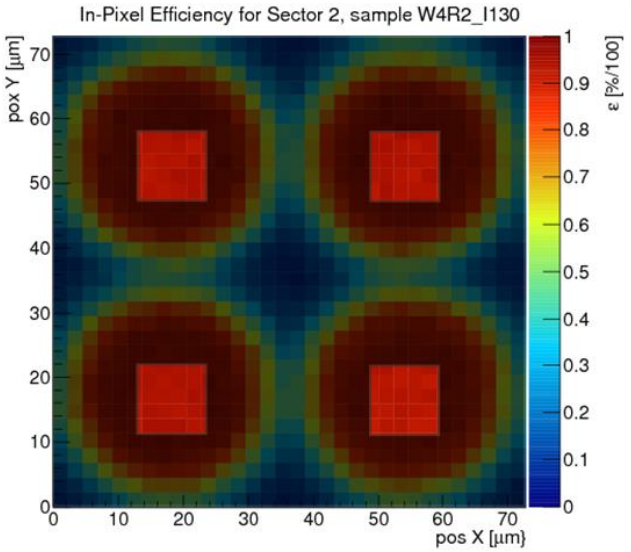


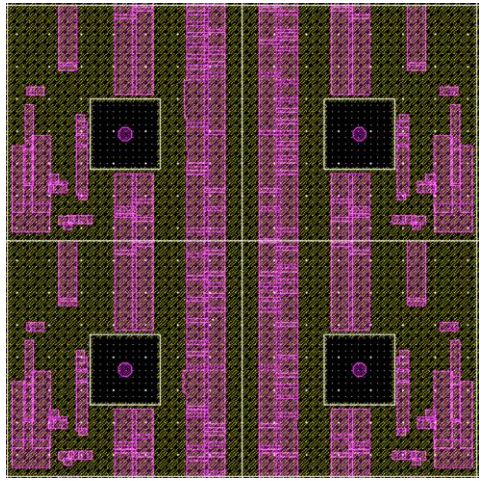


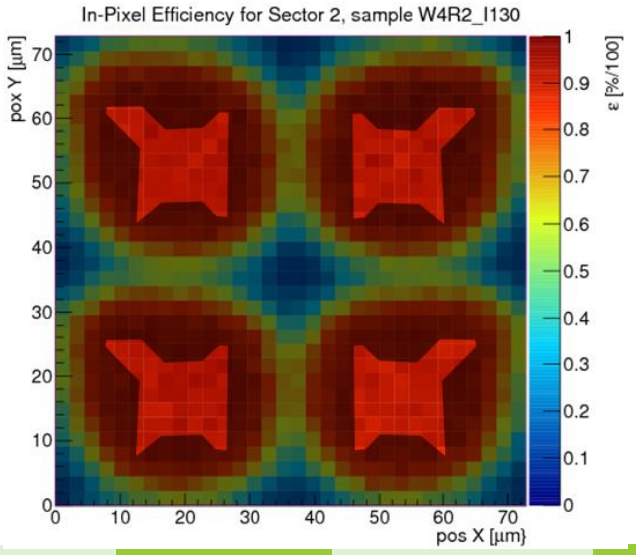


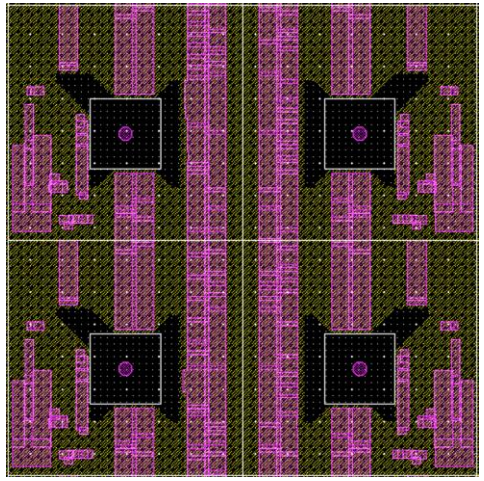


Efficiency vs. deep p-well coverage

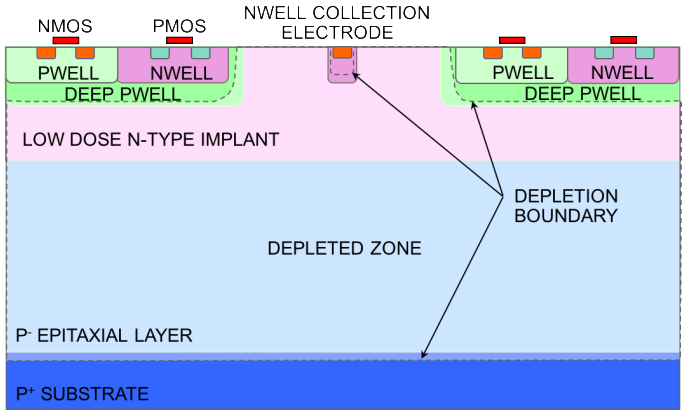




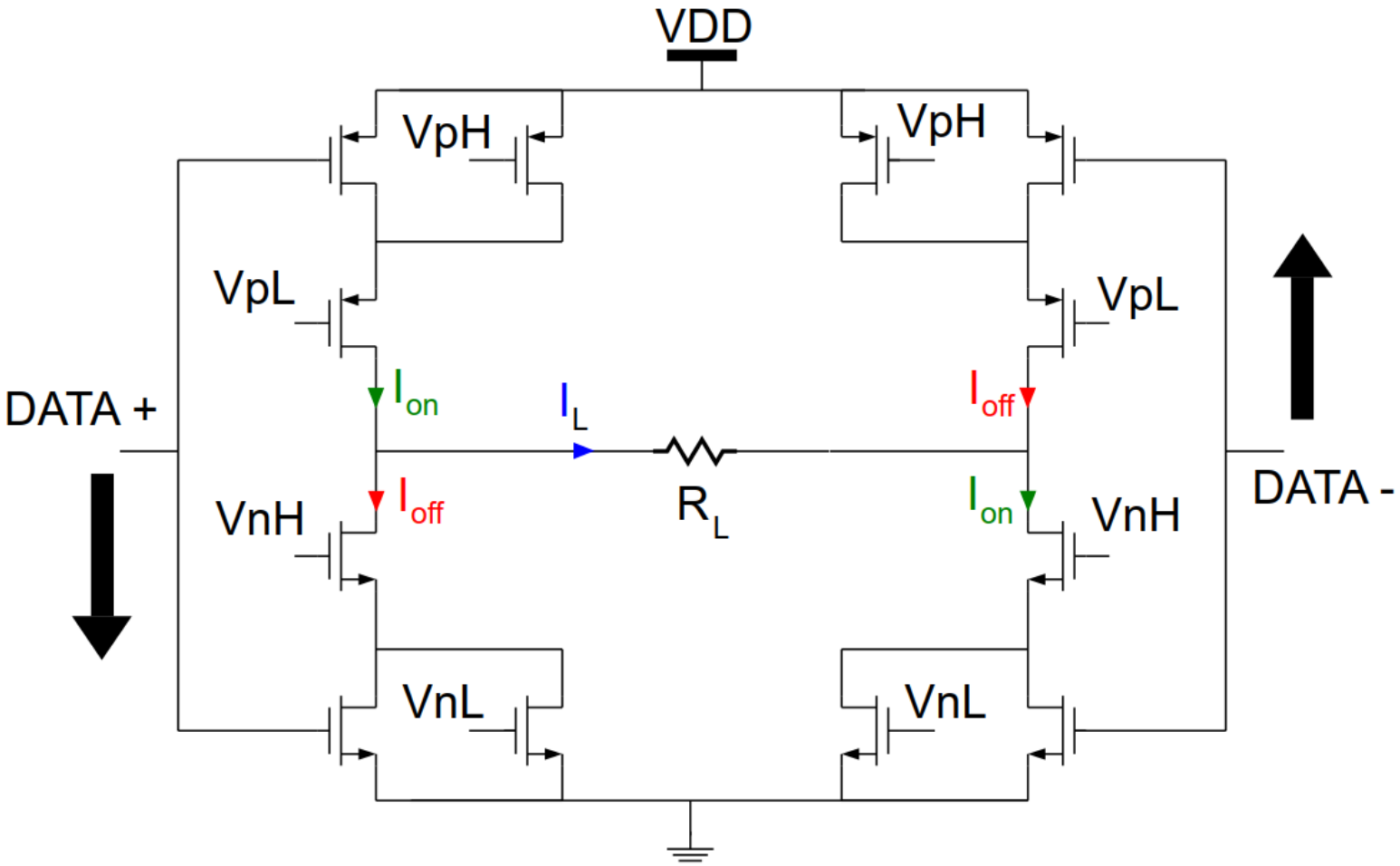




- Deep p-well only needed under n-wells of PMOS transistors
- In-pixel efficiency can be correlated to deep p-well coverage around the collection electrode
- Removed deep p-well results in higher overall efficiency due to higher lateral electric field

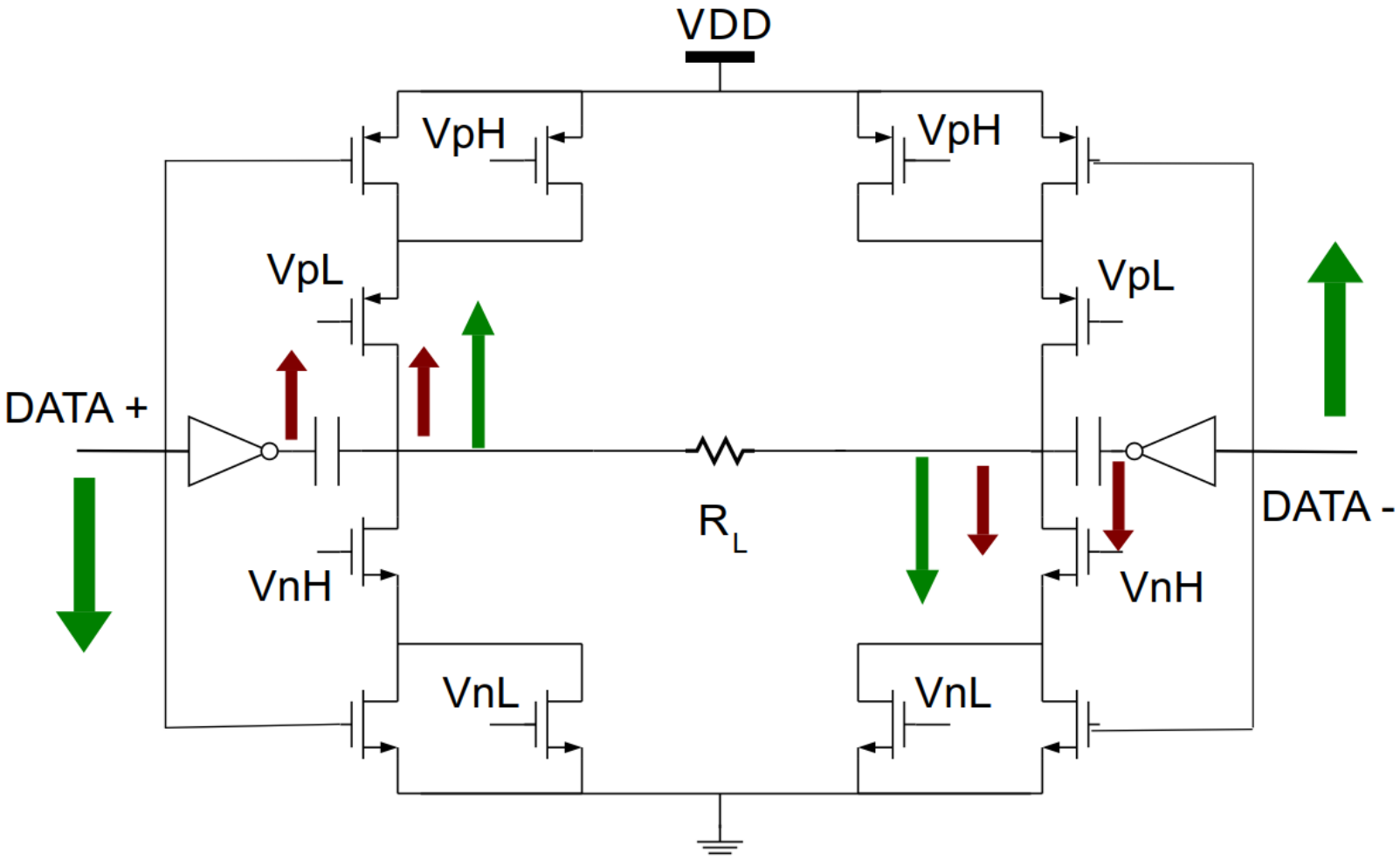


LAPA H-BRIDGE



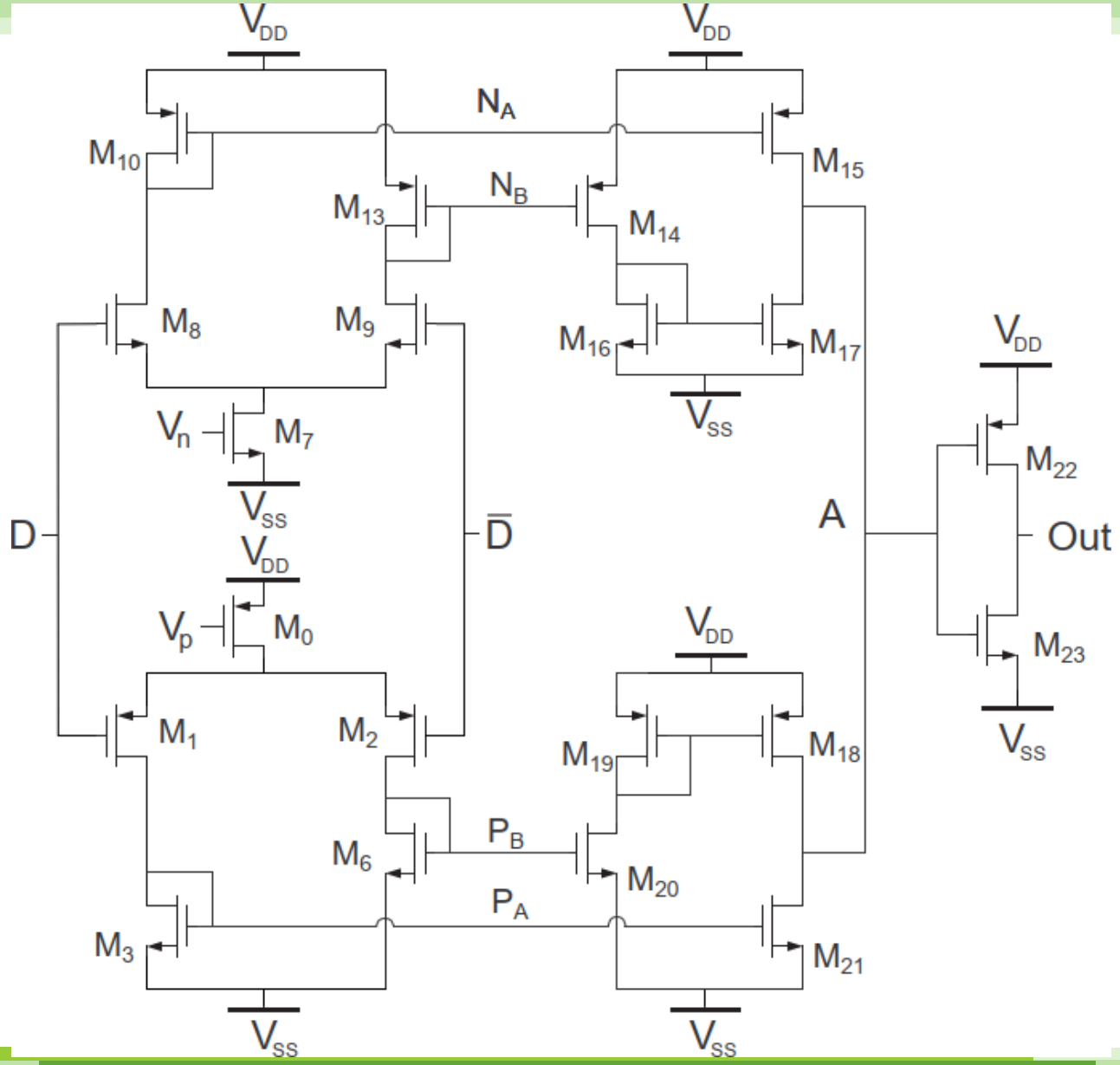
7 HBRIDGE blocks of 0.8mA - max: total 6mA

LAPA-PRE-EMPHASIS



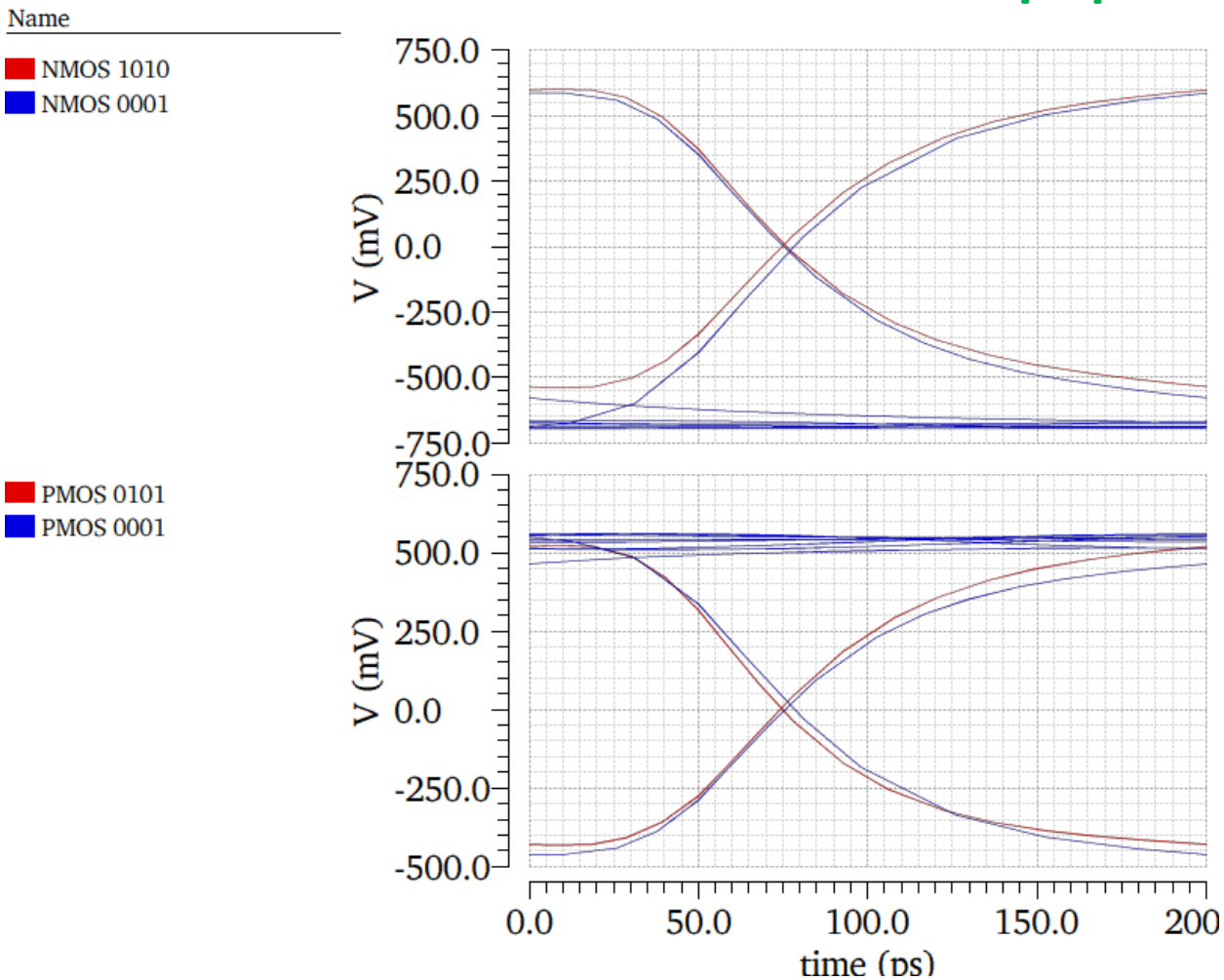
16 BLOCKS driving 25fF coupled with the output pad

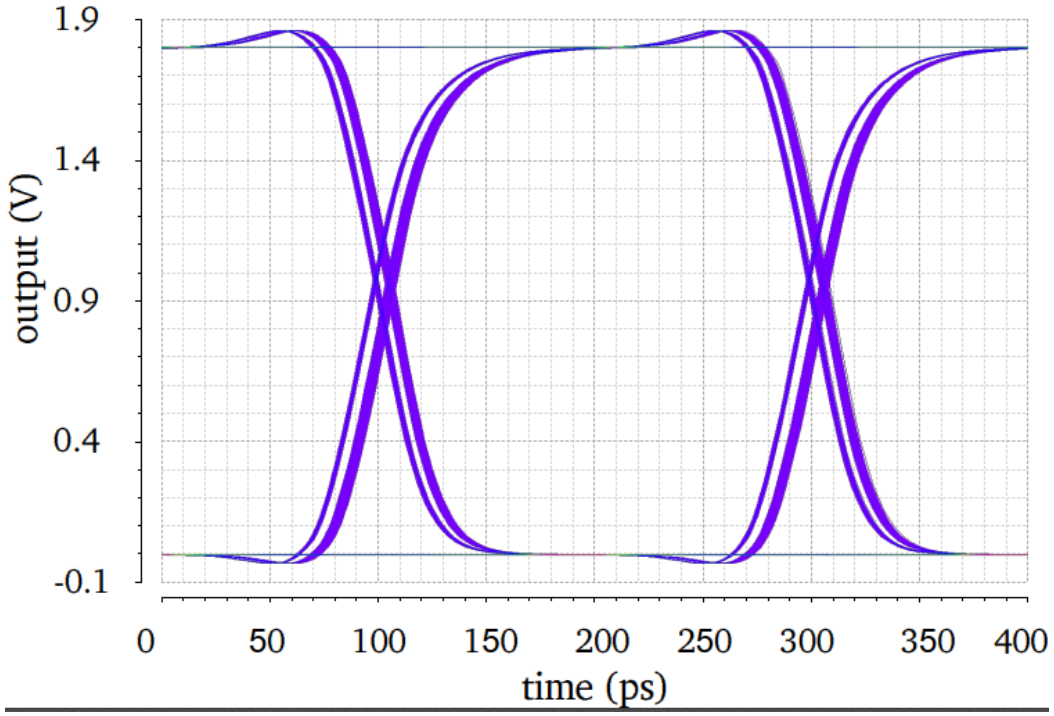
LAPA-RX


VDD
VDD
NA
M10
M15
NB
M13
M14
M8
M9
M16
M17
VDD
Vn
M7
VSS
VSS
D
D̄
A
VDD
M22
Out
Vp
M0
M23
VDD
VSS
M1
M2
M19
M18
PB
M6
M20
PA
M3
M21
VSS
VSS

LAPA Eye diagram simulation

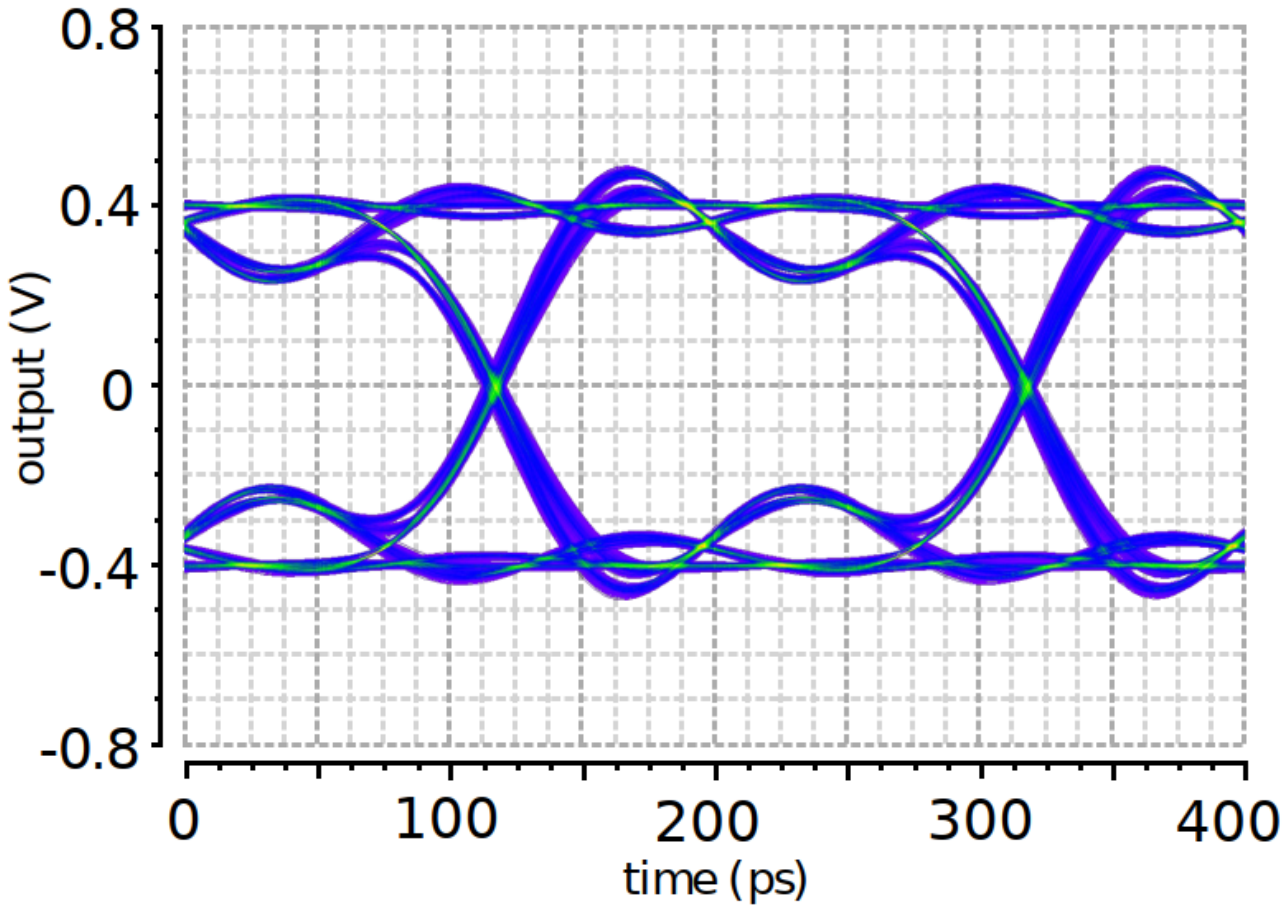
RX – 10 ps peak to peak jitter ISI ☹



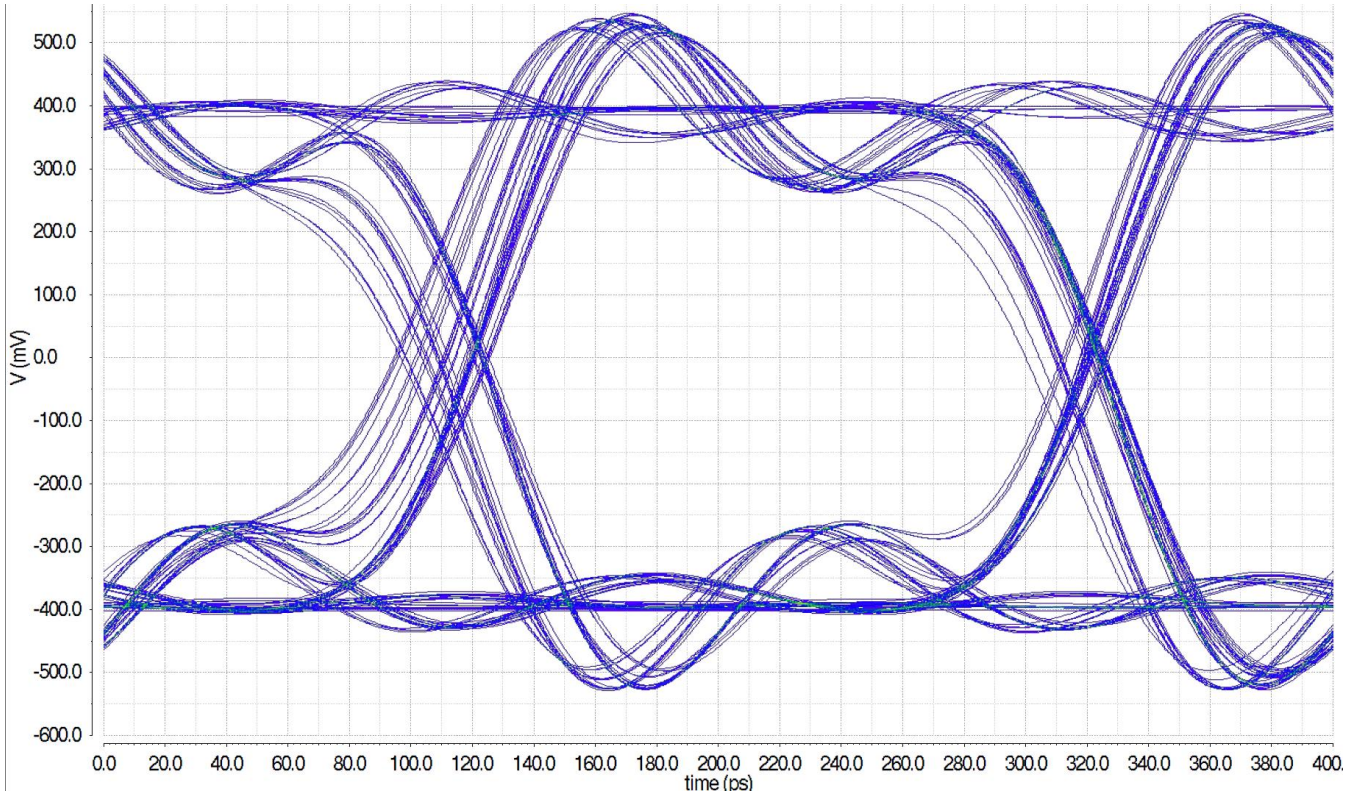


LAPA Eye diagram simulation

TX -15 ps peak to peak jitter



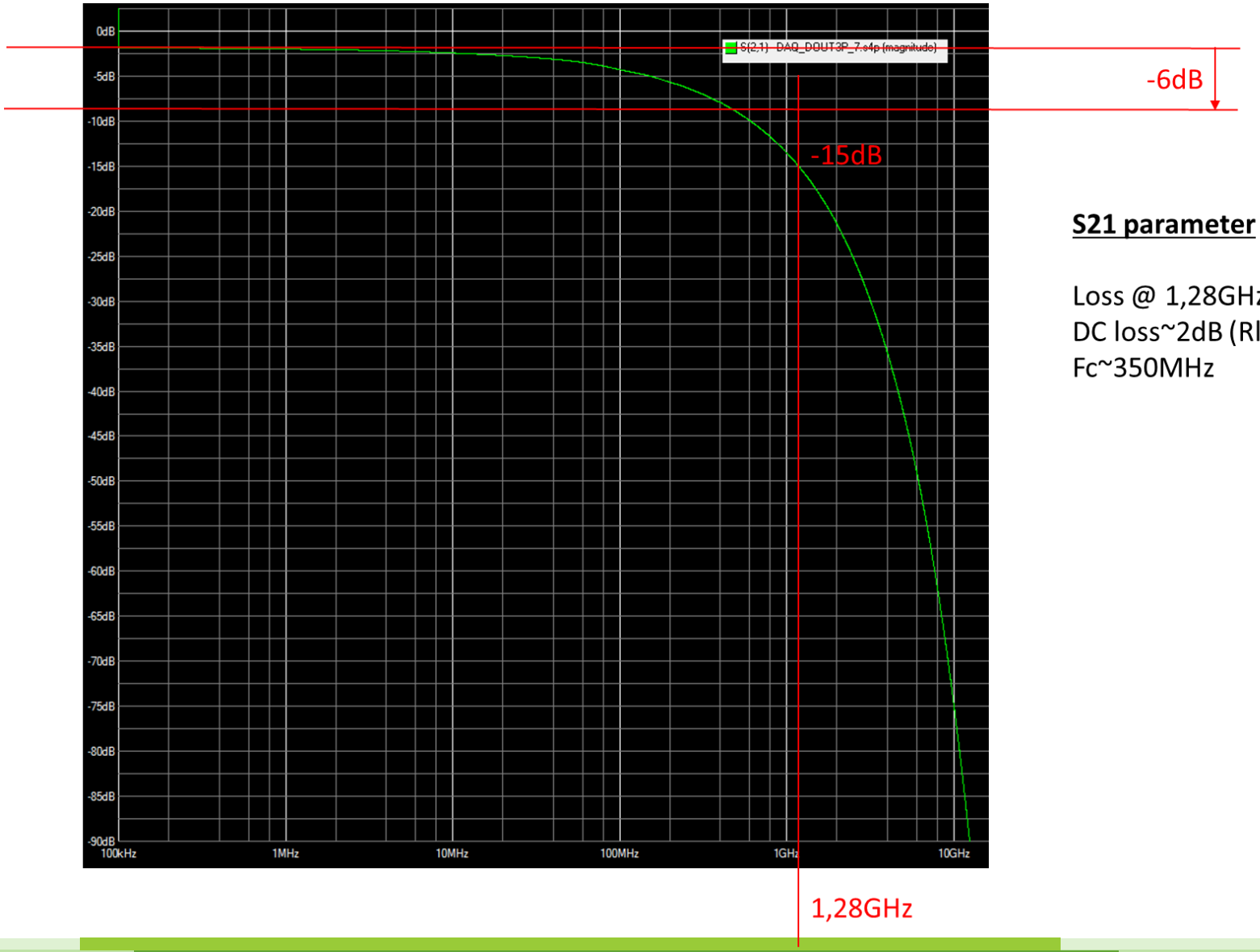
LAPA TESTCHIP SIMULATION



2.5GHz LVDS IN – LVDS OUT. 100Ω termination. 1pF load.

Simulated jitter=45ps

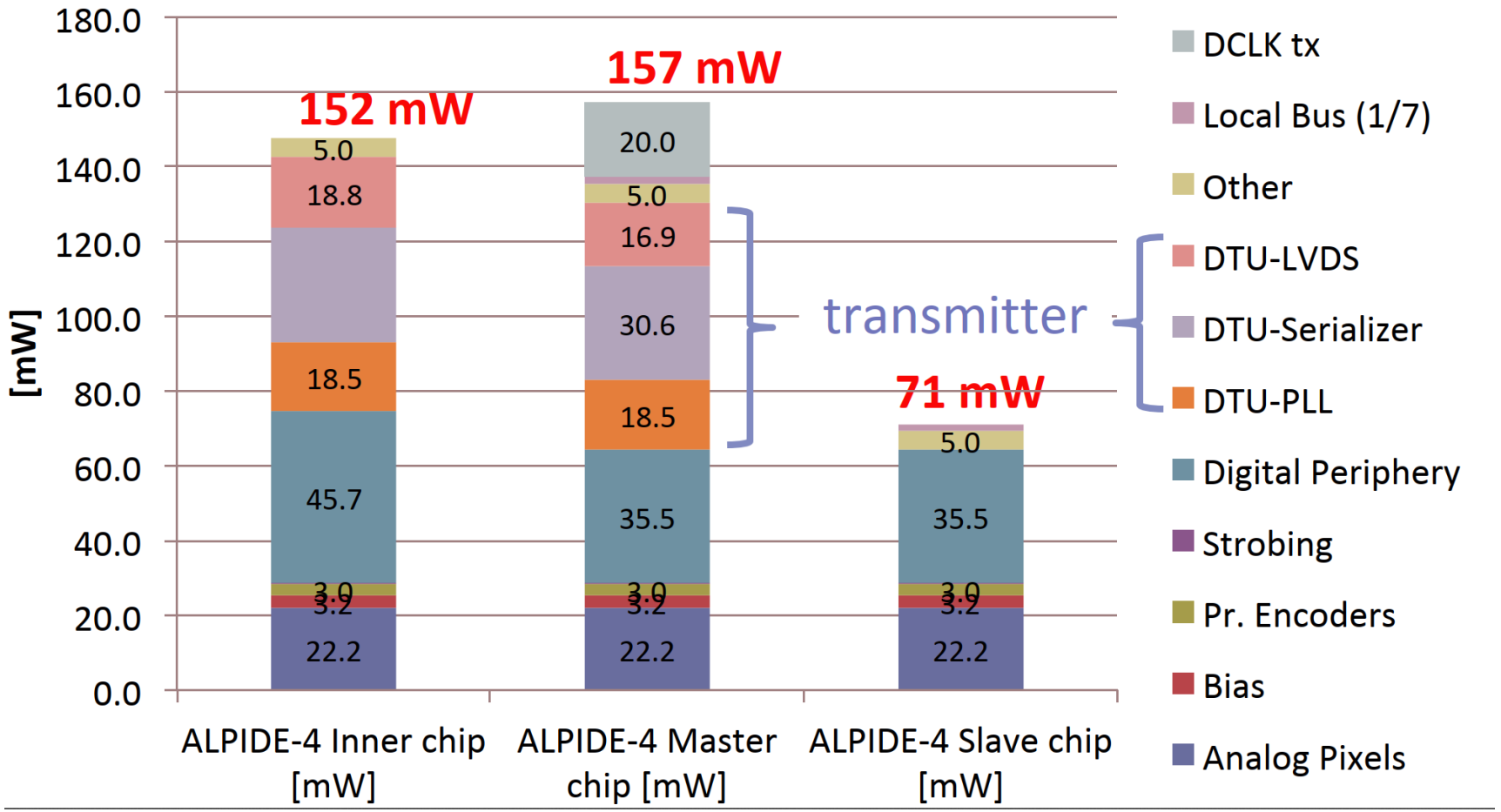
ATLAS ITk flex simulation



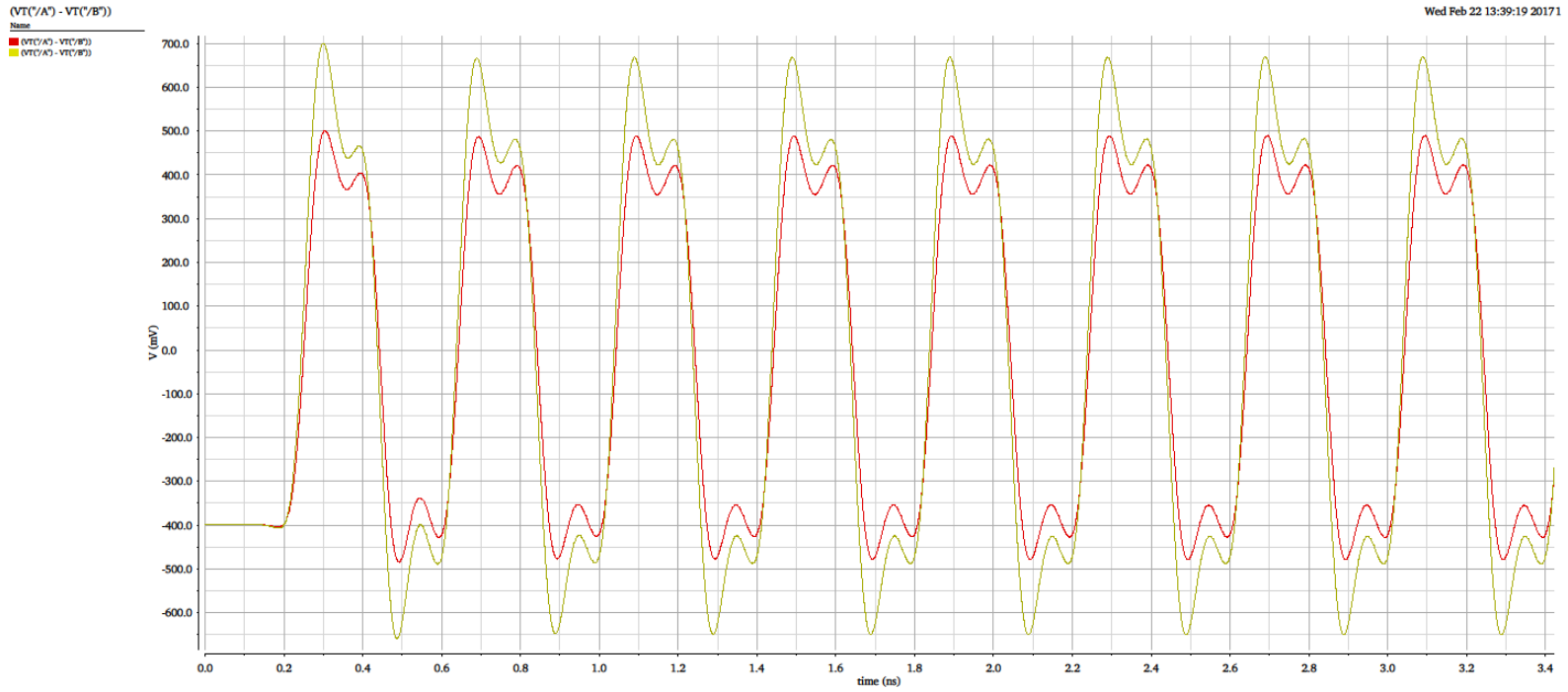
S21 parameter

Loss @ 1,28GHz~15dB
DC loss~2dB (Rlin~20ohms)
Fc~350MHz

ALPIDE Power Consumption



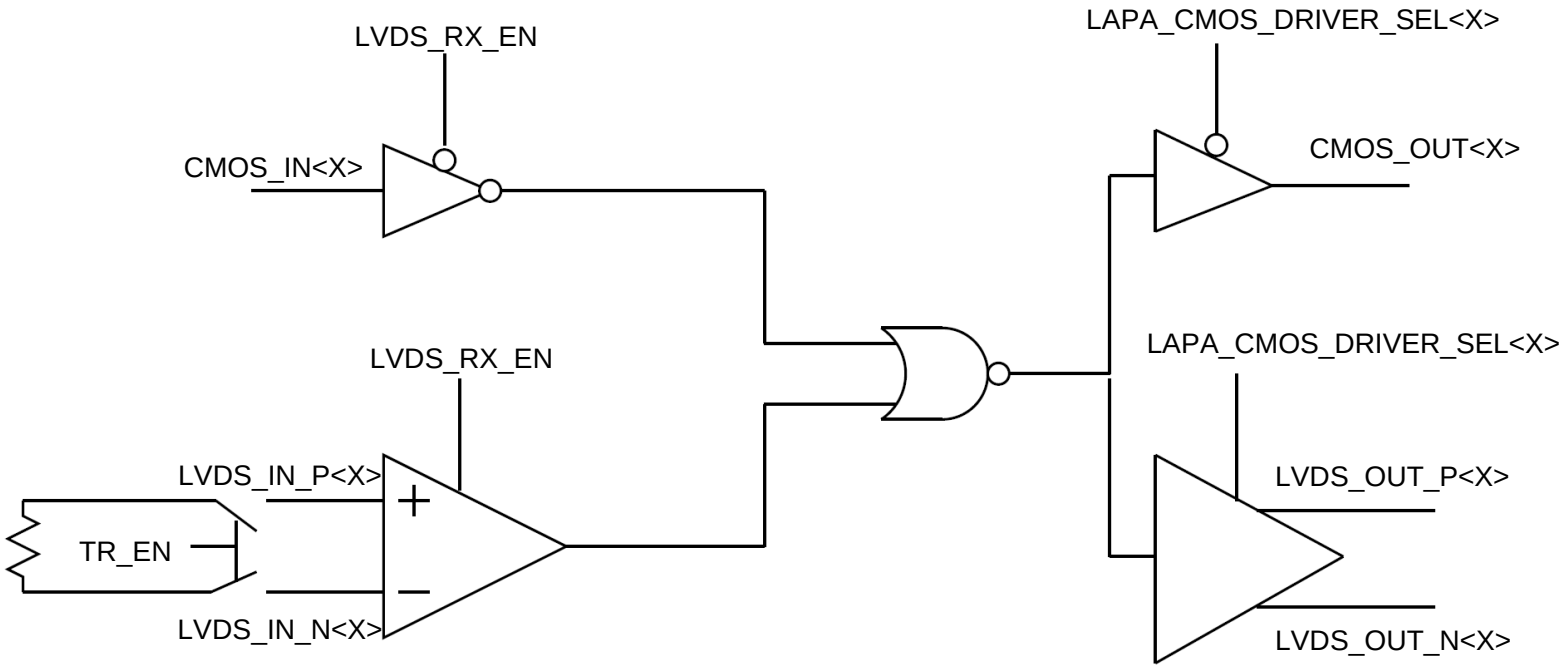
Pre Emphasis Simulations



PRE ♯	PwSH $[mW]$	PwDig $[mW]$	PwToT $[mW]$
8	7.2	18.6	26.8
16(max)	7.2	25.4	33.6

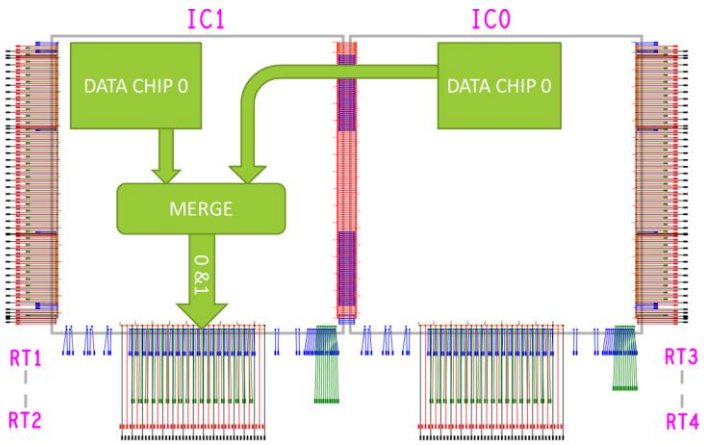
Simulations of the LVDS OUTPUT

LAPA Single Channel Schema



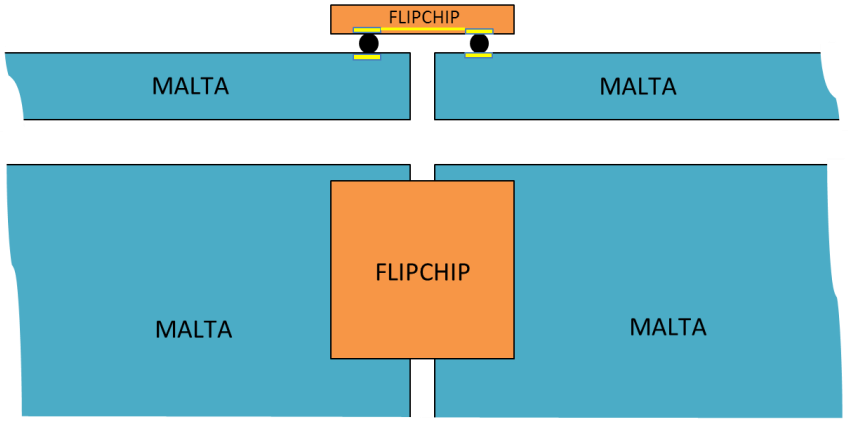
Chip 2 Chip Communication

Wirebond connection



MALTA can transmit power and data asynchronously to a neighboring chip (via CMOS pad), merging the data of multiple pixel matrix in just one parallel output

Flip chip connection



Connection between neighboring chips using flip chip

- Better for assembling
- Allow additional electronics in the flipchip