12th LHC electronics workshop

- Valencia, Spain
  - 24-29 September 2006
  - Organisers
    - Instituto de Fisica Corpuscular (IFIC)
    - Consejo Superior de Investigaciones Científicas (CSIC)
    - Universidad de València
  - Chair of local organisers
    - Juan Valls (Valencia)

Previous LHC Electronics workshops

1995	Lisbon	Portugal
1996	Balaton	Hungary
1997	London	UK
1998	Rome	Italy
1999	Snowmass	USA
2000	Cracow	Poland
2001	Stockholm	Sweden
2002	Colmar	France
2003	Amsterdam	Holland
2004	Boston	USA
2005	Heidelberg	Germany
2006	Valencia	Spain

Heidelberg 2005

- 12-16 September 2005
  - Ruprechts-Karls-Universität Heidelberg:
  - Kirchhoff Institute for Physics Physics Institute.
  - Max-Planck Institute for Nuclear Physics

- Local Organisers
  - Ulrich Uwer, Chair
  - K. Meier
  - M. Schmelling
  - K. Sparenberg
  - U. Trunk

LECC history

- Following DRDC era, an LHCC sub-committee reported on electronics
  - LHC Electronics (Review) Board, later revised to LEB
- 2001: Director of Research for Collider Physics and Management of the Experimental Physics Division set up the LHC Electronics Coordinating Committee
  - Present chairperson: Lucie Linssen
- Original mandate
    - Minutes May 2001 http://ep-mgt-lecc.web.cern.ch/ep-mgt-lecc/LECC_Minutes/Minutes_1.htm
  - Identify and implement common solutions for the electronics of the LHC experiments wherever possible.
  - Review and recommend support for the LHC experiments.
  - Facilitate the design, fabrication, testing, commissioning and maintenance of electronics for the LHC experiments.
  - Organize an annual LHC Electronics Workshop
- However, less clear mechanism for reports and actions than LEB

Conference organisation 2006

Local Organisation

Juan A. Valls, Chair

Emilio Higón

Antonio Ferrer

Belén Salvachúa

Esteban Fullana

Proceedings

Sandra Claude, CERN

Scientific Organisation

J. Christiansen, CERN

K. Einsweiler, LBL

P. Farthouat, CERN

F. Formenti, CERN

G. Hall, Imperial College

M. Letheren, CERN

L. Linssen, CERN

A. Marchioro, CERN

J. Nash, CERN

C. Parkman, CERN

E. Petrolo, INFN, Rome

S. Quinton, RAL

V. Radeka, BNL

W. Smith, Wisconsin

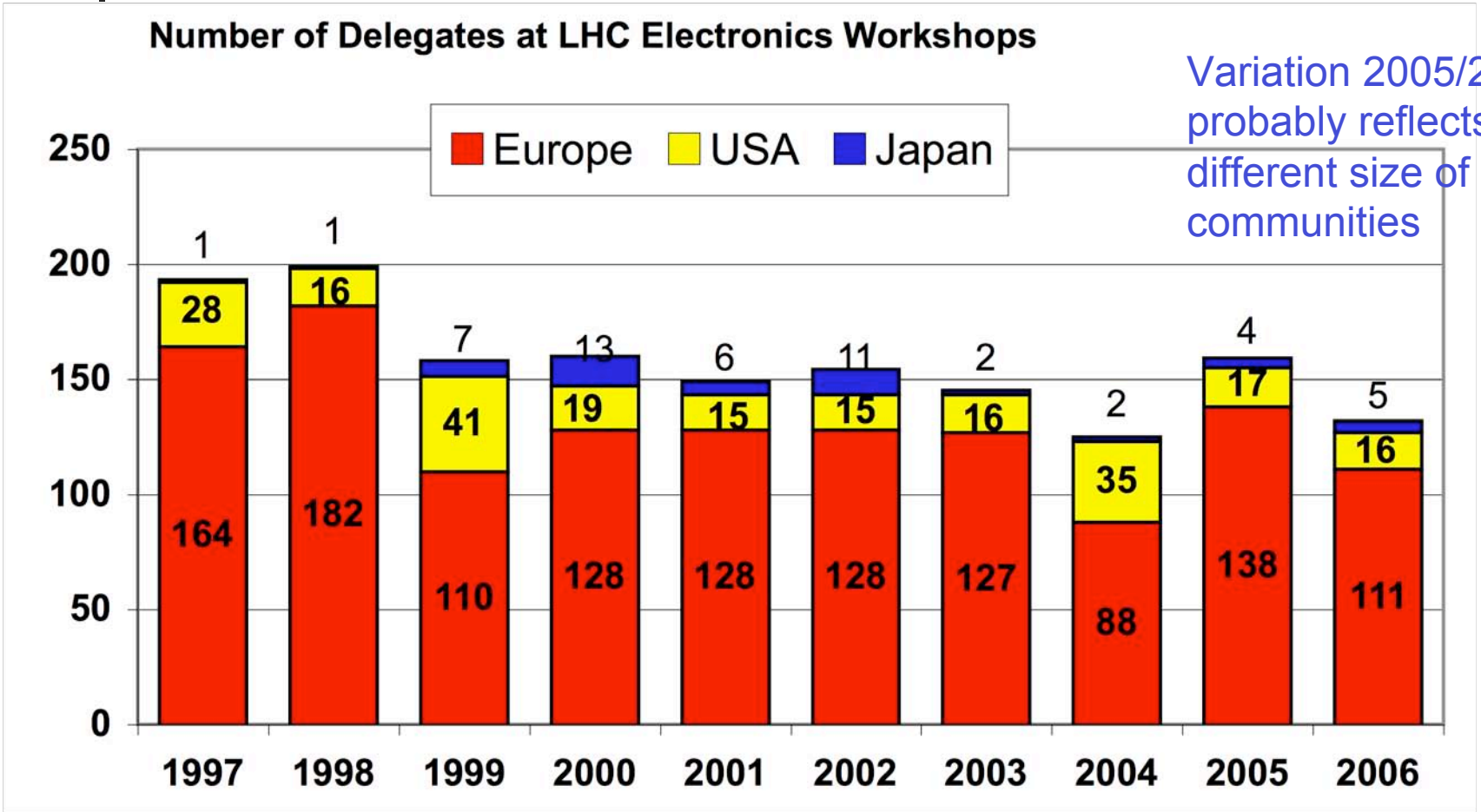
F. Vasey, CERN

T. Wijnands, CERN

R. Yarema, FNAL

- Scientific organisation by LECC and additional members
  - Several have contributed for many years

Participation



Variation 2005/2006 probably reflects different size of local communities

Finances

- As usual the Workshop was self-financing

- We are very grateful for support from
  - The local institutes
  - CERN - especially proceedings and poster
  - Industrial exhibitors
    - Wiener Plein and Baus Ltd

Presentations and Proceedings

- Statistics
  - 11 invited plenary talks [2004: 10]
  - 62 parallel session talks [2004: 60]
  - dedicated meetings of microelectronics user group and optoelectronic working group within the conference
  - 44 posters [2004: 21]
  - Proceedings: will be printed (soon) as usual : CERN 2006-***
    and will go to the web with previous proceedings
  - http://lhc-electronics-workshop.web.cern.ch/LHC-electronics-workshop/default.htm
- Presentations also available
  - http://indico.cern.ch/conferenceTimeTable.py?confId=574
  - Indico has been a very valuable tool for organising the workshop
    - abstracts, paper selection, agenda, handling talks, archiving,…

Plenary talks 2006

- Antonio Ferrer — *Particle and Astroparticle Physics in Spain*
- Mike Lamont — *LHC machine, calibration…commissioning*
- Ernesto Perea — *CMOS directions in industry*
- Vyshi Suntharalingam — *3D electronics*
- Tim Greenshaw — *Detector and Readout Systems for ILC*
- Ray Larsen — *High Availability Electronics standards*
- Marco Van Uffelen — *Optoelectronics for remote-handled maintenance tasks in ITER*
- Rui De Oliveira — *State of the art technologies for front-end hybrids*
- Ray Yarema — *3D Circuit Integration for High Energy Physics*
- Franco Maloberti — *Technology Scaling and CMOS Analog Design*
- Andy Butterworth — *LHC machine RF issues and developments*

Rigid-flex substrates (Hybrids)

- NB this type of conference allows to follow/investigate topical issues
  - Several projects had problems in this area
  - But also some notable successes
- Plenary talk from Rui de Oliveira (CERN) in 2006
  - User requirements and available technologies constantly evolving
  - Followed dedicated one-day session in 2005
    - Industrial and user views of issues and lessons learned
- Common themes emerged clearly
  - Relatively easy to agree on “best practice”
  - Less easy to know how best to implement or enforce it
  - Written summary of session produced
    - May be helpful to others

Hybrids 2005 - issues

- Quality Assurance
  - QA culture and risk assessment vital
  - Budget for it, including time
  - Avoid excessive specs & be prepared to review real needs
- Partnerships with industry
  - Number of specialist companies is small
  - Need to work closely with them
  - Observe design rules and industrial prior experience
- Contracts and tendering
  - Is preparation adequate?
  - Lowest cost tendering adds risk, so qualify vendors
  - Late changes add cost, so users need to be open about all requirements

CMOS electronics

- Not a new subject - but remains very relevant
  - Trends — Ernesto Perea (STM)
  - Challenges of design — Franco Maloberti (U. Pavia)
  - Managing access — Sandro Marchioro (CERN) & MUG
- Messages
  - Manufacturer investments enormous ($2-3B)
    - Trend for global collaboration will continue
  - CMOS scaling paradigm is breaking down
  - Moore's law requires constant power density- not just size reduction
  - Reducing power while increasing performance still challenging
  - Digital compensation techniques for analogue imperfections
  - HEP community has gained much experience but will require more learning to benefit from next generation (<0.13μm)

3D electronics

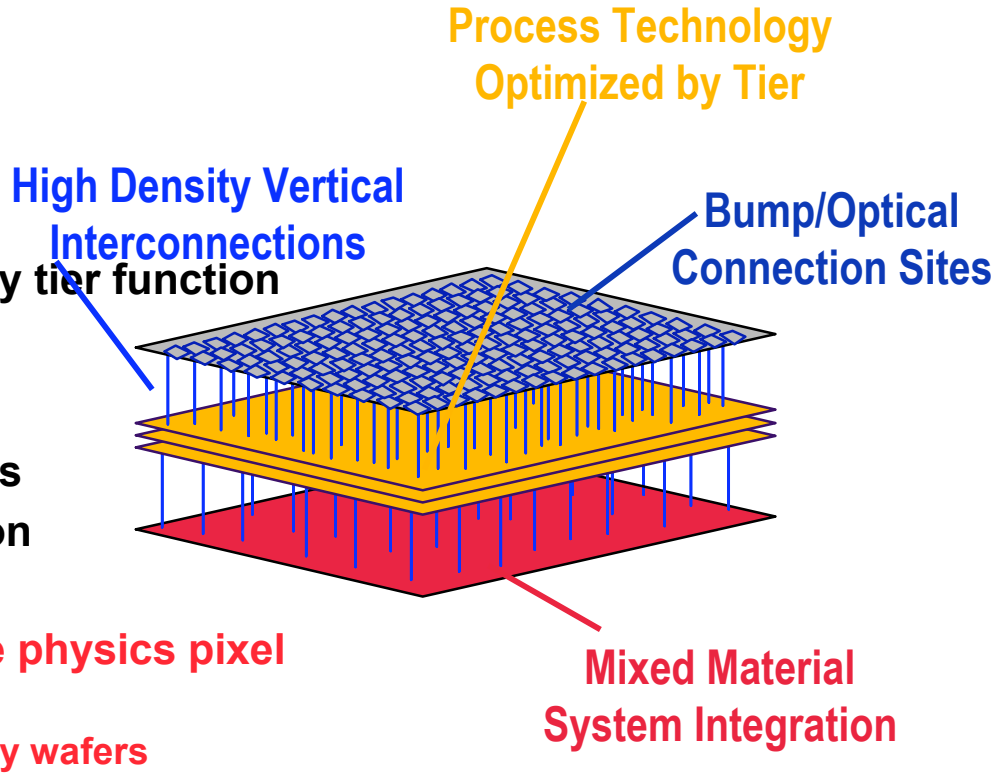
- Impressive progress described by Vyshi Suntharalingam (MIT) and Ray Yarema (FNAL)
- Requirements for HEP front end electronics and detectors continue to push limits for mass, power, and resolution.
  - little room for cooling material and hence low power needed.
  - resolution requires smaller pixels, which increases readout circuit density.
- Industry is moving toward 3D to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk
- Developments include sizeable sensors with high yield of pixels and MPW runs - industry and research community
  - NB new design tools needed as well as technology

Motivation for 3-D Circuit Technology

- 3-D Circuit = Multi-layer (multi-tier) stacked circuit

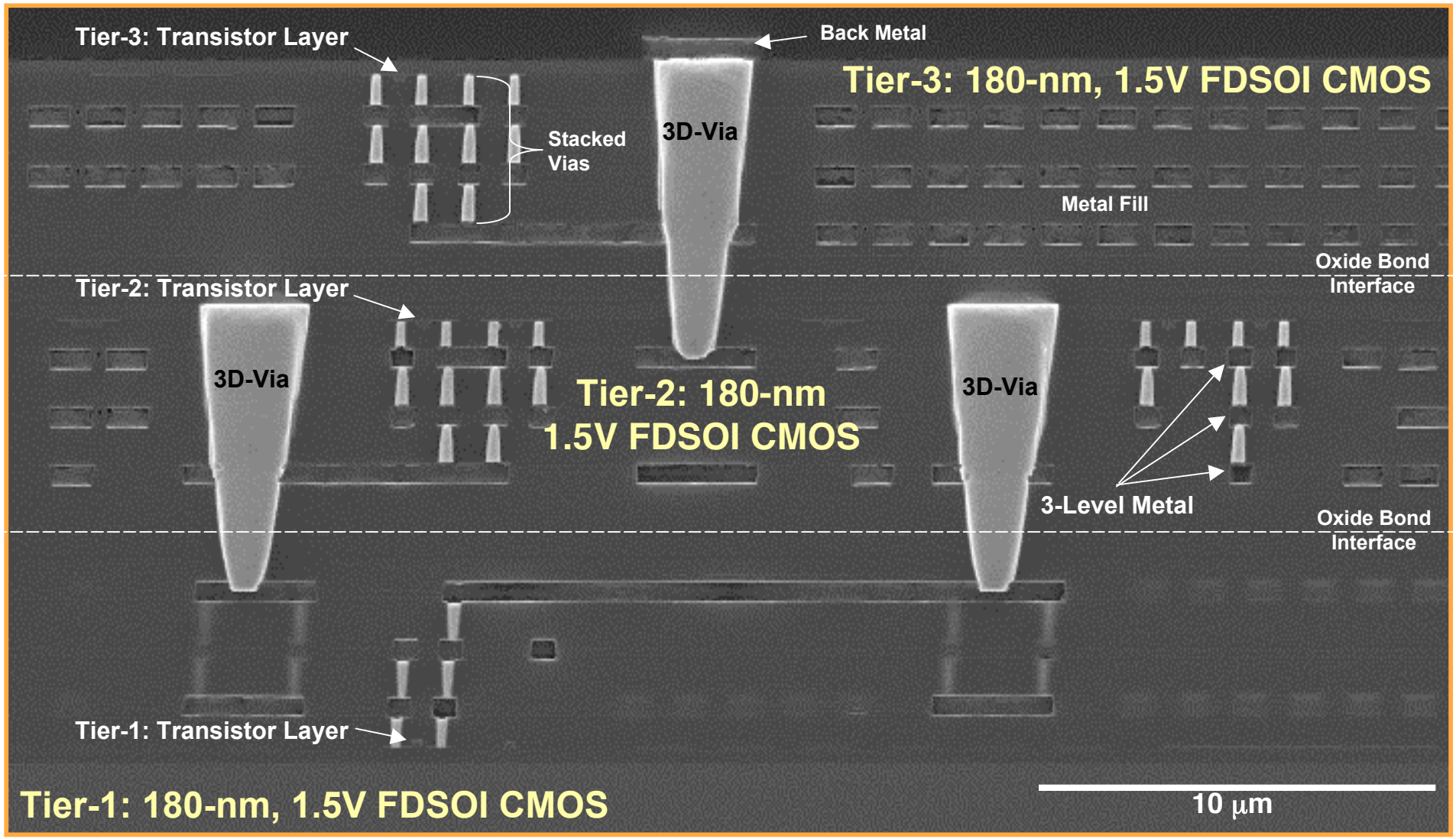
- Advantages
  - Reduced interconnect length
  - Reduced chip size
  - Reduced parasitics
  - Reduced power
  - Fabrication process optimized by tier function

- Applications
  - High bandwidth microprocessors
  - Mixed material system integration
  - Advanced focal planes
  - Obvious possibilities for particle physics pixel detectors
    - Including separate high resistivity wafers



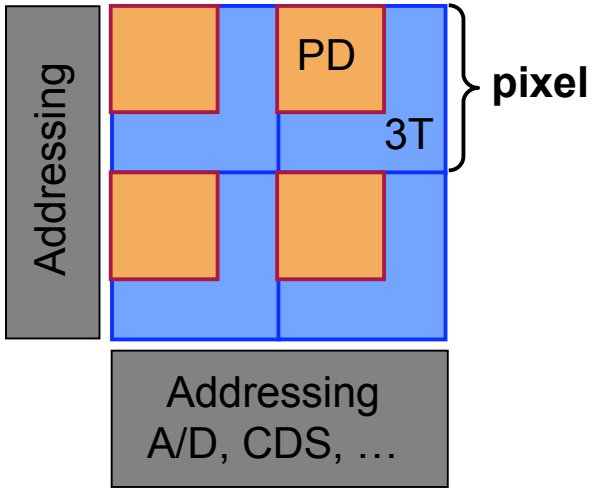
Cross-Section of 3-Tier 3D-integrated Circuit
(DARPA 3DL1 *Multiproject Run*)

3 FDSOI CMOS Transistor Layers, 10-levels of Metal



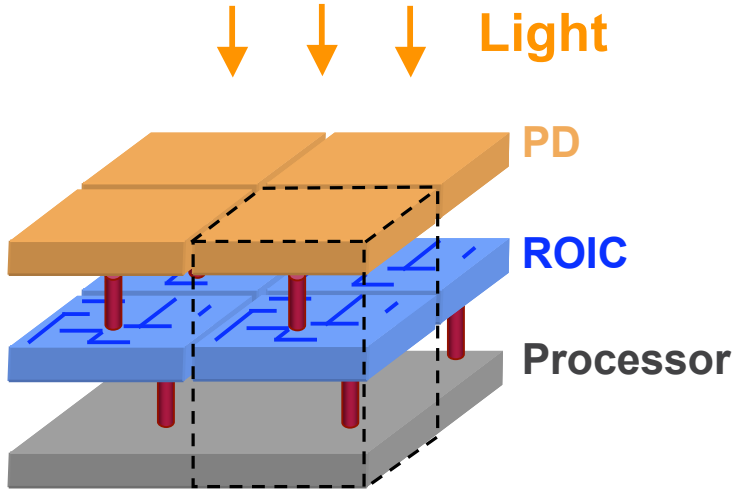
Advantages of Vertical Integration

Conventional Monolithic APS



- Pixel electronics and detectors share area
- Fill factor loss
- Co-optimized fabrication
- Control and support electronics placed outside of imaging area

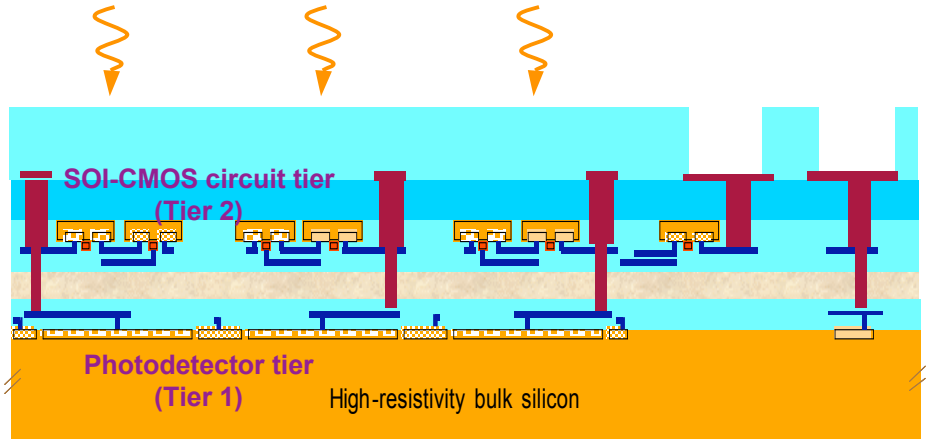
3-D Pixel



- 100% fill factor detector
- Fabrication optimized by layer function
- Local image processing
  - Power and noise management
- Scalable to large-area focal planes

Preliminary Tier-1-2 3D Imager Test Results

- **Electrical probe station preliminary imager test result using *frontside* illumination**
  - **Final processing steps will result in unobstructed backside illuminated device**



35-mm slide image projected through CMOS-circuit-side of 3D-integrated imager on chip test station

1024 x 1024 Image
from *FIRST* 3D-Integrated Wafer Pair*

Image acquired at 10 frames/sec
(Background Subtracted, Pixel Yield > 99.9%, 3.8M transistors)

Parallel sessions

- Clear evolution of emphasis to LHC installation phase
  - Large fraction of contents on production, commissioning, implementation, performance of final systems
    - including some machine electronic systems
  - Reports on installation of infrastructure in underground areas
- Points which emerge
  - Not all procurements are yet complete
    - Our planning & timescales are stressing small manufacturers
    - Installation of some important services is later than users desire
  - Commissioning of final systems in-situ will need time
    - Cabling and (many delicate) interconnections are hard to accelerate
    - Few electronics systems are “switch-on and go”
  - Operation of all systems together will be a new experience

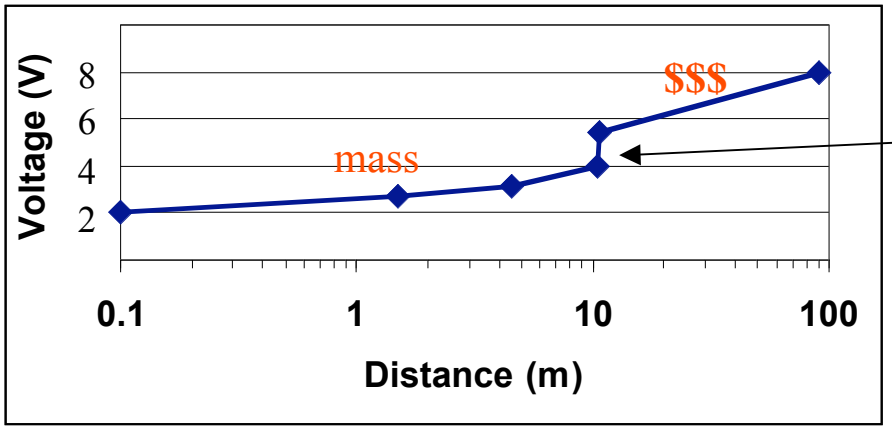
Upgrades for SLHC

- Not yet ready with experiment plans, but several critical areas identified and discussed
  - Power
  - Data and control communications
  - Clock, trigger and control distribution
    - + need to converge, with machine, on acceptable clock frequency
- Some scope for common efforts but
  - Power delivery (and reduction, if achievable) is **crucial** for upgraded trackers, but not a sexy subject
    - Little work ongoing at present
  - Experiments want possibility to influence developments of future common systems
    - Important to learn from past experiences

From R Ely, M Garcia-Sciveres

High Power + Low Voltage = MASS + $$$

Next time, deliver power at higher voltage



Voltage between +ve and ground leads vs. distance from module

Remote sensing rad.-hard **linear** regulators necessary for safe operation

- Pixel Electronics operate at ~2V => large current
- ~2A low voltage per module (1744 modules) -3488A!

- Work in ATLAS
- Serial Power (*reported LECC 2005*)
  - Demonstrated with present Pixel modules by Bonn
  - SCT modules and staves by RAL and LBNL
- DC-DC converters proposed by LBNL
  - Prototype switches fabricated and tested

Optical links

- Now a foundation stone technology
  - Vital for future readout and control systems
  - Essential for low mass, high speed, low noise
  - Much has been learned in LHC experiment applications
- Still not inconceivable to re-use some components
  - But drive/receive electronics must be new
- Active collaboration being developed
  - ATLAS + CMS + CERN + …
- Many would like to see standard technology adopted
  - Not yet clear how easy this will be

Margins for operation at SLHC (6: summary)

Francois Vasey (CERN)

- Tx and Rx need careful study
  - Are we reaching the limit?
  - Rx SEE sensitivity to be mitigated
- Fiber
  - Radiation tolerance probably OK
  - Capacity increase OK in SM, NOT OK in SIMM, OK in GRIN
- Electronics
  - Generalized Bottleneck
- Geometry
  - Possibility to move away from beam axis to gain margin against radiation damage

- Good overall agreement between ATLAS and CMS observations

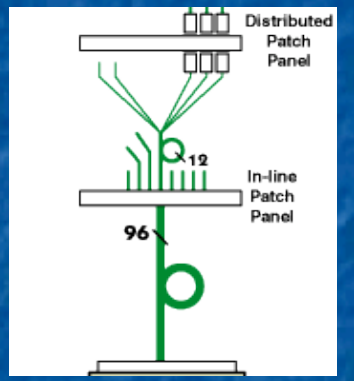
The Options for an Upgrade (1)

- Reuse the existing system
  - Check margins carefully
  - Boost analog link capacity by developing CODEC and MODEM
    - See paper by S. Dris
- Reuse the fiber plant only
  - Develop TRx, SERDES and CODEC
    - See paper by P. Moreira
  - Check compatibility and margins of legacy fiber and connectors
- Start from scratch
  - Possibly using components identical to existing ones
- A combination of the above
  - Geometry dependent system implementation

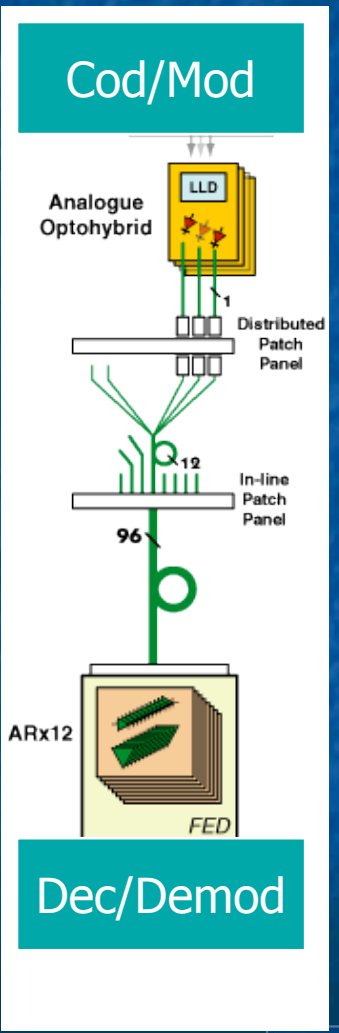
?

Francois Vasey (CERN)

Cod
Ser
Tx



Rx
Des
Dec



Future

- The conference remains useful with a strong commitment from a sizeable community of regular participants
  - 13th LHC electronics workshop
  - Prague, Czech Republic 3-7 September 2007
- LECC & the workshop should contribute in reporting and influencing the development of upgrades
  - Other activities, eg ILC, can also profit from LHC experience
- HEP depends heavily on electronic technologies
  - Some are advanced, and we need to learn and adapt to them
  - others are mundane but are now on very large scale
- LHC physics depends on successfully installed and commissioned electronic systems
  - It's too early to assume this will be easy and much remains to be done
  - Managing risk under schedule and resource pressures should be a concern