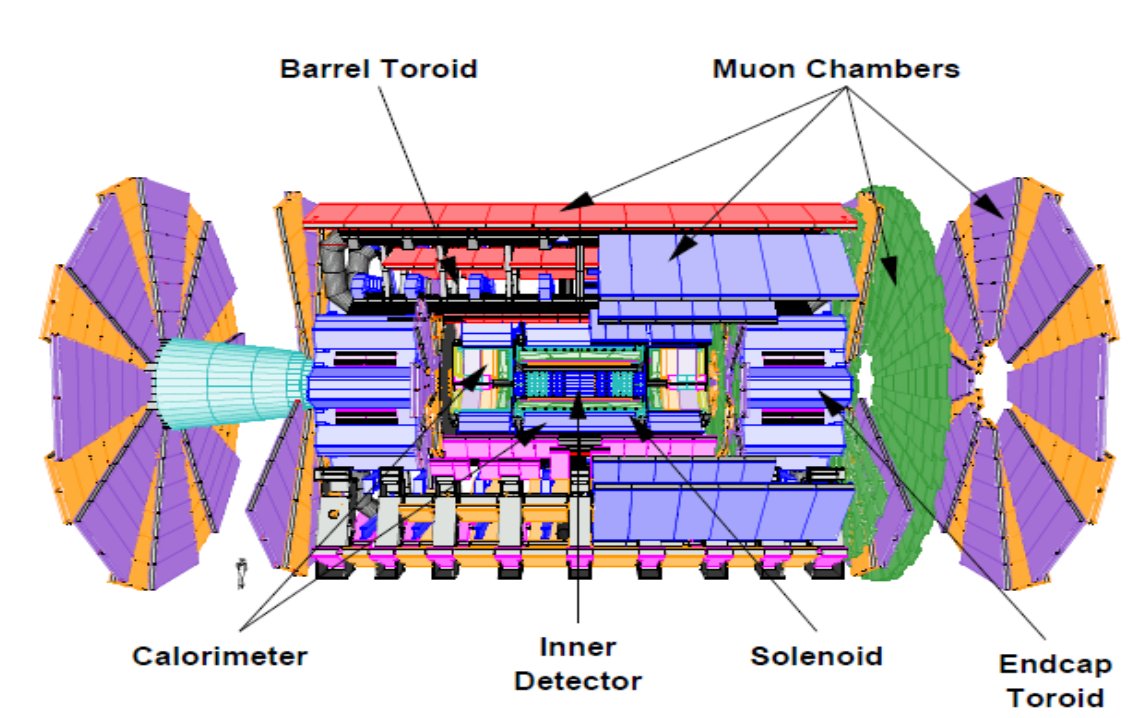




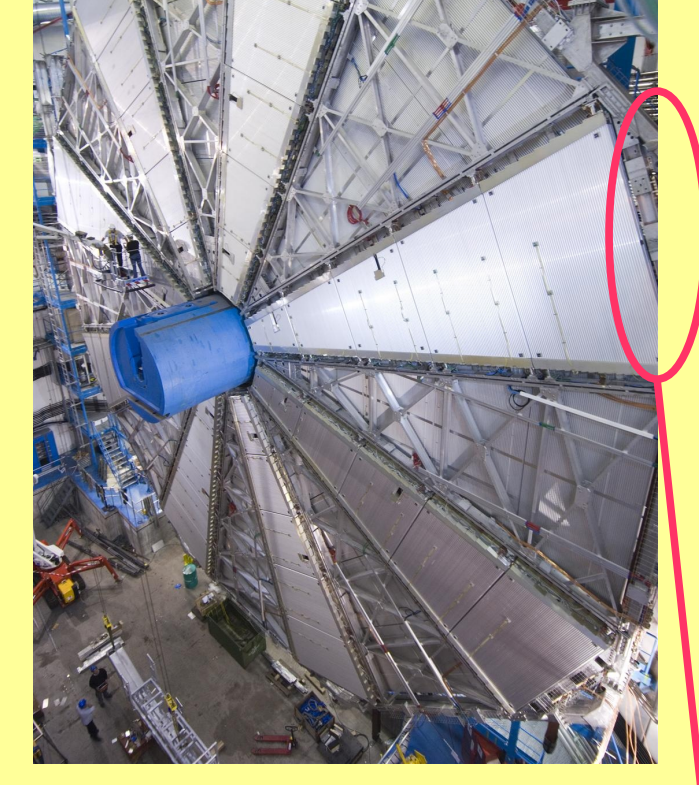
A Preamp-Shaper-Discriminator Chip for the ATLAS MDT Upgrade in a 130nm CMOS technology

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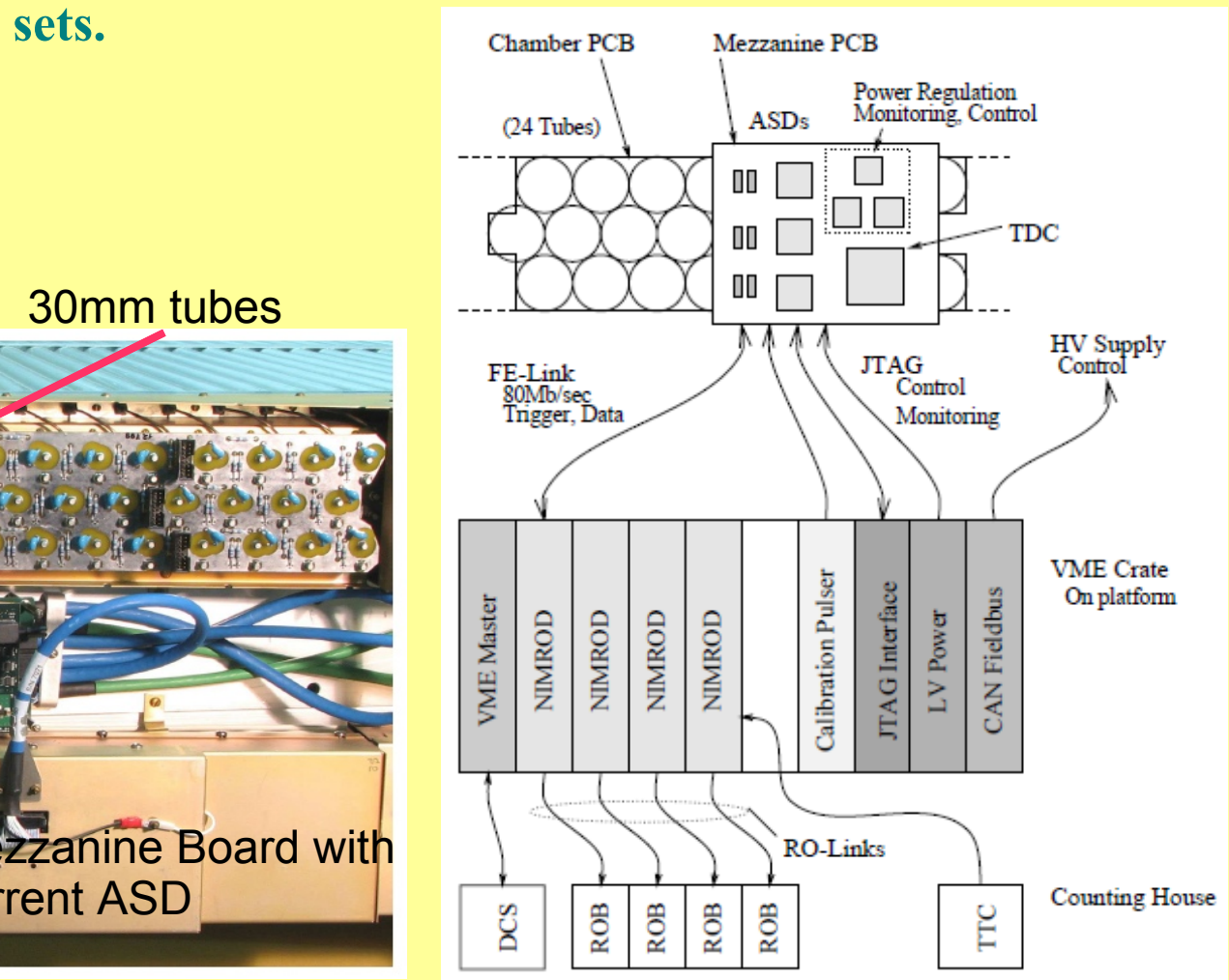
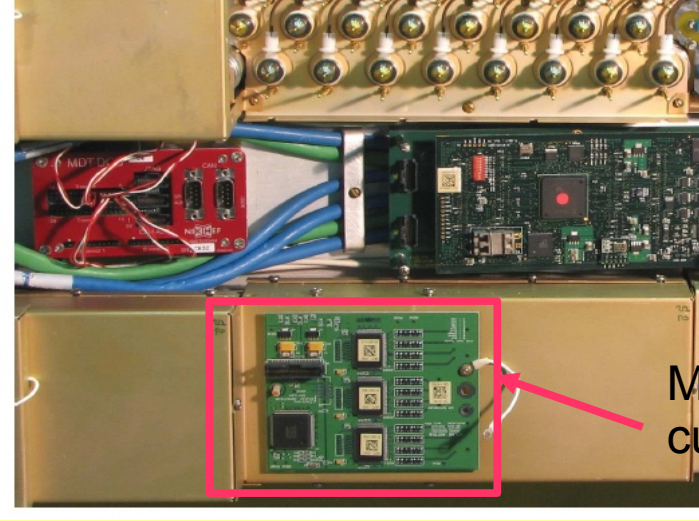
Current Muon Drift Tubes (MDT) Electronics in ATLAS

MDT Big Wheel Side C



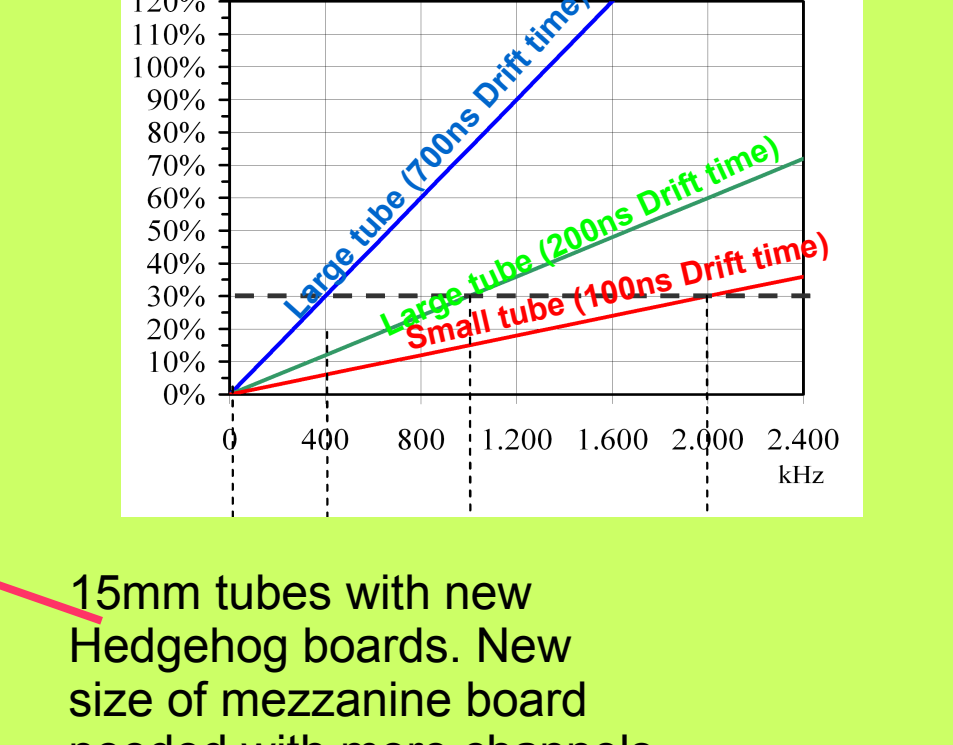
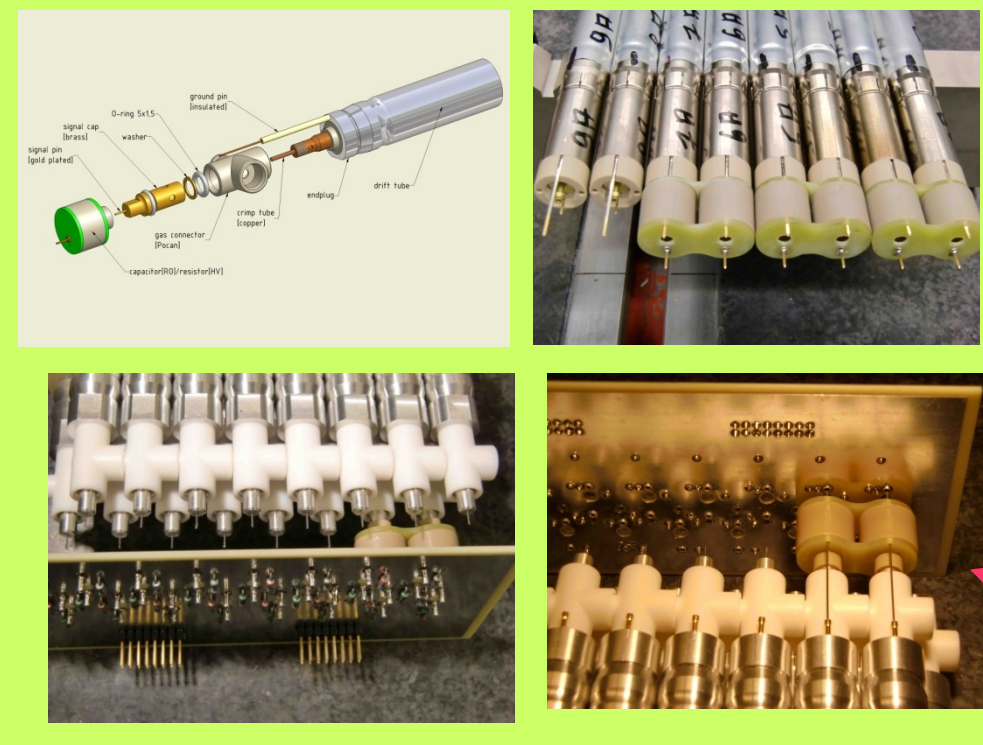
- The ATLAS MDT system consists of about 350,000 pressurized drift tubes of 3 cm diameter
- The MDTs are read out by an ASD at one end, and the other end is terminated with the characteristic impedance of the tube (370 Ω)
- To minimize cost, the MDT signals are carried on twolayer "hedgehog boards" that to a mezzanine board, which contains 24 readout channels: 3 Octal ASDs, a single 24-channel TDC, and associated control circuitry. A single MDT chamber may have as many as 432 drift tubes or 18 hedgehog/mezzanine board sets.

MDT Electronics



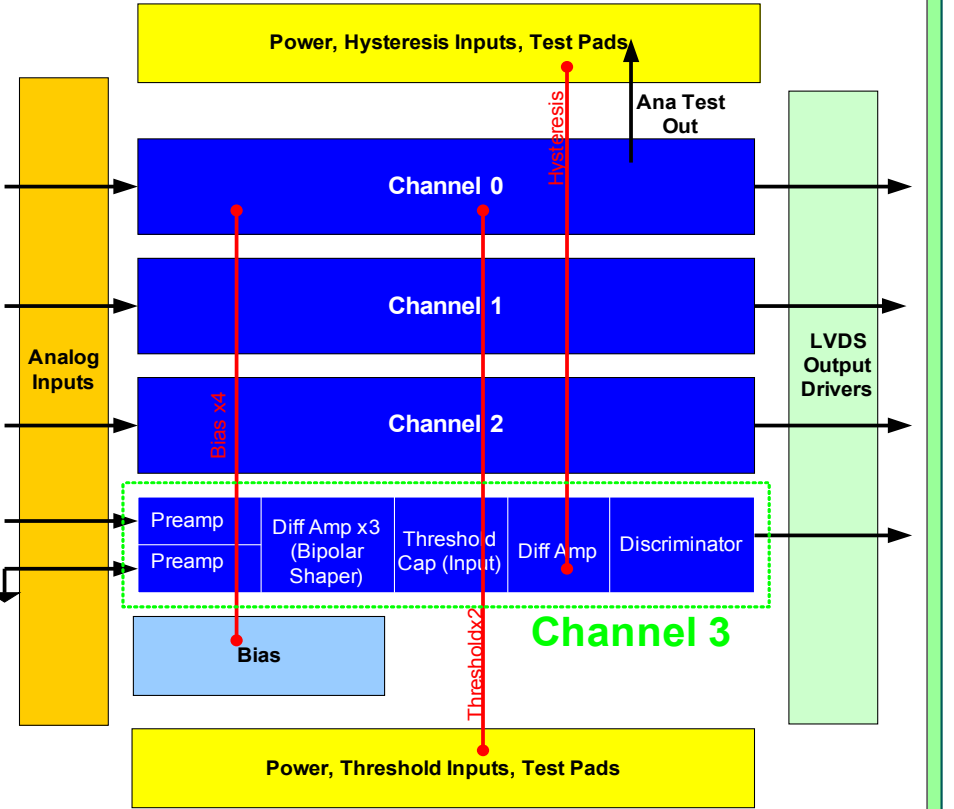
ASD Chip Upgrade Motivation

- Readout system BW designed for 400kHz/tube, which is insufficient in forward region at high sLHC background rates. Smaller tubes and new corresponding front-end electronics are required.
- Need to integrate more channels on single ASD chip (> 8)
- Insufficient # of existing ASD chips available for testing, production
- Re-spin of old chip (in HP 0.5um) not feasible
- Integration into new L1 trigger scheme (muon track trigger)
- Voltage Regulators on-chip, better PSRR. Lower supply voltage?
- Need to reduce Mezzanine board size due to smaller 15mm tube size
- Fix pair-mode problem (flip flop meta-stability)
- Max drift time of new 15mm tubes is 200ns; programmable deadtime



Front-end (ASD) Chip Overview

- 4 identical Analog-only Channels
- TOT-mode only, no Wilkinson ADC
- 'Global' Threshold and Hysteresis supplied from DACs off-chip
- Similar schematics to previous chip, so direct technology comparison possible
- Output must be compatible to existing TDC
- No JTAG, scan chain implemented
- 44-pin Kyocera ceramic QFP
- 2.1mm x 2.1mm total size
- ESD devices used on input, output



Package Pin #	Chip Pin #	Name	IO	Function
1	1	VDD1	IO	Power Supply (VDD1)
2	2	VSS1	IO	Power Supply (VSS1)
3	3	VDD2	IO	Power Supply (VDD2)
4	4	VSS2	IO	Power Supply (VSS2)
5	5	VDD3	IO	Power Supply (VDD3)
6	6	VSS3	IO	Power Supply (VSS3)
7	7	VDD4	IO	Power Supply (VDD4)
8	8	VSS4	IO	Power Supply (VSS4)
9	9	IN0P	IO	Analog Input 0 (Positive)
10	10	IN0N	IO	Analog Input 0 (Negative)
11	11	IN1P	IO	Analog Input 1 (Positive)
12	12	IN1N	IO	Analog Input 1 (Negative)
13	13	IN2P	IO	Analog Input 2 (Positive)
14	14	IN2N	IO	Analog Input 2 (Negative)
15	15	IN3P	IO	Analog Input 3 (Positive)
16	16	IN3N	IO	Analog Input 3 (Negative)
17	17	OUT0P	IO	Analog Output 0 (Positive)
18	18	OUT0N	IO	Analog Output 0 (Negative)
19	19	OUT1P	IO	Analog Output 1 (Positive)
20	20	OUT1N	IO	Analog Output 1 (Negative)
21	21	OUT2P	IO	Analog Output 2 (Positive)
22	22	OUT2N	IO	Analog Output 2 (Negative)
23	23	OUT3P	IO	Analog Output 3 (Positive)
24	24	OUT3N	IO	Analog Output 3 (Negative)
25	25	TEST0	IO	Test Pad 0
26	26	TEST1	IO	Test Pad 1
27	27	TEST2	IO	Test Pad 2
28	28	TEST3	IO	Test Pad 3
29	29	TEST4	IO	Test Pad 4
30	30	TEST5	IO	Test Pad 5
31	31	TEST6	IO	Test Pad 6
32	32	TEST7	IO	Test Pad 7
33	33	TEST8	IO	Test Pad 8
34	34	TEST9	IO	Test Pad 9
35	35	TEST10	IO	Test Pad 10
36	36	TEST11	IO	Test Pad 11
37	37	TEST12	IO	Test Pad 12
38	38	TEST13	IO	Test Pad 13
39	39	TEST14	IO	Test Pad 14
40	40	TEST15	IO	Test Pad 15
41	41	TEST16	IO	Test Pad 16
42	42	TEST17	IO	Test Pad 17
43	43	TEST18	IO	Test Pad 18
44	44	TEST19	IO	Test Pad 19
45	45	TEST20	IO	Test Pad 20
46	46	TEST21	IO	Test Pad 21
47	47	TEST22	IO	Test Pad 22
48	48	TEST23	IO	Test Pad 23
49	49	TEST24	IO	Test Pad 24
50	50	TEST25	IO	Test Pad 25
51	51	TEST26	IO	Test Pad 26
52	52	TEST27	IO	Test Pad 27
53	53	TEST28	IO	Test Pad 28
54	54	TEST29	IO	Test Pad 29
55	55	TEST30	IO	Test Pad 30
56	56	TEST31	IO	Test Pad 31
57	57	TEST32	IO	Test Pad 32
58	58	TEST33	IO	Test Pad 33
59	59	TEST34	IO	Test Pad 34
60	60	TEST35	IO	Test Pad 35
61	61	TEST36	IO	Test Pad 36
62	62	TEST37	IO	Test Pad 37
63	63	TEST38	IO	Test Pad 38
64	64	TEST39	IO	Test Pad 39
65	65	TEST40	IO	Test Pad 40
66	66	TEST41	IO	Test Pad 41
67	67	TEST42	IO	Test Pad 42
68	68	TEST43	IO	Test Pad 43
69	69	TEST44	IO	Test Pad 44
70	70	TEST45	IO	Test Pad 45
71	71	TEST46	IO	Test Pad 46
72	72	TEST47	IO	Test Pad 47
73	73	TEST48	IO	Test Pad 48
74	74	TEST49	IO	Test Pad 49
75	75	TEST50	IO	Test Pad 50
76	76	TEST51	IO	Test Pad 51
77	77	TEST52	IO	Test Pad 52
78	78	TEST53	IO	Test Pad 53
79	79	TEST54	IO	Test Pad 54
80	80	TEST55	IO	Test Pad 55
81	81	TEST56	IO	Test Pad 56
82	82	TEST57	IO	Test Pad 57
83	83	TEST58	IO	Test Pad 58
84	84	TEST59	IO	Test Pad 59
85	85	TEST60	IO	Test Pad 60
86	86	TEST61	IO	Test Pad 61
87	87	TEST62	IO	Test Pad 62
88	88	TEST63	IO	Test Pad 63
89	89	TEST64	IO	Test Pad 64
90	90	TEST65	IO	Test Pad 65
91	91	TEST66	IO	Test Pad 66
92	92	TEST67	IO	Test Pad 67
93	93	TEST68	IO	Test Pad 68
94	94	TEST69	IO	Test Pad 69
95	95	TEST70	IO	Test Pad 70
96	96	TEST71	IO	Test Pad 71
97	97	TEST72	IO	Test Pad 72
98	98	TEST73	IO	Test Pad 73
99	99	TEST74	IO	Test Pad 74
100	100	TEST75	IO	Test Pad 75
101	101	TEST76	IO	Test Pad 76
102	102	TEST77	IO	Test Pad 77
103	103	TEST78	IO	Test Pad 78
104	104	TEST79	IO	Test Pad 79
105	105	TEST80	IO	Test Pad 80
106	106	TEST81	IO	Test Pad 81
107	107	TEST82	IO	Test Pad 82
108	108	TEST83	IO	Test Pad 83
109	109	TEST84	IO	Test Pad 84
110	110	TEST85	IO	Test Pad 85
111	111	TEST86	IO	Test Pad 86
112	112	TEST87	IO	Test Pad 87
113	113	TEST88	IO	Test Pad 88
114	114	TEST89	IO	Test Pad 89
115	115	TEST90	IO	Test Pad 90
116	116	TEST91	IO	Test Pad 91
117	117	TEST92	IO	Test Pad 92
118	118	TEST93	IO	Test Pad 93
119	119	TEST94	IO	Test Pad 94
120	120	TEST95	IO	Test Pad 95
121	121	TEST96	IO	Test Pad 96
122	122	TEST97	IO	Test Pad 97
123	123	TEST98	IO	Test Pad 98
124	124	TEST99	IO	Test Pad 99
125	125	TEST100	IO	Test Pad 100

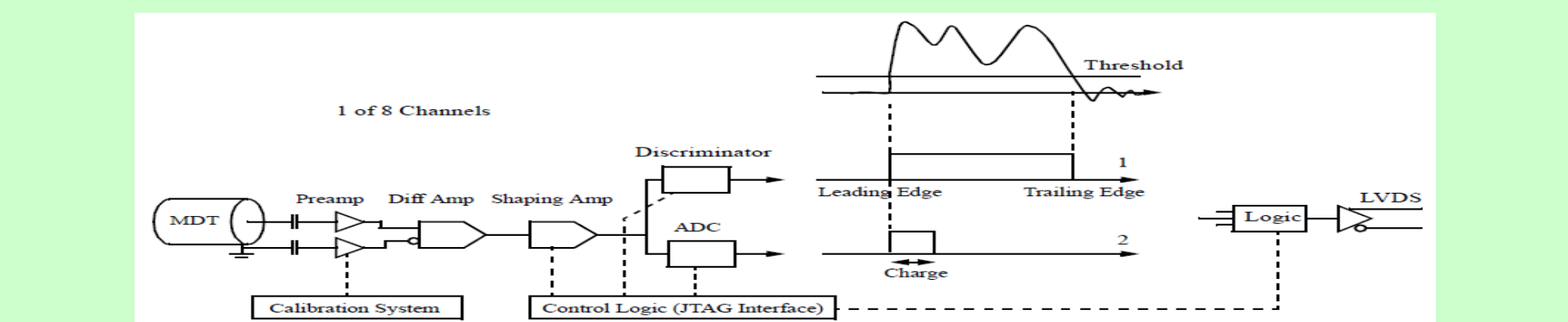
Technology Overview

- IBM 130nm technology is a proven, rad tolerant, well-established and supported technology used in many LHC chip designs already at CERN
- Pure CMOS 8RF-DM technology (no bipolar)
- Thick-oxide 3.3V NMOS/PMOS for entire design. No thin oxide.
- Submitted design on MPW through CERN/MOSIS in 05/2009
- Rad-hard technology (proton, gamma tested; neutron not tested)
- Good Design kit, detailed models and tech documentation (Mixed-signal design possible with Europractice tools available)
- MIM-cap and MOS caps available
- 4 MPW runs per year possible with MOSIS. (4 planned in 2011)
- Detailed modelling of various devices; STI stress, well proximity
- Wide choice of devices available, design kit is flexible.

Process	8RF-DM	8RF-DW	SWL	SNP	SEF	SLP/RF
Process	130nm	130nm	130nm SIGE	130nm SIGE	90nm	90nm
Vdd (V)	1.2/1.5	1.2/1.5	1.2	1.2	1.2	1.0/1.2
Pad cell (V)	2.5/3.3	2.5/3.3	2.5/3.3	2.5/3.3	2.5	2.5
Level of Metals	6-8	6-8	6-8	6-8	4-10	4-10
Metallization	Cu	Cu + Al	Cu + Al	Cu + Al	Cu	Cu
Analog Thick Metal	No	Yes	Yes	Yes	No	No
Density (kg/mm ²)	200	200	200	200	400	400
Power (µm/Hz/gate)	0.009	0.009	0.009	0.009	0.006	0.006
Ring Osc. Delays (ps)	27	27	27	27	21	21
Bipolar beta	-	-	230	600	-	-
Bipolar ft (GHz)	-	-	100	200	-	-
MIMcap (fF/µm ²)	n/a	2.05	4.1	1.0	n/a	n/a
VNCPAP (fF/µm ²)	n/a	1.3	1.3	n/a	n/a	n/a
Resistors	n'diff, p' n' poly, tantalum	n'diff, p' n' poly, tantalum	n'diff, p' n' poly, tantalum	n'diff, p' n' poly, tantalum	n'diff, p' n' poly, tantalum	n'diff, p' n' poly, tantalum
else	yes	yes	yes	yes	yes	yes

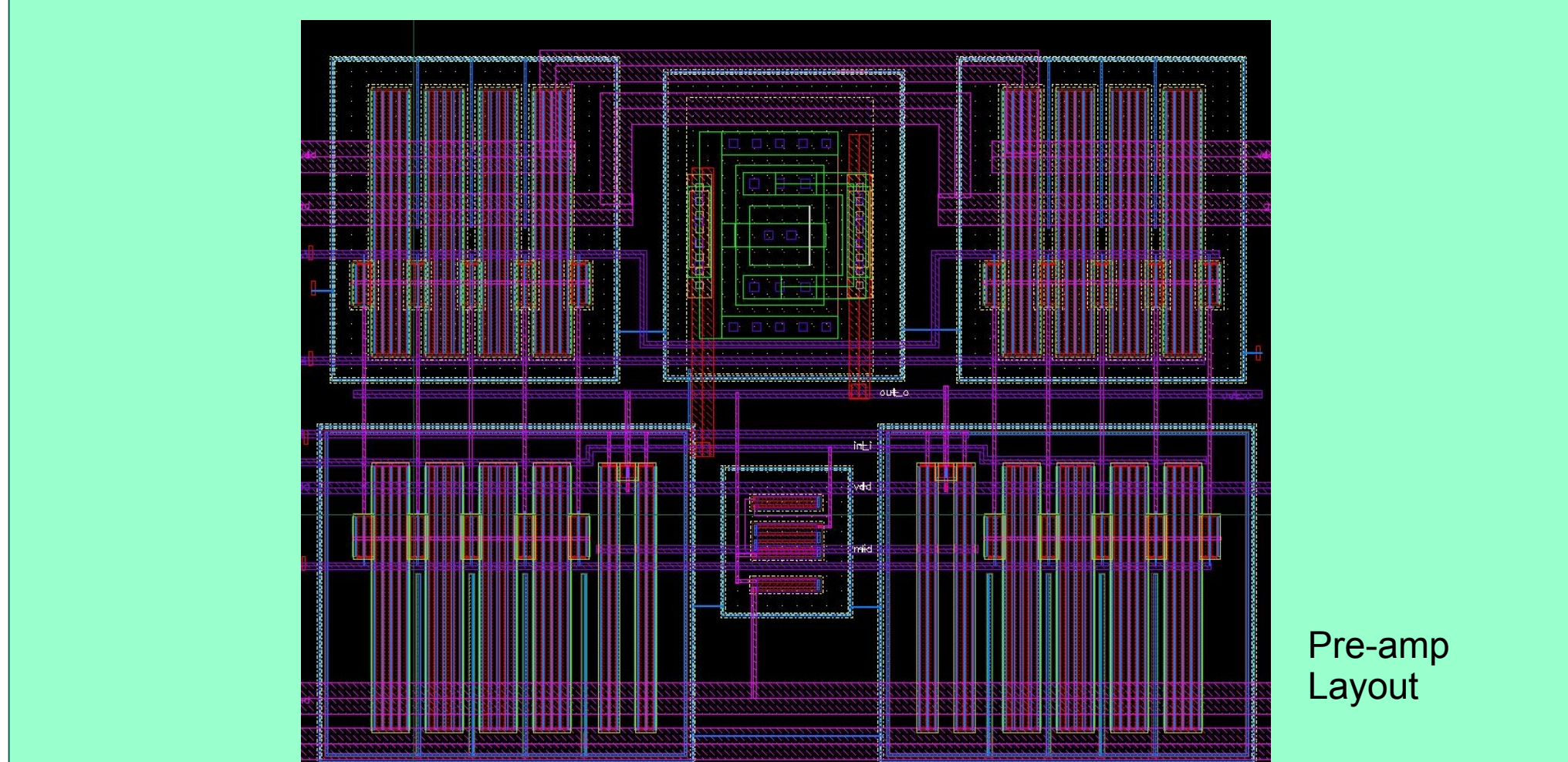
Chip Requirements

Input Impedance	120Ω
Noise	ENC=6000e- rms (or 4 pc-)
Shaping	Bipolar
Shaper Peaking Time	15ns
Linear Range	1.5V or 500 pc-
Nominal threshold setting	60mV or 20 pc- (6noise)
Supply Voltage	3.3V
Power dissipation	< 33mW per channel
Output to TDC	LVDS
Gain Uniformity	< 2%
# of Channels	4 (>8 on following chips)
Channel Crosstalk	< 1.5%
Preamp Charge Gain	1mV/fC
Signal Path	differential
Chip Mode	TOT only (no digital)



Layout Issues

- Separate substrate / Gnd pins, better for noise
- Power wiring done on AL - MA/E1 layers (7mohm)
- Matching / Symmetry of Analog Differential circuits important
- Numerous guard rings to reduce substrate noise and coupling
- Symmetric pad layout; Supply pads placed strategically on chip edges
- Double-diode ESD protection used on channel inputs and outputs
- MIM caps and oppres resistors used for shapers
- Dummy NMOS, PMOS, and resistors used in design for matching.
- Common centroid layout used where possible

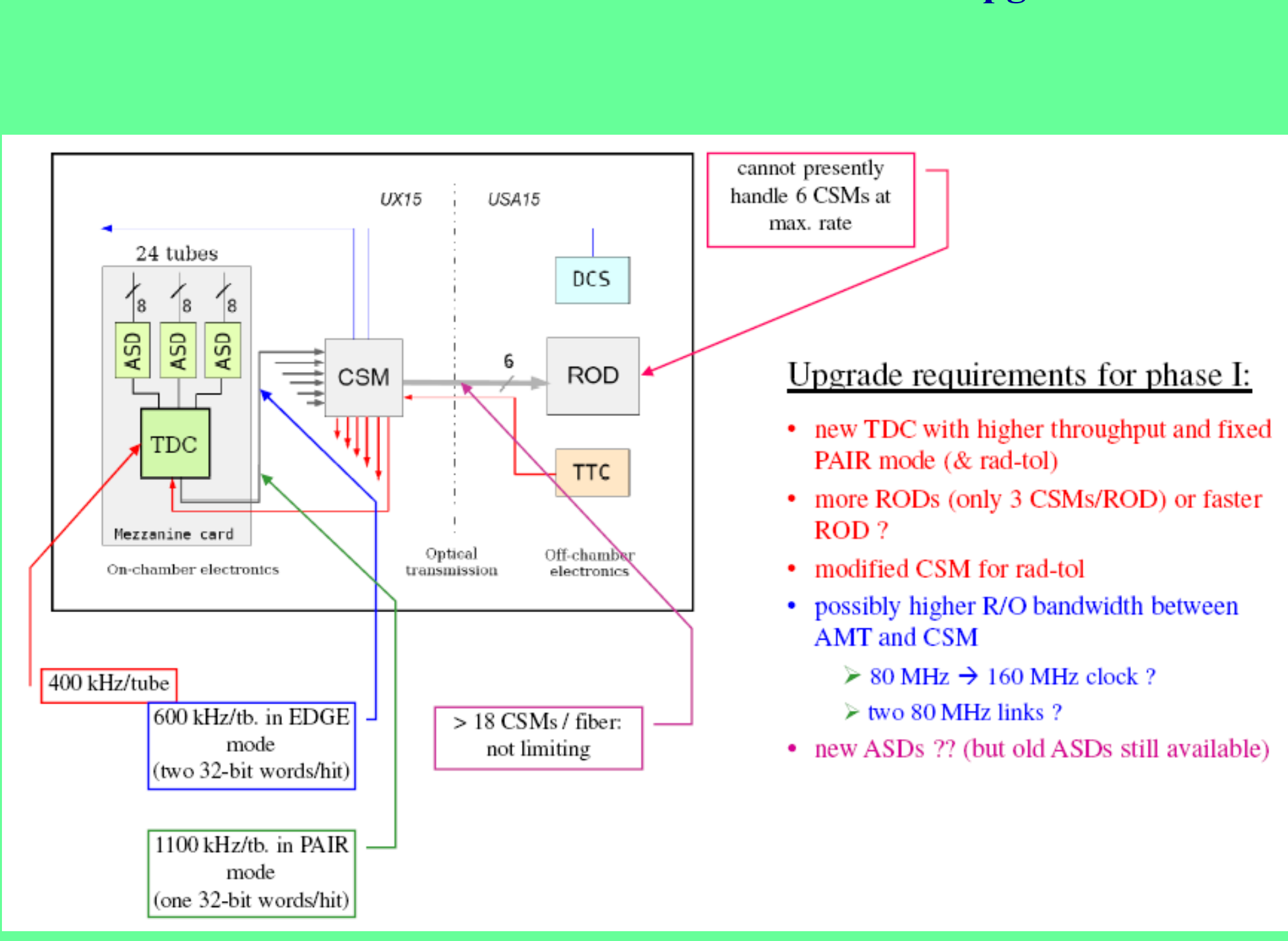


Test Setup



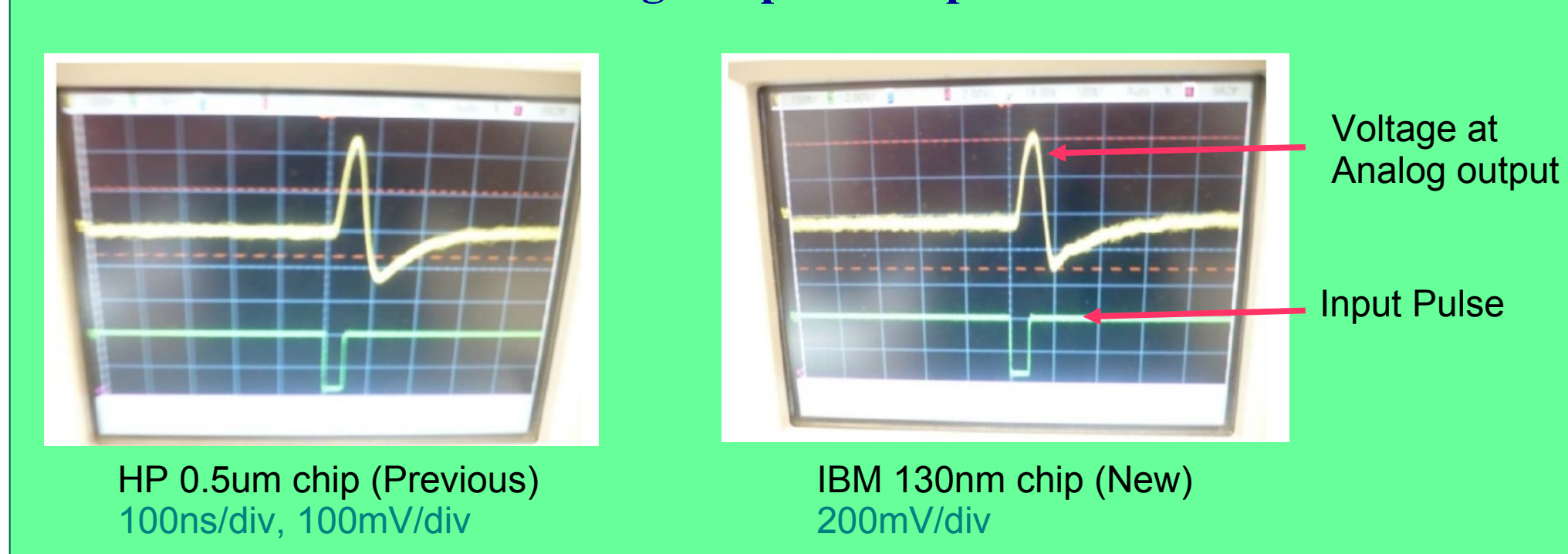
New Mezzanine card (2-layer PCB) with new 2xASD mounted side-by-side comparison of previous chip/card and new

Limitation of Readout Bandwidth for Upgrade



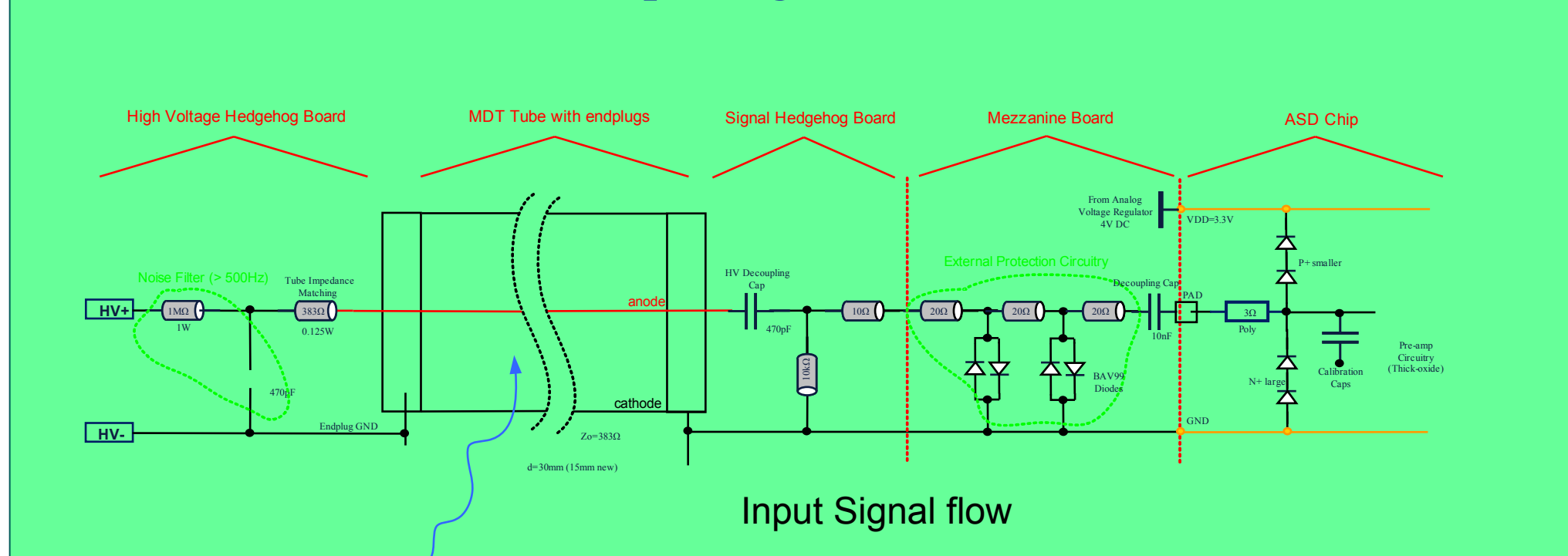
- Upgrade requirements for phase I:
 - new TDC with higher throughput and fixed PAIR mode (& rad-tol)
 - more RODs (only 3 CSMs/ROD) or faster ROD?
 - modified CSM for rad-tol
 - possibly higher R/O bandwidth between AMT and CSM
 - > 80 MHz → 160 MHz clock?
 - two 80 MHz links?
 - new ASDs ?? (but old ASDs still available)

Analog Output Comparison

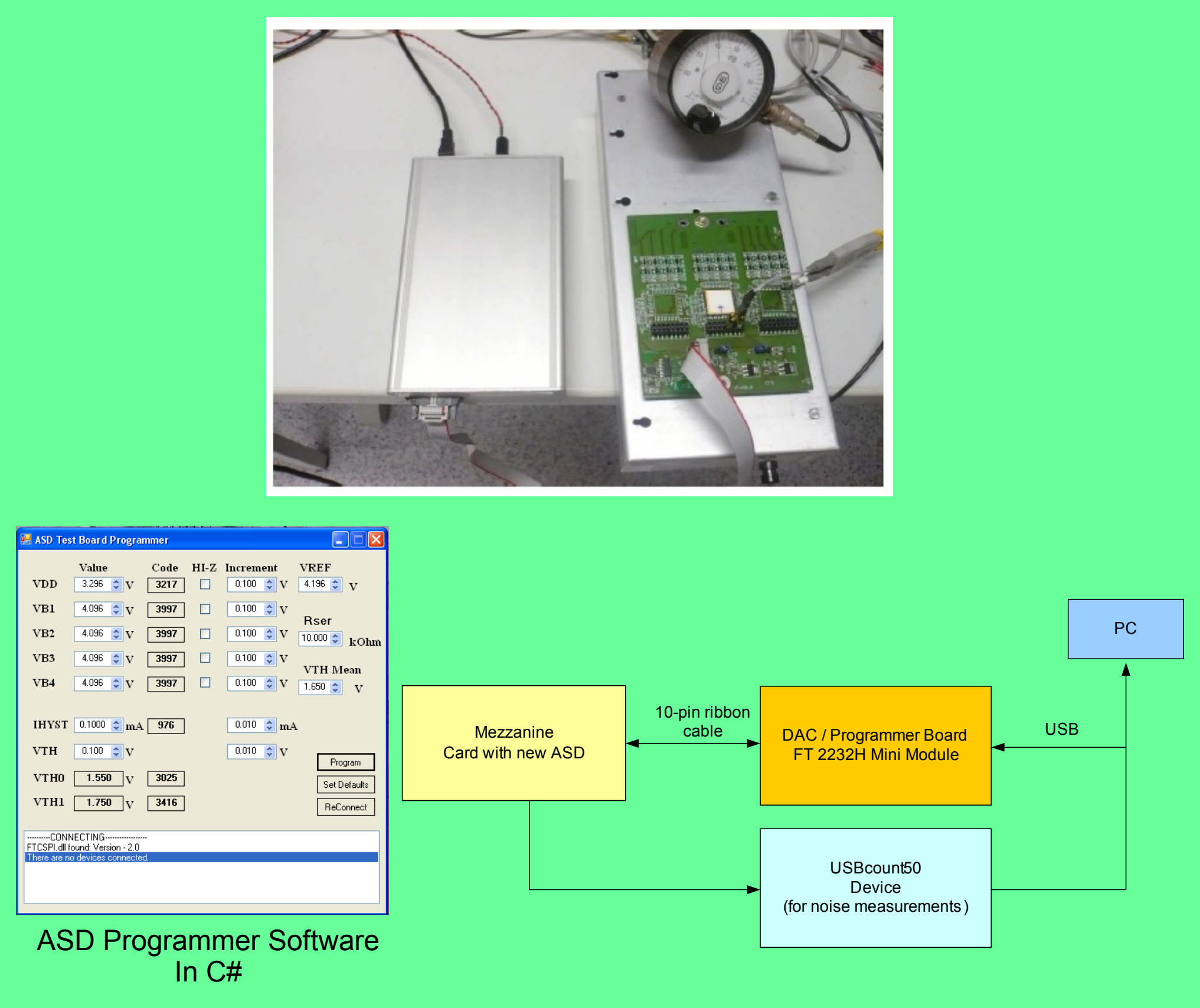


HP 0.5um chip (Previous) 100ns/div, 100mV/div
 IBM 130nm chip (New) 200mV/div

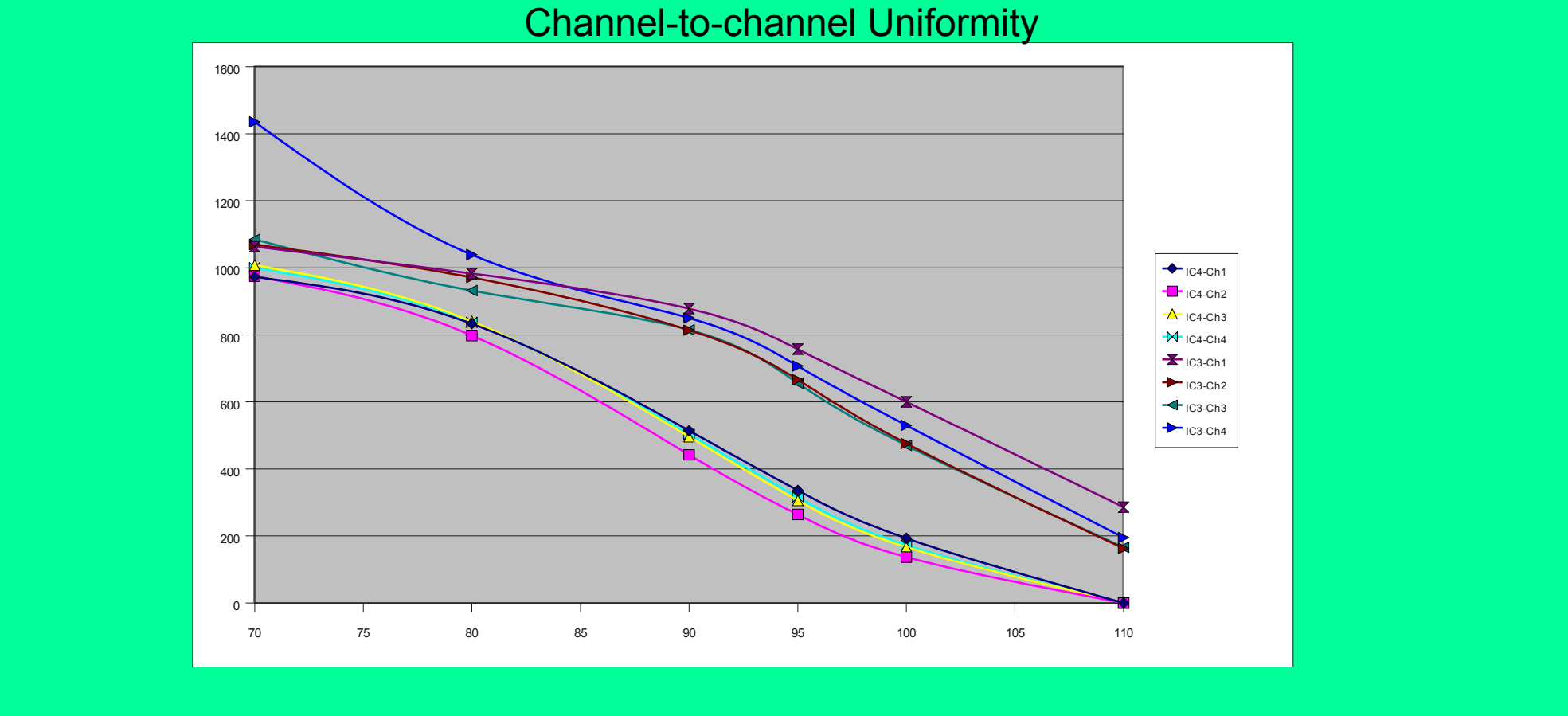
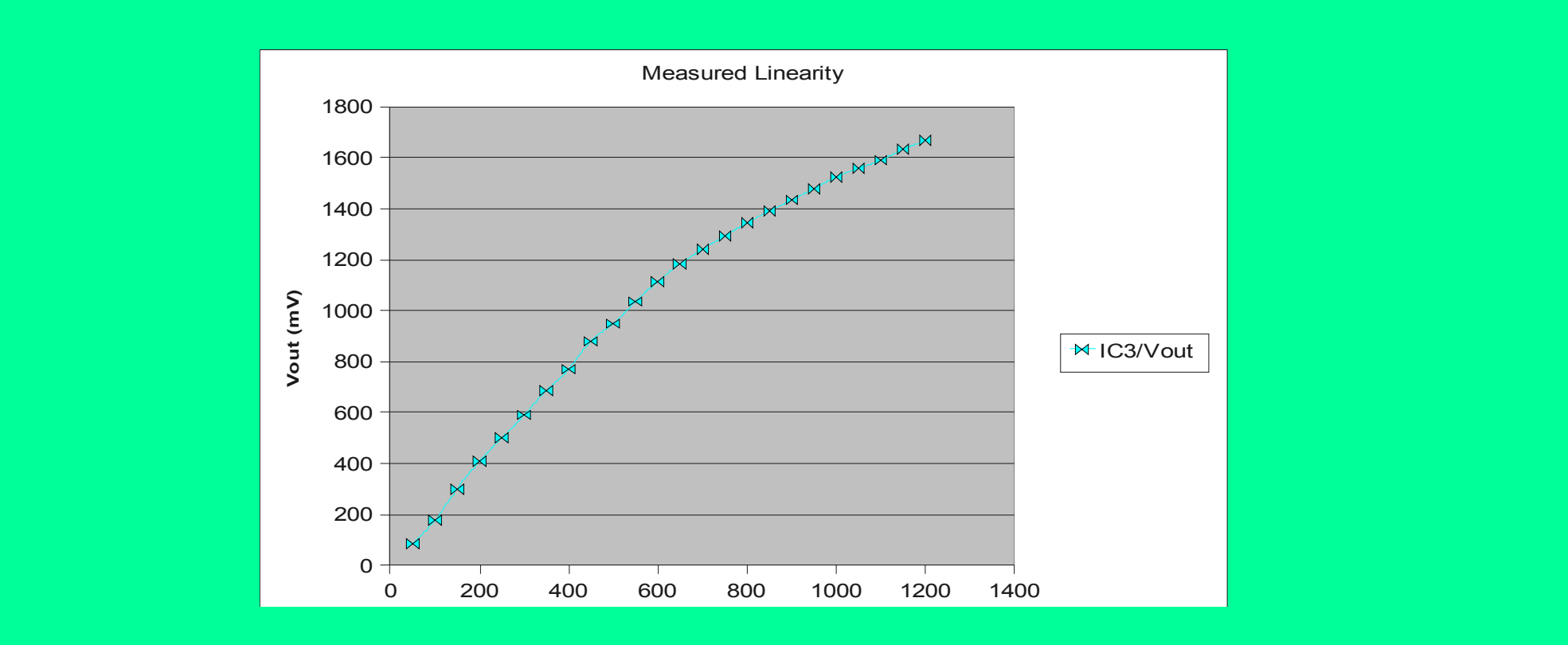
Input Signal Path



Test Setup



Simulations / Measurements



SUMMARY AND OUTLOOK

- We are testing 2 ASD chips that were radiated (neutrons) at Rez, CZ. Results will be known soon.
- The next version of the chip is scheduled for Spring 2011 with MOSIS using the same 130nm technology.
- This version will have DAC/ADCs on chip, calibration input caps, JTAG, and digital logic.
- Areas to improve are the decoupling of the supply net between the output driver and discriminator/preamp.
- More than 8 channels on the chip are also possible.
- Separate (not global) threshold setting will be made.
- More testpads