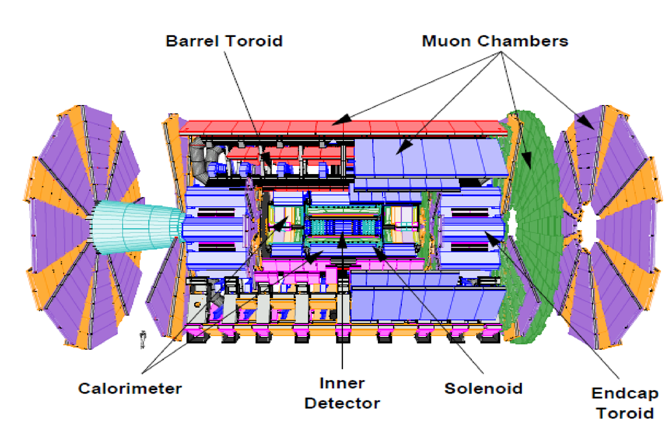
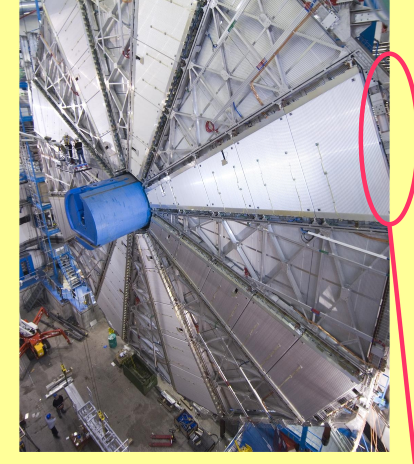


A Preamp-Shaper-Discriminator Chip for the ATLAS MDT Upgrade in a 130nm CMOS technology

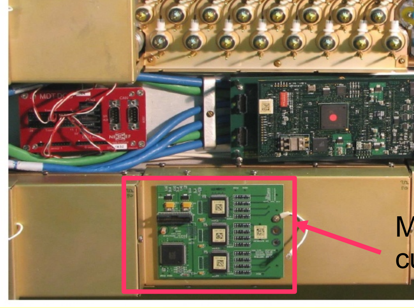
Brad Weber[a], H. Kroha[a], S. Abovyan[b], V. Danielysan[b], O. Reimann[a], R. Richter[a]
[a] Max-Planck-Institut für Physik, Munich
[b] Yerevan Physics Institute, Armenia

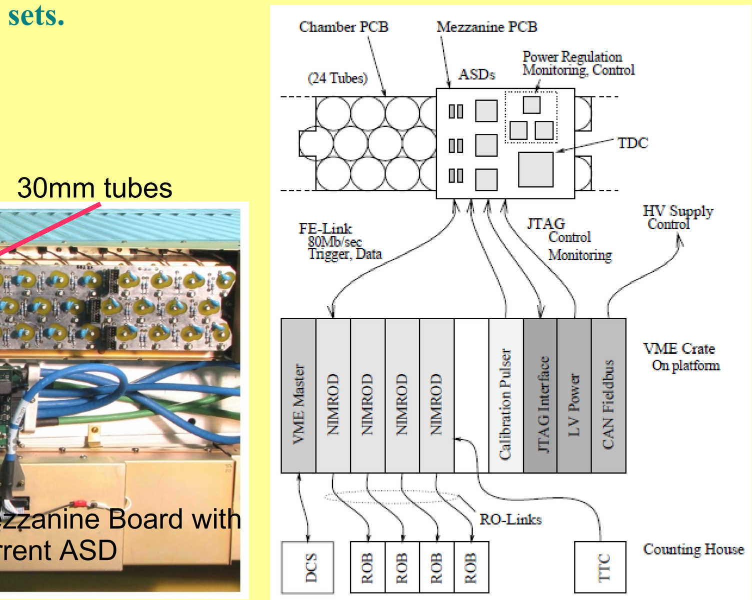
Current Muon Drift Tubes (MDT) Electronics in ATLAS



- The ATLAS MDT system consists of about 350,000 pressurized drift tubes of 3 cm diameter
- The MDTs are read out by an ASD at one end, and the other end is terminated with the characteristic impedance of the tube (370 Ω)
- To minimize cost, the MDT signals are carried on twolayer "hedgehog boards" to a mezzanine board, which contains 24 readout channels: 3 Octal ASDs, a single 24-channel TDC, and associated control circuitry. A single MDT chamber may have as many as 432 drift tubes or 18 hedgehog/mezzanine board sets.

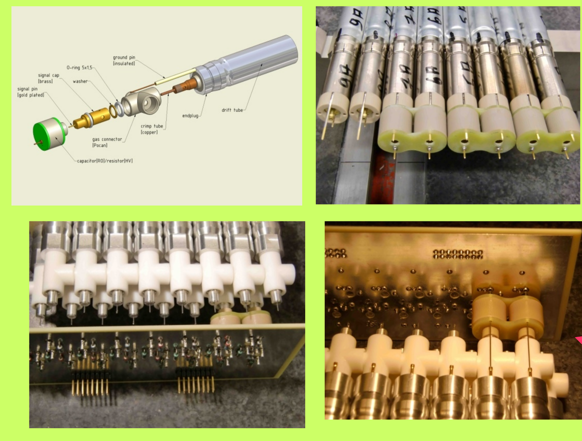
30mm tubes

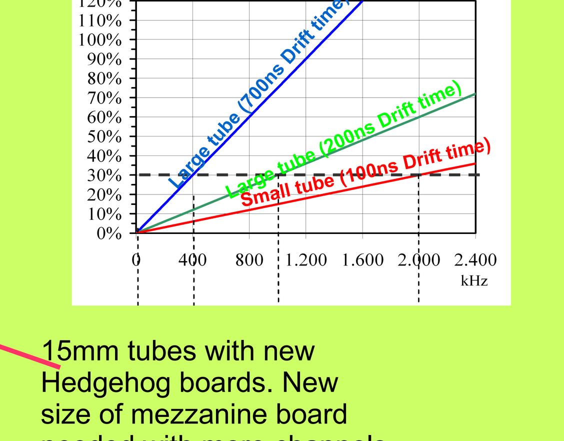




ASD Chip Upgrade Motivation

- Readout system BW designed for 400kHz/tube, which is insufficient in forward region at high sLHC background rates. Smaller tubes and new corresponding front-end electronics are required.
- Need to integrate more channels on single ASD chip (> 8)
- Insufficient # of existing ASD chips available for testing, production
- Re-spin of old chip (in HP 0.5um) not feasible
- Integration into new L1 trigger scheme (muon track trigger)
- Voltage Regulators on-chip, better PSRR. Lower supply voltage?
- Need to reduce Mezzanine board size due to smaller 15mm tube size
- Fix pair-mode problem (flip flop meta-stability)
- Max drift time of new 15mm tubes is 200ns; programmable deadtime

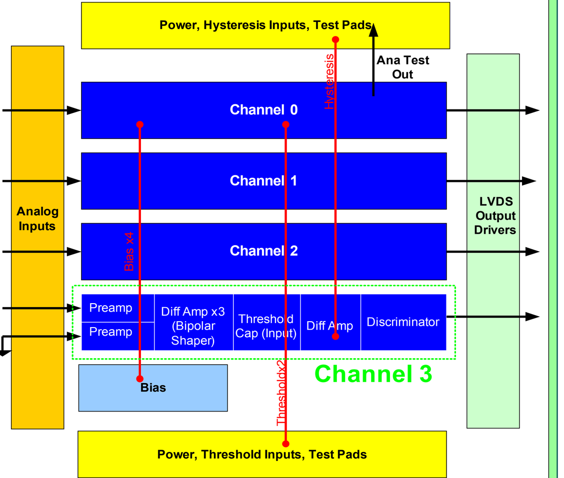




15mm tubes with new Hedgehog boards. New size of mezzanine board needed with more channels.

Front-end (ASD) Chip Overview

- 4 identical Analog-only Channels
- TOT-mode only, no Wilkinson ADC
- 'Global' Threshold and Hysteresis supplied from DACs off-chip
- Similar schematics to previous chip, so direct technology comparison possible
- Output must be compatible to existing TDC
- No JTAG, scan chain implemented
- 44-pin Kyocera ceramic QFP
- 2.1mm x 2.1mm total size
- ESD devices used on input, output



Package Pin #	Chip Pad #	Name	IO	Function
18	1	VSS	IO	Supply Low - GND
19	2	INA0	Input	Preamp Input A (Channel 0)
20	3	INB0	Input	Preamp Input B (Channel 0)
21	4	INA1	Input	Preamp Input A (Channel 1)
22	5	INB1	Input	Preamp Input B (Channel 1)
24	6	INA2	Input	Preamp Input A (Channel 2)
25	7	INB2	Input	Preamp Input B (Channel 2)
26	8	INA3	Input	Preamp Input A (Channel 3)
27	9	INB3	Input	Preamp Input B (Channel 3)
28	10	VDD	IO	Supply High - VDD
29	11	VSS	IO	Supply Low - GND
30	12	VB1	Output	Preamp Bias Voltage 1
31	13	VB2	Output	Preamp Bias Voltage 2
32	14	VB4	Output	Preamp Bias Voltage 4
33	15	VB3	Output	Preamp Bias Voltage 3
35	16	VSS	IO	Supply Low - GND
36	17	VTH0	Input	Discriminator Threshold Input 0
37	18	VTH1	Input	Discriminator Threshold Input 1
38	19	VDD	IO	Supply High - VDD
39	20	VSS	IO	Supply Low - GND
40	21	VDD	IO	Supply High - VDD
41	22	OUTB3	Output	Preamp Output B (Channel 3)
42	23	OUTA3	Output	Preamp Output A (Channel 3)
43	24	OUTB2	Output	Preamp Output B (Channel 2)
44	25	OUTA2	Output	Preamp Output A (Channel 2)
2	26	OUTB1	Output	Preamp Output B (Channel 1)
3	27	OUTA1	Output	Preamp Output A (Channel 1)
4	28	OUTB0	Output	Preamp Output B (Channel 0)
5	29	OUTA0	Output	Preamp Output A (Channel 0)
6	30	VSS	IO	Supply Low - GND
7	31	VDD	IO	Supply High - VDD
8	32	VSS	IO	Supply Low - GND
9	33	ANB0	Output	Analog Line Output A (Channel 0)
10	34	ANA0	Output	Analog Line Output B (Channel 0)
11	35	VDD	IO	Supply High - VDD
13	36	VSS	IO	Supply Low - GND
14	37	VDD	IO	Supply High - VDD
15	38	IHYST	Input	Discriminator Hysteresis Input
16	39	SUB	IO	Substrate (Connect to GND)
17	40	VDD	IO	Supply High - VDD

* Pins (on package) 1, 12, 23, 34 are no connect   VDD=3.3V, VSS=0V
* Package pins are for 44 pin package

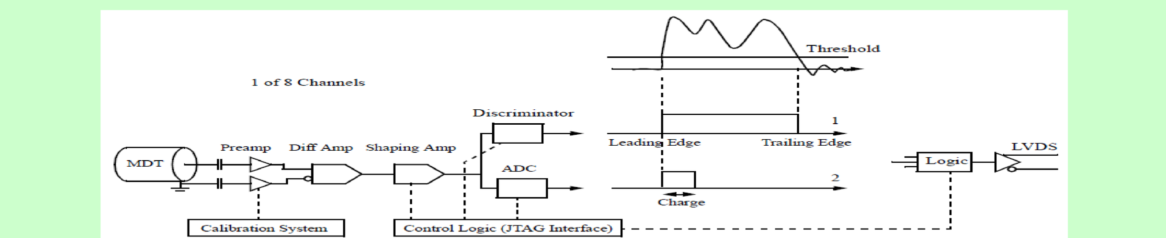
Technology Overview

- IBM 130nm technology is a proven, rad tolerant, well-established and supported technology used in many LHC chip designs already at CERN
- Pure CMOS 8RF-DM technology (no bipolar)
- Thick-oxide 3.3V NMOS/PMOS for entire design. No thin oxide.
- Submitted design on MPW through CERN/MOSIS in 05/2009
- Rad-hard technology (proton, gamma tested; neutron not tested)
- Good Design kit, detailed models and tech documentation (Mixed-signal design possible with Europractice tools available)
- MIM-cap and MOS caps available
- 4 MPW runs per year possible with MOSIS. (4 planned in 2011)
- Detailed modelling of various devices; STI stress, nwell proximity
- Wide choice of devices available, design kit is flexible.

	8RF-LM	8RF-DM	8WL	8HP	9SF	9LP/RF
Process	130nm	130nm	130nm SiGe	130nm SiGe	90nm	90nm
Vdd (V)	1.2/1.5	1.2/1.5	1.2	1.2	1.0/1.2	1.0/1.2
Pad cell (V)	2.5/3.3	2.5/3.3	2.5/3.3	2.5/3.3	2.5	2.5
Level of Metals	6-8	6-8	6-8	6-8	4-10	4-10
Metalization	Cu	Cu + Al	Cu + Al	Cu + Al	Cu	Cu
Analog Thick Metal	No	Yes	Yes	Yes	No	Yes
Density (Kgates/mm2)	200	200	200	200	400	400
Power (μw/MHz/gate)	0.009	0.009	0.009	0.009	0.006	0.006
Ring Osc. Delays (ps)	27	27	27	27	21	21
Bipolar beta	-	-	230	600	-	-
Bipolar ft (GHz)	-	-	100	200	-	-
MIMcap (fF/μm²)	n/a	2.05	4.1	1.0	n/a	
VNCAP (fF/μm²)	n/a	1.3	1.3	n/a	n/a	
Resistors	n⁺diff. p⁺, p⁻ poly. tantalum	n⁺diff. p⁺, p⁻ poly. tantalum	n⁺diff. p⁺, p⁻ poly. p poly tantalum	n⁺diff. p⁺, p⁻ poly. tantalum	n⁺diff. p⁺, p⁻ poly. tantalum	n⁺diff. p⁺, p⁻ poly. tantalum
efuse	yes	yes	yes	yes	yes	yes

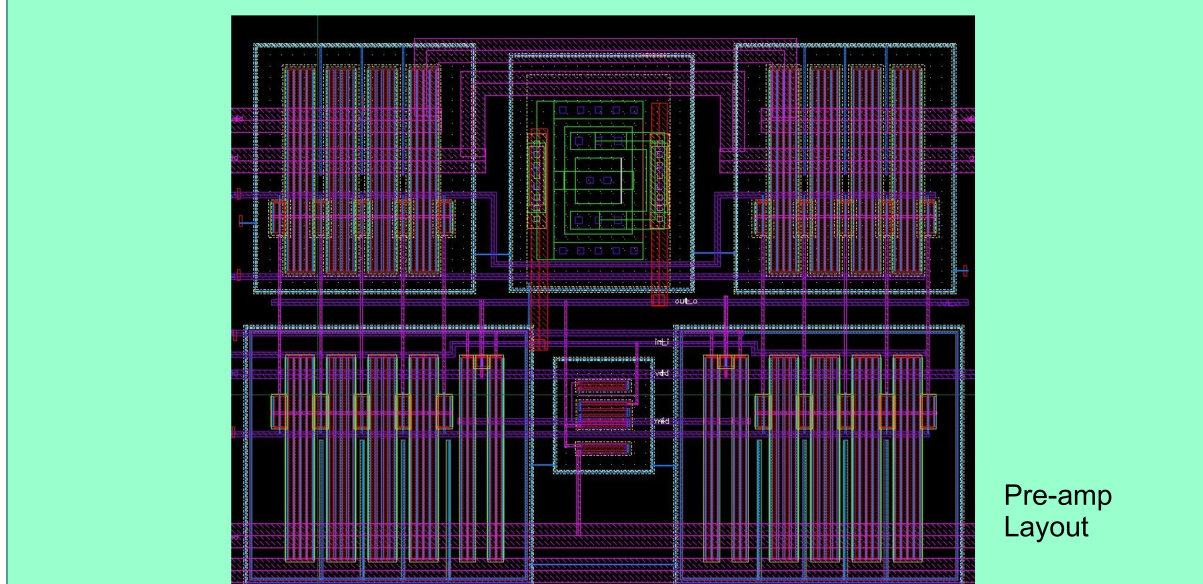
Chip Requirements

Input Impedance	120Ω
Noise	ENC=6000e- rms (or 4 pe-)
Shaping	Bipolar
Shaper Peaking Time	15ns
Linear Range	1.5V or 500 pe-
Nominal threshold setting	60mV or 20 pe- (6σnoise)
Supply Voltage	3.3V
Power dissipation	< 33mW per channel
Output to TDC	LVDS
Gain Uniformity	< 2%
# of Channels	4 (>8 on following chips)
Channel Crosstalk	< 1.5%
Preamp Charge Gain	1mV/fC
Signal Path	differential
Chip Mode	TOT only (no digital)



Layout Issues

- Seperate substrate / Gnd pins, better for noise
- Power wiring done on AL - MA/E1 layers (7mohm)
- Matching / Symmetry of Analog Differential circuits important
- Numerous guard rings to reduce substrate noise and coupling
- Symmetric pad layout; Supply pads placed strategically on chip edges
- Double-diode ESD protection used on channel inputs and outputs
- MIM caps and opppcres resistors used for shapers
- Dummy NMOS, PMOS, and resistors used in design for matching.
- Common centroid layout used where possible

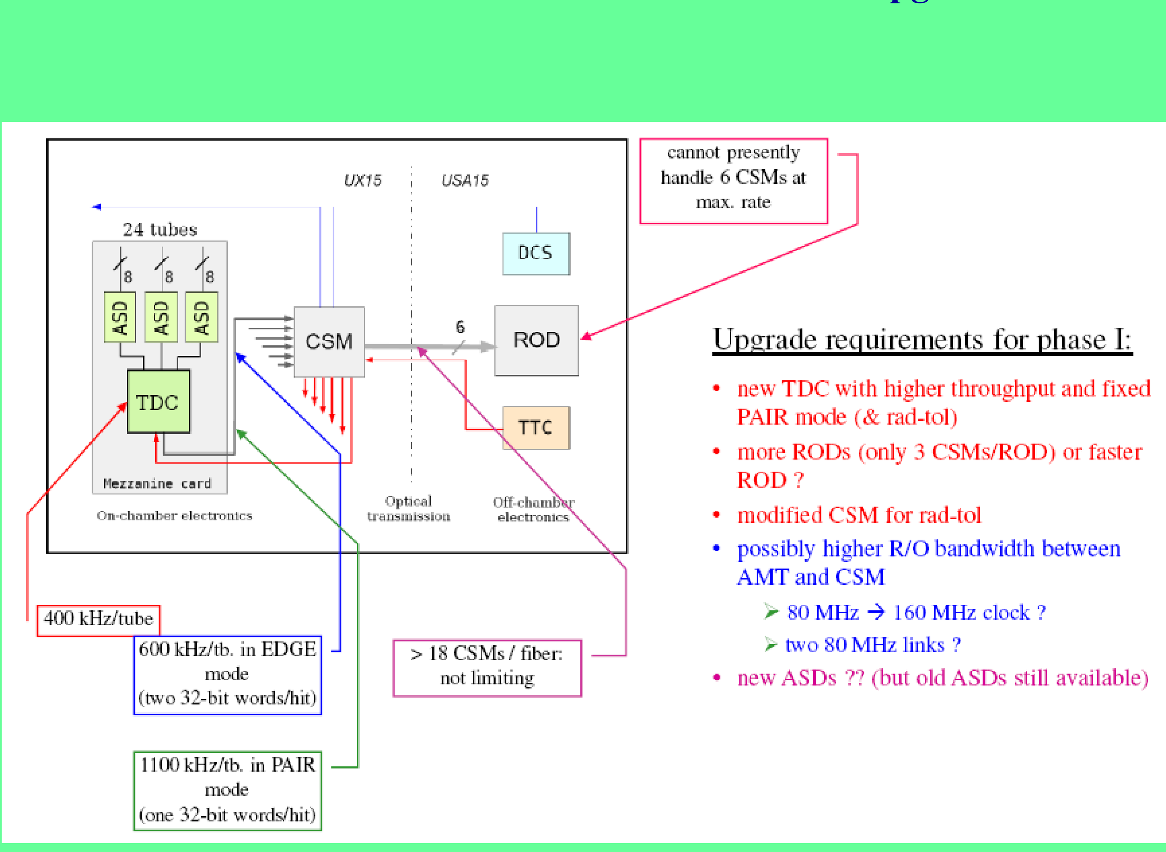


Test Setup

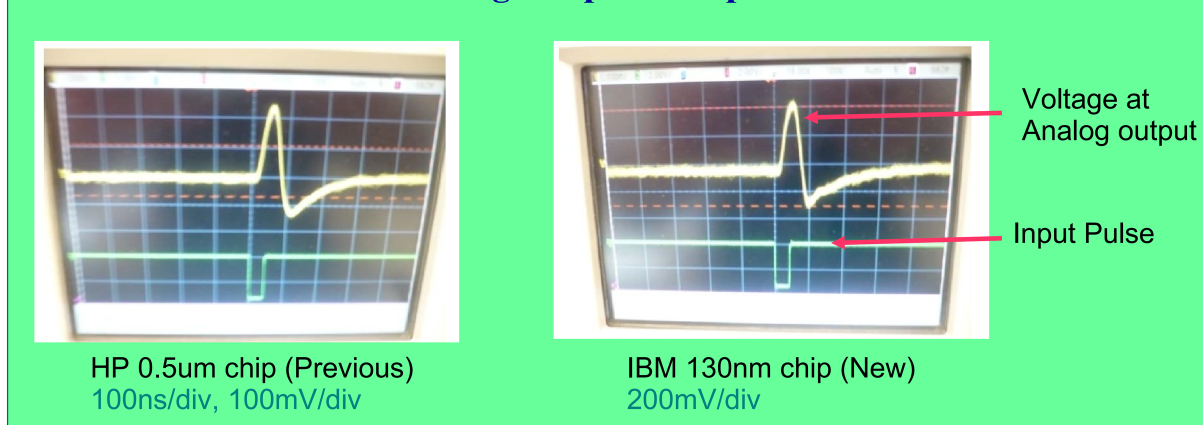
New Mezzanine card (2-layer PCB) with new 2xASD mounted

Side-by-side comparison of previous chip/card and new

Limitation of Readout Bandwidth for Upgrade



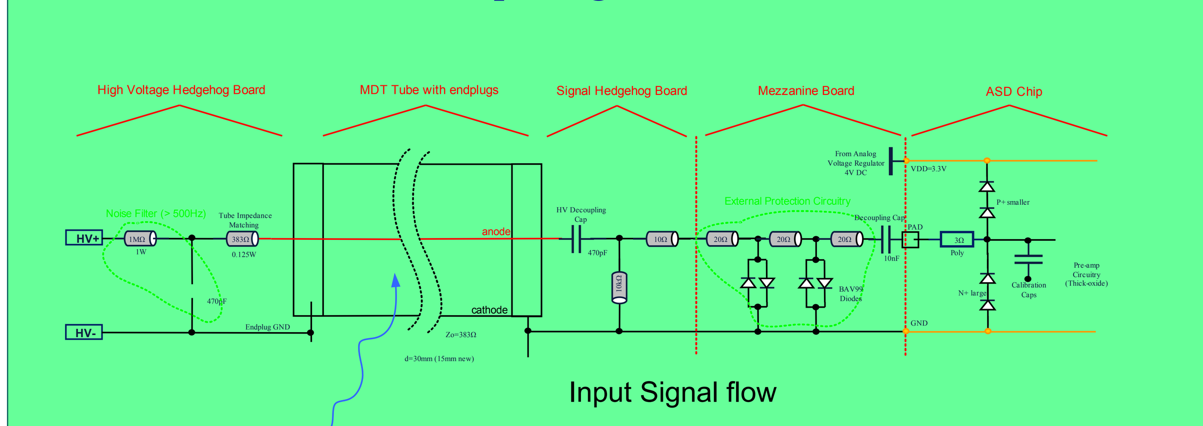
Analog Output Comparison



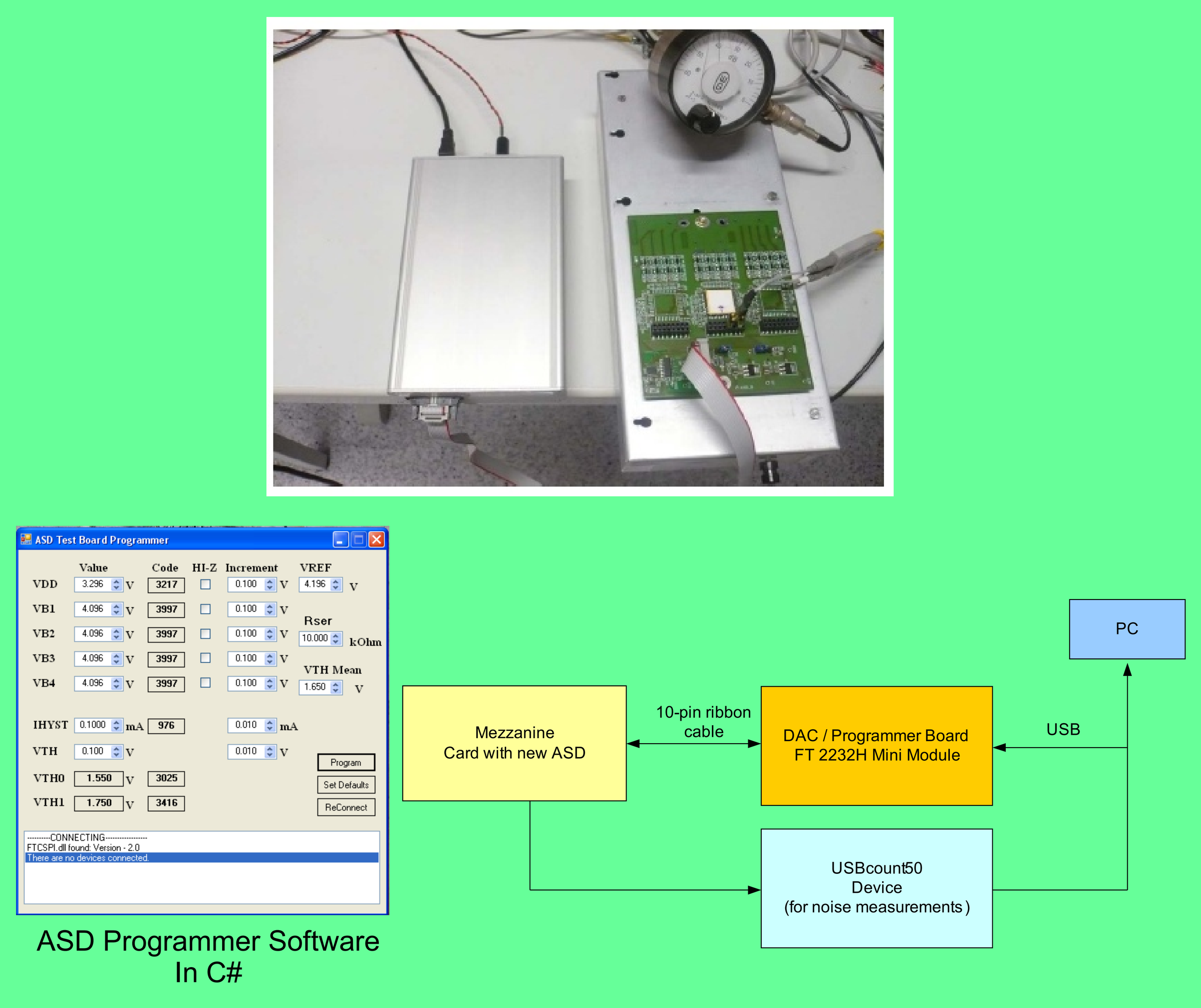
HP 0.5um chip (Previous)
100ns/div, 100mV/div

IBM 130nm chip (New)
200mV/div

Input Signal Path

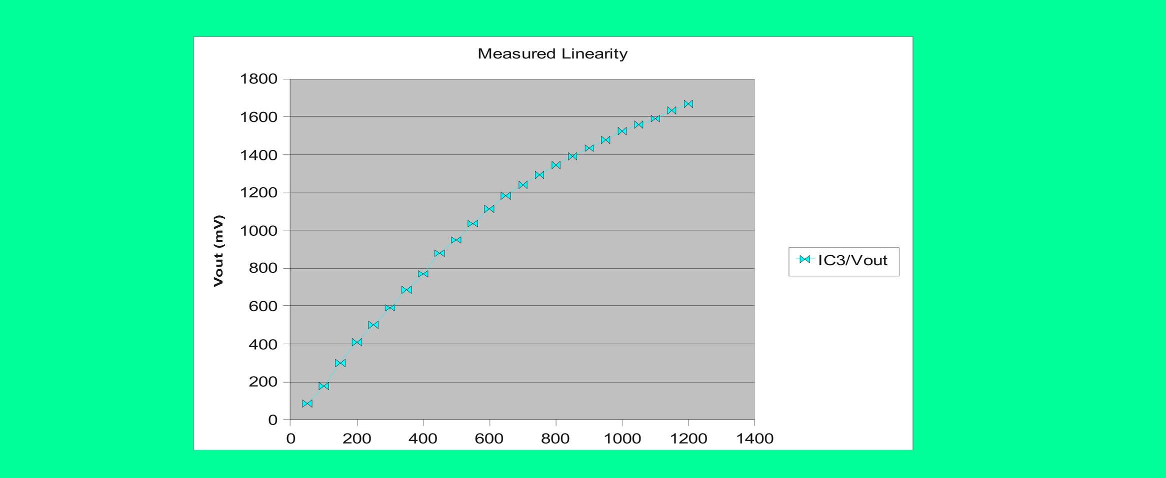


Test Setup

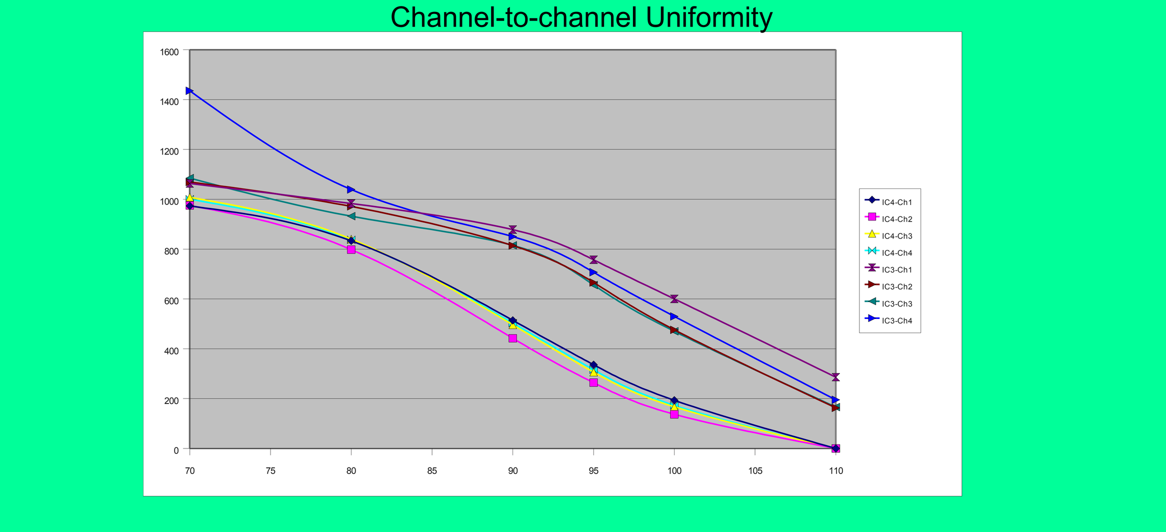


ASD Programmer Software In C#

Simulations / Measurements



Channel-to-channel Uniformity



SUMMARY AND OUTLOOK

- We are testing 2 ASD chips that were radiated (neutrons) at Rez, CZ. Results will be known soon.
- The next version of the chip is scheduled for Spring 2011 with MOSIS using the same 130nm technology.
- This version will have DAC/ADCs on chip, calibration input caps, JTAG, and digital logic.
- Areas to improve are the decoupling of the supply net between the output driver and discriminator/preamp.
- More than 8 channels on the chip are also possible.
- Seperate (not global) threshold setting will be made.
- More testpads