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R&D towards the Module and Service Structure design for the ATLAS Inner Tracker at the Super LHC (SLHC)

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The main goal of this R&D program is to prove to the community that a modular silicon strip tracker concept is a reasonable design that can satisfy the required material, mechanical, electrical and thermal performance specifications throughout the SLHC period. The R&D program places considerable emphasis on design aspects that minimize the development and construction effort and cost, while maintaining an optimal material budget. The University of Geneva and KEK have built four modules respectively with common components and similar procedures. Each site has performed single module tests and 4-module combined tests with local DC-DC converter power supplies and compared them for cross checking. Details of the module design and electrical performance are presented. The status of the 8-module installation in a realistic support structure is also reported.

Summary

The R&D module program is part of the strip upgrade investigation for the future ATLAS Tracker Upgrade. The main goal of this program is to prove to the community that a modular silicon strip tracker concept is a reasonable design that can satisfy the required material, mechanical, electrical and thermal performance specifications throughout the SLHC period. Given the ˜200 m2 surface of the upgraded silicon strip tracker, the R&D program places considerable emphasis on design aspects that minimize the development and construction effort and cost, while maintaining an optimal material budget. A flexible integration of multi-module supports to an overall ID structure is under design and evaluation.

The module concept is based on the present ATLAS SCT. Modularity can help to ease production, quality assurance and repairs. Furthermore, it will give good replaceability and Z-overlapping.

The proposed double-sided silicon strip detector at the super LHC experiment includes four short-strip segments on each silicon sensor to cope with a very high track density. Each module has 10,240 channels read out by 80 128-channel chips. Two hybrids on each module side each have two rows of 10 readout chips, with each row bonded to a strip segment. A total of 36 hybrids have been successfully built. The dead channel rate and the dead chip rate were found to be 0.22% and 0.21%, respectively for probed ASIC chips.

The University of Geneva and KEK have each built 4 modules, with common components and similar procedures. Very uniform distributions for gain and ENC have been observed. The average of gain and ENC are measured to be about 100 mV/fC and about 570e, respectively. These results are in good agreement with the expected design performance. A major aim of the R&D program has already been achieved: the relatively simple and fast fabrication of double sided modules with good electrical performance and low cost. Apart from the powering and the end-of-stave card, the modules contain all the active components, and furthermore their modularity allow easy replacement or rework.

We are planning to install eight double-sided modules in a realistic support structure equipped with all service bus cables. The hybrid is read out via a module control ASIC chip. Low voltage power to the hybrid is stabilized with a local DC-DC converter that enables reduction of power-loss in the long supply cables. The present status is reported.

Furthermore, a half-module was irradiated to a level of 0.4–1.4 x 10ˆ15 p/cm2 using 24 GeV/c protons at the CERN SPS. Measurements of the charge collection efficiency are also presented.

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