

Enhancement of the ATLAS Trigger System with a Hardware Tracker Finder FTK

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The existing three-level ATLAS trigger system is deployed to reduce the event rate from the bunch crossing rate of 40 MHz to ~200 Hz for permanent storage at the LHC design luminosity of $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. When the LHC reaches beyond the design luminosity, the load on the Level-2 trigger system will significantly increase due to both the need for more sophisticated algorithms to suppress background and the larger event sizes. The Fast Tracker (FTK) is a proposed upgrade to the current ATLAS trigger system that will operate at the full Level-1 accepted rate of 100 KHz and provide high quality tracks at the beginning of processing in the Level-2 trigger, by performing track reconstruction in hardware with massive parallelism of associative memories. The system design is being advanced and justified with the performance in important physics areas, b-tagging, tau-tagging and lepton isolation. The system requirement and capability are being evaluated with the ATLAS MC simulation at different LHC luminosities. The prototyping with current technology is undergoing and the R&D with new technologies has been started.

Summary

With the LHC approaching the design specifications, the ATLAS detector will be exposed to proton proton collisions at the center of mass energy of 14 TeV with the bunch crossing rate of 40 MHz. In order to reduce this rate down to the level at which only interesting events will be fully reconstructed, a three-level trigger system has been deployed. The Level-1 trigger reduces the rate down to 75 (100) kHz via the custom-built electronics. The Region of Interest Builder delivers the Region of Interest records to the Level-2 trigger which runs the selection algorithms with the commodity processors and brings the rate further down to ~3.5 KHz. Finally the Event Filter reduces the rate down to ~200 Hz for permanent storage.

The LHC accelerator upgrade is being planned and the luminosity is expected to reach $2.5\text{-}3 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and higher. This makes the trigger task even more difficult since signal rates increase linearly with luminosity and backgrounds go up even more quickly. The suitable trigger strategy should be flexible in order to maximize the trigger capability without knowing a priori characteristic of the new physics. Early track reconstruction can be an important element. At Level-2, tracks coming from a secondary vertex or not pointing to the beamline identify b-jets, while tau-jets can be separated from background using the number of tracks within a narrow cone and the number in a larger isolation region. Electron and muon triggers can also be improved at high luminosity with a track-based isolation while the traditional calorimeter-based isolation degrades.

FTK is an electronics system that rapidly finds and fits tracks in the inner detector silicon layers for every event that passes the Level-1 trigger. Pattern recognition is carried out by the Associative Memory device which finds track candidates in coarse resolution roads. When a road has silicon hits in all layers or all except one, a fit is carried out with the full resolution hits within the road to determine the track helix parameters and a goodness of fit. Tracks that pass a χ^2 cut are kept and their parameters are sent to Level-2. For a given event, it only take a few 100 MHz clock cycles to extract compatible trajectories from the large Associative Memory banks. The FTK is able to compute the helix parameters for all tracks in an event at high luminosity and apply quality cuts in less than 100 microseconds. Thus the FTK will enable early rejection of background events and leave more Level-2 execution time for sophisticated algorithms by moving track reconstruction into a hardware system with massively parallel processing that produces global track reconstruction with near offline resolution.

The prototype is using 180 nm technology. A new design with 90 nm technology is being introduced to maximize the pattern density and to minimize the power consumption. Possible future extensions based on 3-D technology is being investigated.

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