Contribution ID: **25** Type: **Poster**

Mechanics and detector integration in the PANDA Micro-Vertex-Detector

Thursday, September 23, 2010 4:00 PM (2 hours)

The Micro-Vertex-Detector is the innermost detector of the PANDA experiment using silicon pixel detectors in the inner and double-sided microstrip detectors in the outer parts.
The ongoing hardware development, the implementation of the cooling system and the detector integration will be highlighted. This includes a summary of measurements with test systems, the machining of support components and the description of the cooling, cabling and support concept. All information is collected in a detailed detector model which is implemented into the detector simulation package to check the physics performance of the MVD during the detector development.
Supported by EU and BMBF

Summary

The PANDA experiment is part of the FAIR project which is currently under construction at GSI. It is a fixed target experiment using an antiproton beam with a momentum range between 1.5 GeV/c and 15 GeV/c yielding a high luminosity of up to 2×10³²cm⁻²s⁻¹. The expected interaction rate is in the order of 2×10⁷ events per second.
The MVD volume is restricted to a radius of 150 mm maximum in order to fit inside the outer tracking detector of the experiment. It consists of four barrel-shaped sensor layers and six disk layers. These cover a polar angle range from 6° up to 150° in 2π. The innermost layers have a distance of only 2 cm to the nominal interaction vertex. To cope with the high count rates, silicon pixel detectors are used in the inner parts while double-sided silicon strip detectors are used at the outer parts in order to reduce the number of readout channels and thus to minimize the power dissipation. The requested radiation tolerance is in the order of 10¹⁴ n_{eq}cm⁻² within 10 years of lifetime (duty cycle: 50%). Moreover, there is no common first level trigger in the experiment and thus self-triggering readout electronics is required. Due to the fixed target setup, a very anisotropic particle flux will impinge on different regions of the MVD. The maximum count rates for single frontend chips will be in the order of several million events per second.
The current hardware development concentrates on the sensor and readout design, a test-setup for double-sided silicon strip detectors and the development of FPGA-based data acquisition systems. The cooling system is foreseen to work in a leakless underpressure mode using water as coolant. The detector support is based on light carbon structures. First components have been developed and a prototype for the global frame for the integration of the MVD inside the PANDA experiment is commissioned.
A detailed engineering model including the routing, cooling and support concept has been implemented successfully into the physics detector simulation using a CAD converter. With this tool it is also possible to perform a precise mapping of the material budget which is a crucial point for detector optimization. All listed aspects will be discussed in the presentation.

Primary author: WÜRSCHIG, Thomas (HISKP, Uni Bonn)

Presenter: WÜRSCHIG, Thomas (HISKP, Uni Bonn)

Session Classification: POSTERS Session

Track Classification: Systems. Planning, installation, commissioning and running experience