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A 25 GS/s sampling ASIC in a 130nm CMOS technology.

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In the scope of time of flight measurements at the scale of a few pico-seconds, a CMOS fast sampler chip is being developed in a 130nm CMOS technology. It includes a 10-20GS/s timing generator comprising a Delay Locked Loop and programmable sampling windows, and four channels of 256 sampling cells able to record up to of 25 ns of analog information. An input discriminator triggers the freezing of the sampling cells which comprise a comparator allowing an on-chip 12-bit analog to digital conversion. The design and tests results of the sampler ASIC and associated test structures are presented.

Summary

Fast waveform sampling is more and more used for front-end processing of time of flight photodetectors, allowing for instance to reconstruct to the picosecond range the time of arrival of a photon signal.
Micro-Channel Plate devices produce signals with bandwidths in the range of 1-10GHz. In order to make possible the implementation of such a front=end processing on detector systems comprising a large number of channels, an ASIC is under design using the mixed-mode 130nm CMOS process currently available from the Muptiproject Wafer Centers.
The ASIC architecture described comprises switched capacitors array (SCA) timed by a delay locked loop which provides 50-100ps equally spaced clock phases derived from a main 40-80 MHz input clock in order to avoid delays drifts due to temperature, voltage supply and process variations. Variable length sampling windows controls the five-channel SCA, where the input signals are sampled and stored. An input discriminator freezes the sampling process when a given threshold is exceeded.
Each sampling cell comprises a storage capacitor (40fF), a write and a read switch, a voltage follower, and a comparator for on-chip digitization. This ADC converts in parallel the voltages of all cells, it is clocked by a ring oscillator able to run up to 2GHz. A ramp generator allows achieving the conversions in less than 2 microseconds
The chip has been designed using the IBM 130nm CMOS design kit provided by CERN, and sent to foundry in February 2010. A second chip comprising several test structures such as sampling cells, a timing generator and its associated delay Locked Loop components such as a phase detector and a charge pump, a 2GHz ring oscillator, and 50Ohms transmission lines has also been sent to foundry recently. Four full SCA channels and an extra calibration channel have been implemented, fed in parallel by the control signals from the timing generator. Results are presented in terms of sampling rate, differential and integral linearities, noise, analog bandwidth, intrinsic timing resolution as well as with fast Micro-Channel Plate photo-detectors signals as input.

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