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Response of a commercial 0.25 μm Thin-Film Silicon-on-Sapphire CMOS Technology to Total Ionizing Dose

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The radiation response of a commercial 0.25 μm silicon-on-sapphire CMOS technology was characterized at the transistor and circuit levels utilizing standard or enclosed layout devices. Device-level characterization showed ΔVT of less than 170 mV and ΔILEAKAGE of less than 1 nA for nMOSFET and pMOSFET devices at a total dose of 100 krad(SiO2). The increase in power supply current at the circuit level was less than 5%, consistent with the small change in off-state transistor leakage current. The technology exhibits good characteristics for use in the electronics of the ATLAS experiment at the Large Hadron Collider.

Summary

I. Device Description and Experimental Conditions
Two types of shift registers, consisting of 32 D-flip-flop stages, one using standard layout transistors, the other enclosed layout transistors, were fabricated for circuit-level evaluation of radiation-induced leakage current. The shift registers were irradiated with 198 MeV protons while being operated with a 40 MHz clock and the power supply current was monitored. nMOSFET and pMOSFET irradiation bias conditions were VD = 2.5 V and -2.5 V, respectively; all other terminals were grounded. This off-state condition is the worst case for inverters exposed to total ionizing dose. The transistors were irradiated with 10 keV x-rays at a dose rate of 31.5 krad(SiO2) per minute. ID-VG sweeps were performed to characterize the leakage current and threshold voltage of irradiated devices. The sapphire substrate was grounded for both the circuits and devices during irradiation.

II. Experimental Results
In the device-level characterization, an initial positive shift in threshold voltage, the maximum of which was 170 mV, was observed at less than 1 krad(SiO2). No additional threshold-voltage shifts were observed following the initial exposure, up to the largest dose considered here (100 krad(SiO2)). The initial threshold-voltage shift, which is less than the corner-to-corner process variation, is attributable to radiation-induced electron trapping in the sapphire substrate.

The post-irradiation increase in power supply current at the circuit level was less than 5%, which was consistent with the relatively small radiation-induced change in off-state transistor leakage (less than 1 nA at 100 krad(SiO2) for both nMOSFET and pMOSFET devices). Leakage current was consistently higher for standard layout devices than for enclosed layout devices following irradiation because of the elimination of the parasitic edge leakage path in the enclosed layout devices. The increase in leakage current with increasing dose is caused by the formation of a back channel along the sapphire-silicon interface. The off-state drain current increased with increasing drain bias, consistent with carrier generation in the expanded depletion region near the drain and at the sapphire substrate interface.

III. Conclusions
Single transistors and shift registers fabricated in a commercial 0.25 μm SoS CMOS technology were irradiated with 10 keV x-rays and 198 MeV protons, respectively. Radiation-induced changes in threshold voltage were minimal after an initial small shift. At the transistor level, leakage current was observed to be 1 nA or less. This result is consistent with the 5% increase in power supply current observed at the circuit level. The technology shows good radiation response to a total dose of at least 100 krad(SiO2), and appears to be very well suited for operating in the ATLAS TID environment.

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